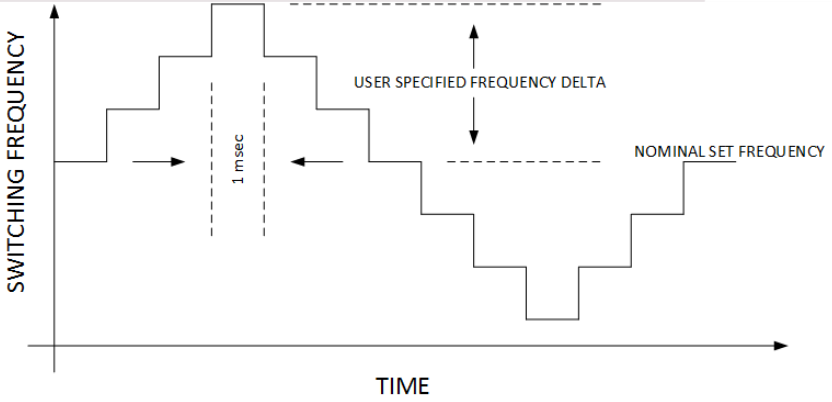
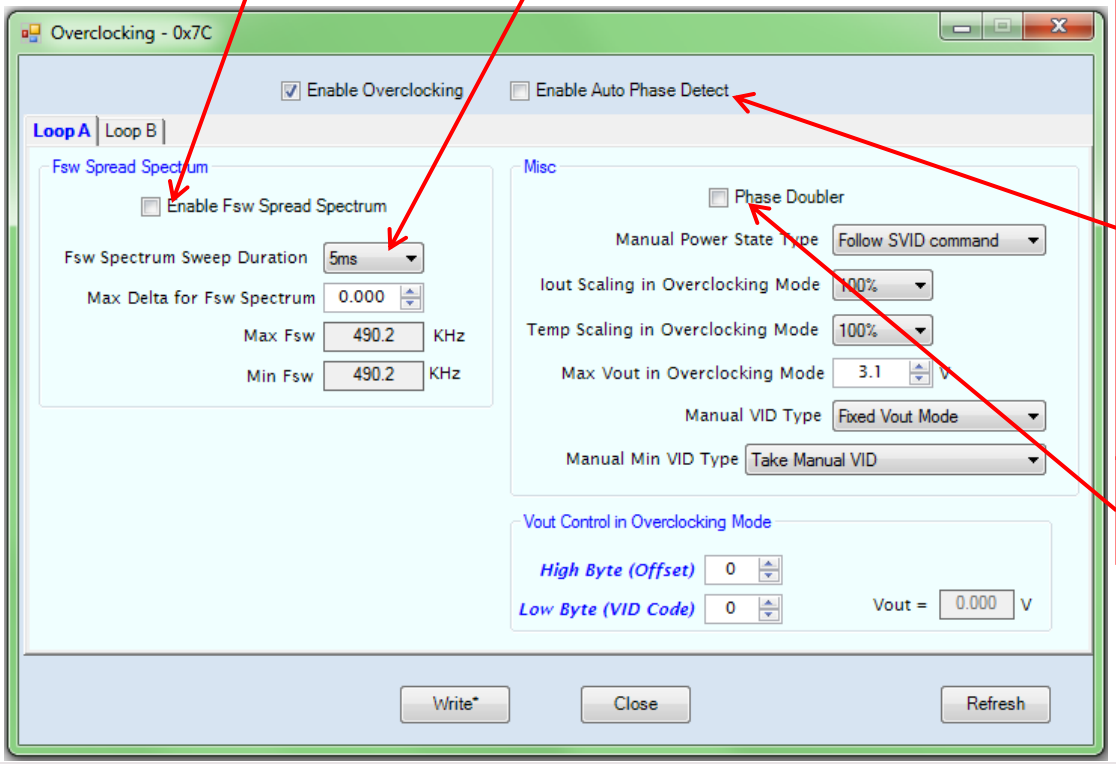
Overclocking...

Fsw Spread Spectrum
Frequency will step up and down between a Maximum **Max Fsw** and a Minimum frequency **Min Fsw.** Step size will depend on number of phases and the set duration



Enable Fsw Spread Spectrum
If marked the frequency will shift between a max and a min value with a selectable repetition frequency

Fsw Spectrum Sweep Duration
How long time for a full cycle of frequency change



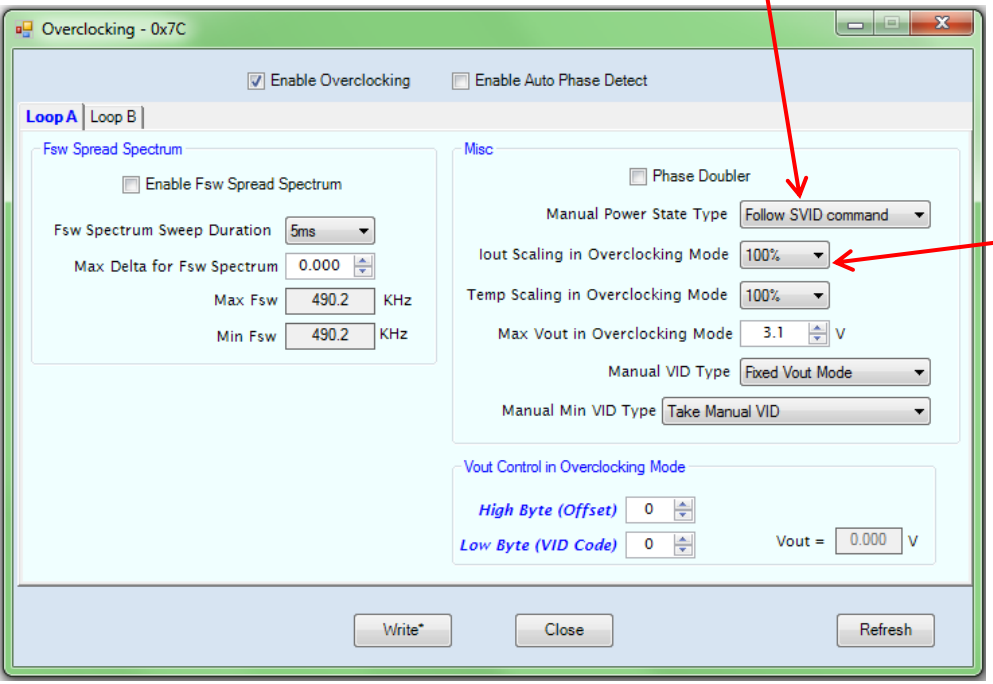
Enable Auto Phase Detect
XDPE10281 is capable of supporting automatic detection of populated phases by measuring the PWM pin voltage after VR_EN assertion, driver VCC POR and VIN greater than the VIN 'ON' Threshold

- Phases must be populated from lowest to highest
- Unpopulated PWM pins must be open (floating)
- A momentary weak pull down will be applied when the PWM pin voltage is sensed

Phase Doubler
Tick if using dual powerstages per phase with a splitter for the PWM signal

Overclocking…

Manual Power State Type:
Either Follow SVID command or force to PS0 that means all phases are active.



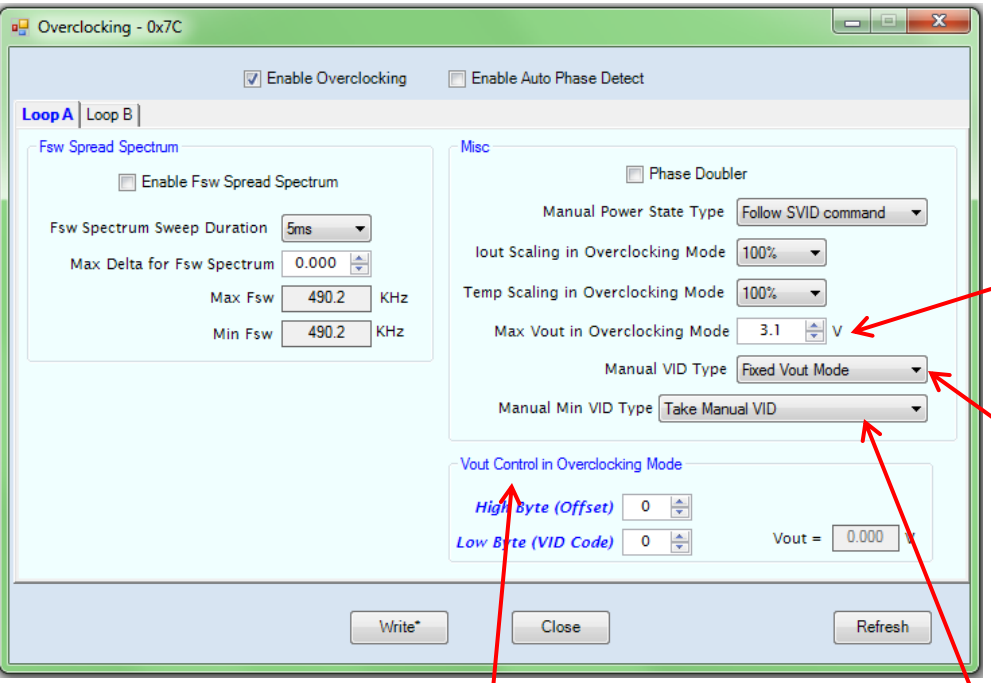
Iout Scaling in Overclocking Mode
and
Temp Scaling in Overclocking Mode
will allow the user to select 25%, 50% or 100% reporting of IOUT(SVID/SVI2) and temperature(SVID) per loop

These settings will only be valid when VOUT is set by the Manual VID ??

Only SVID/SVI2 telemetry will be scaled
I2C and PMBUS reporting will not be scaled, they will report 100% of the actual IOUT and temperature.

Over temperature shutdown will be based on the unscaled (100%) temperature value
OCP will be based on the unscaled (100%) IOUT value

Overclocking…



Max Vout in Overclocking Mode:
Allow a maximum Vout to be set. Any command to set a higher Vout will be ignored and actual Vout will stop at the selected voltage even if commanded to go higher

Manual Min VID type
Select between Take Manual VID orTake MAX of SVID or MAN VID

Manual VID type:
Fixed Vout Mode
Fixed offset mode
In 'Fixed VOUT' Mode, VOUT is set by the VID code specified by the operating mode.
In 'Fixed VOUT' Mode, the SVID ALERT# will assert immediately upon receipt of an SVID command to change VOUT.
- Because VOUT will not change, T_alert assertion will **not** be delayed by VID_DELTA/SLEW_RATE
- In AMD SVI2, VOTF Complete will not assert in Fixed VOUT mode

In 'Fixed VOUT' Mode, changes to the Manual VID register will cause VOUT to change but will not cause SVID ALERT# to assert.
Writing the Manual VID register to 0 will cause VOUT to return to the SVID/SVI2 commanded voltage

Vout control in overclocking mode
Allow MANUAL VID settings
Offset : can be + or - offset
VID code: Vout follows the AMD VID table except for 0 that will cause VOUT to return to the SVID/SVI2 commanded voltage

This functio also work in non overclocking mode to manually enter VID code to set Vout.

NOTICE if Vout been set by a SVI2 command then it is not possible to set a lower output voltage than that command set.