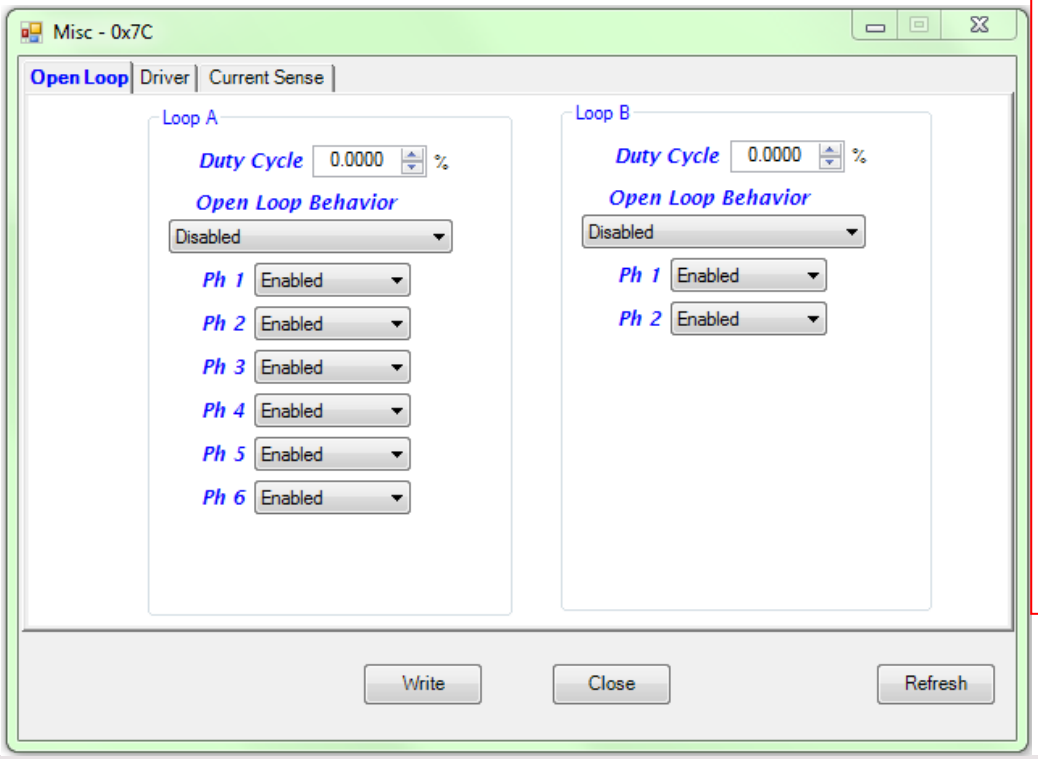
MISC... Open Loop

Duty Cycle
- Fixed duty cycle in open loop

Open Loop Behavior
- *Disabled*: Open loop is disabled
- *Close Loop with Phase Control*
- *Open Loop with Phase Control* controller will send out a fixed **Duty Cycle** .

PH 1/2/3/4/5/6
- *Enabled*: phase 1/2/3/4/5/6 will operate in open loop test
- *Hi-Z*: phase 1/2/3/4/5/6 is not activated.



In open loop mode, output voltage faults (OUVP) protection and all ATR events must be disabled to prevent premature shutdown and false tripping of the ATR.

Step 1: (Important) make sure VR is turned off. i.e. Enable signal low
- It is strongly recommended that the VR be disabled when the user is disabling/enabling open loop function. Otherwise, undesired damage may occur at the power stage.

Step 2: Select the **Open Loop Behavior**
Closed Loop with Phase control
or
Open Loop with Phase Control

Step 3: Set the **Duty Cycle**
- Should be greater than 0%
- To check whether the power stage is operating, a low duty cycle is recommended, typically ~ 10%.

Step 4: Select **PH** x behavior for each Phase
Enabled
or
Hi-Z

Step 5: Click the **Write** button to activate the settings

Step 6: turn on regulator i.e. by enable signal

MISC...

Controller PWM Tri-state type

1.5V: PWM will be force to 1.65V when controller would like to turn off both HSFET and LSFET. This setting is used for drivers which do not have an internal divider to force a Tri-state condition.

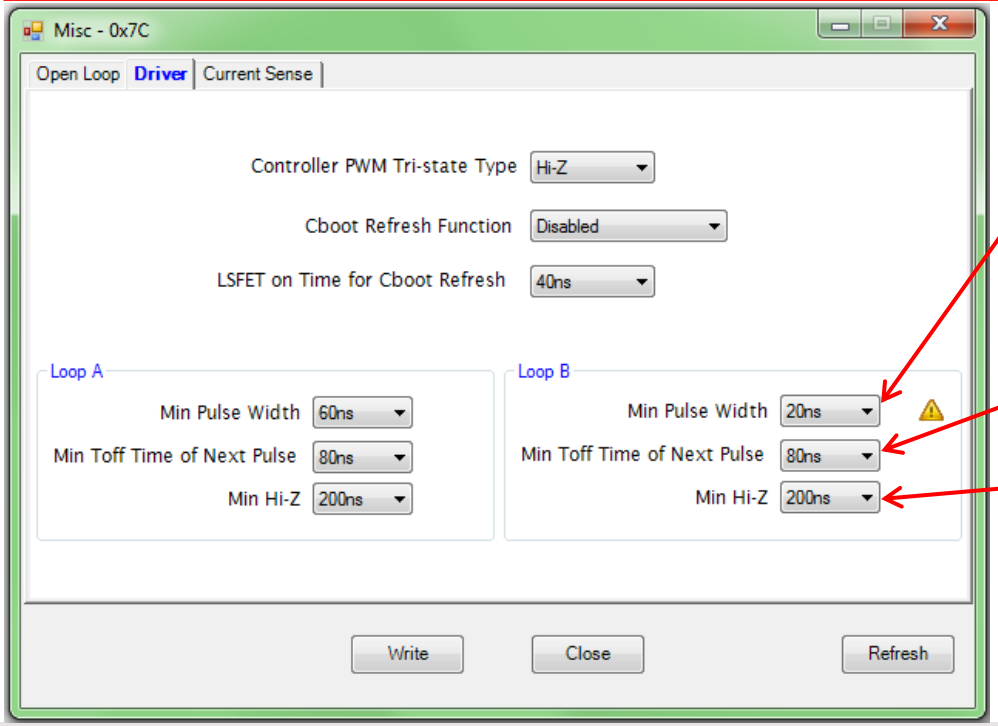
Hi-Z: PWM will stay hi impedance when controller would like to turn off both HSFET and LSFET. The voltage on the PWM for Hi-Z will be determined by the driver's internal divider.

Cboot refresh function

- In some operating modes i.e. Tri-State the PWM may be turned off for a longer time and then Cboot capacitor at powerstage may discharge. This function will allow a short PWM pulse to be issued at regular inteval to restore charge in the capacitor
- Disabled or every 4 , 8 or 16th regular PWM cycle

LSFET on Time for Cboot Refresh

- Setting for how long time the Lowside MOSFET is to turn on each time the Cboot refresh function trigger.



Min Pulse Width

Minimum pulse width(ns)which can be handled by driver. Some drivers need a minimum length of the PWM pulse

In this example there is a yellow triangle next to the selection warning of too short time selected

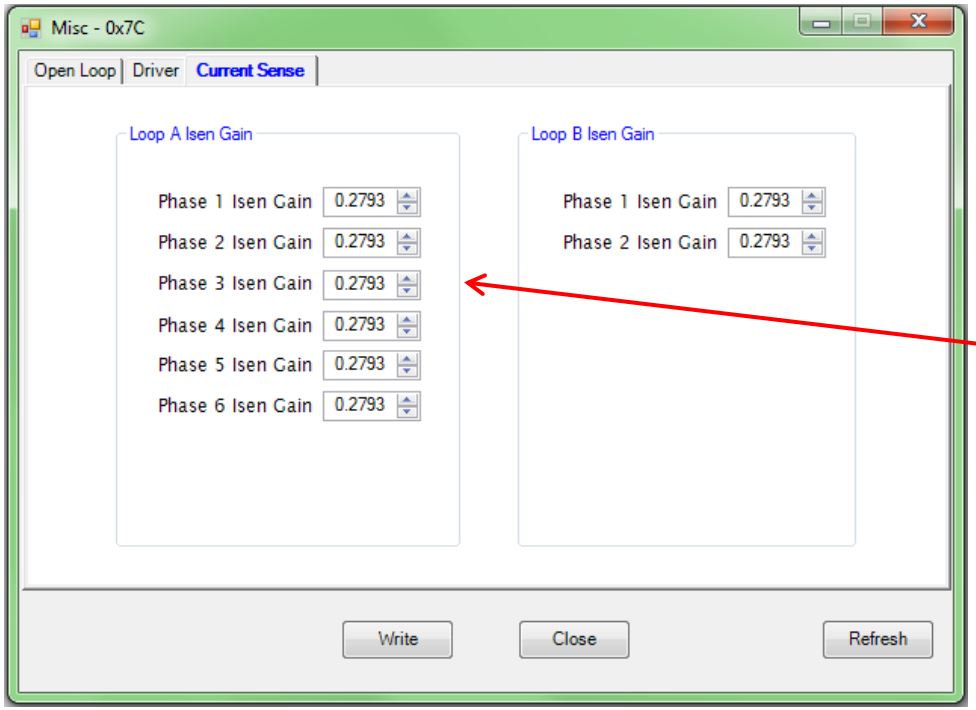
Min Toff time for next Pulse

Minimum PWM low (ns) before the next PWM high pulse

Min Hi-Z

Minimum time (ns) for the PWM to remain low before transitioning to PWM Hi-Z

MISC...



Isen Gain
Same setting as for the Igain setting in **Current Sense** Window.

In some cases there may be a whish to adjust the gain for each phase to compensate for layout or other losses.
Then enter the modified values here.