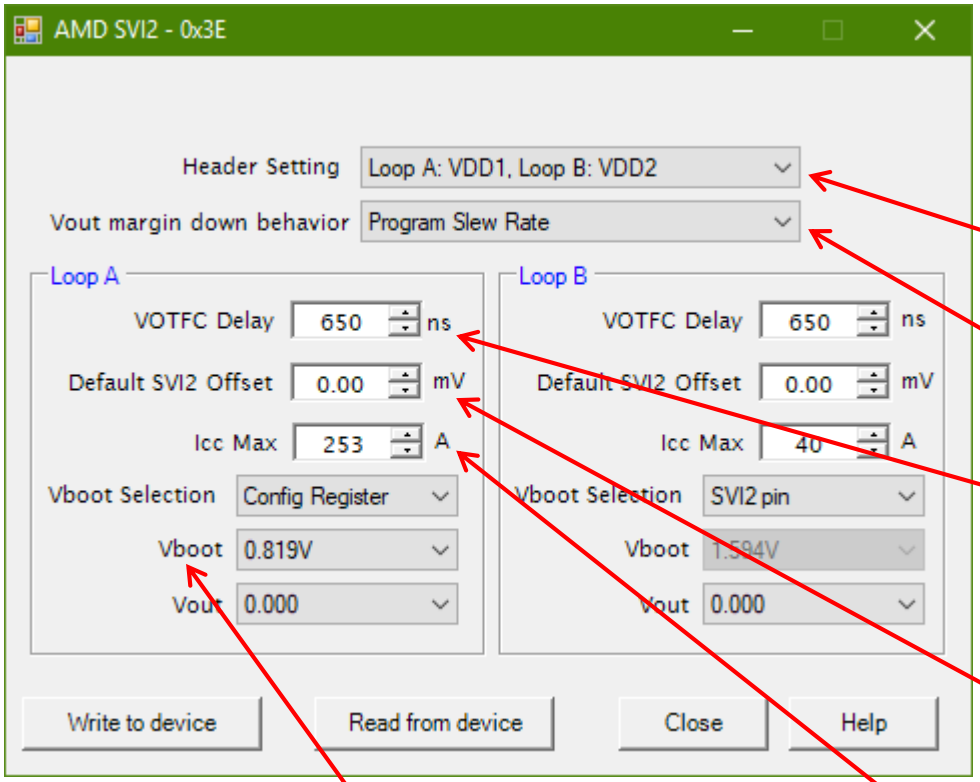
AMD SVI2...

This window contains the settings relevant to SVI2 operation to meet AMD requirements



Header Setting
Controls which of loop A and B are assigned to VDD1 and VDD2.

Vout Down behavior
Select if decay or slew voltage down

VOTFC Delay: Voltage On The Fly Complete signal. Can be set to delay the VOFTC signal after Vout ramp completed. Example: in case of a small overshoot the delay allow Vout to stabilize

Default SVI2 Offset
Compensation for any offset from the requested SVI2 voltage level to what Vout really is.
On a design where the Vout do not match the SVI2 voltage this offset can be adjusted.
Reason for offset can as example be layout of the PCB causes some small voltage drop.

Vboot selection
Select if boot voltage is selected by the SVI2 pins or read from configuration Vboot

Icc Max is the setting for full scale current for the reporting via the SVI2 bus. Set it to the maximum current expected.