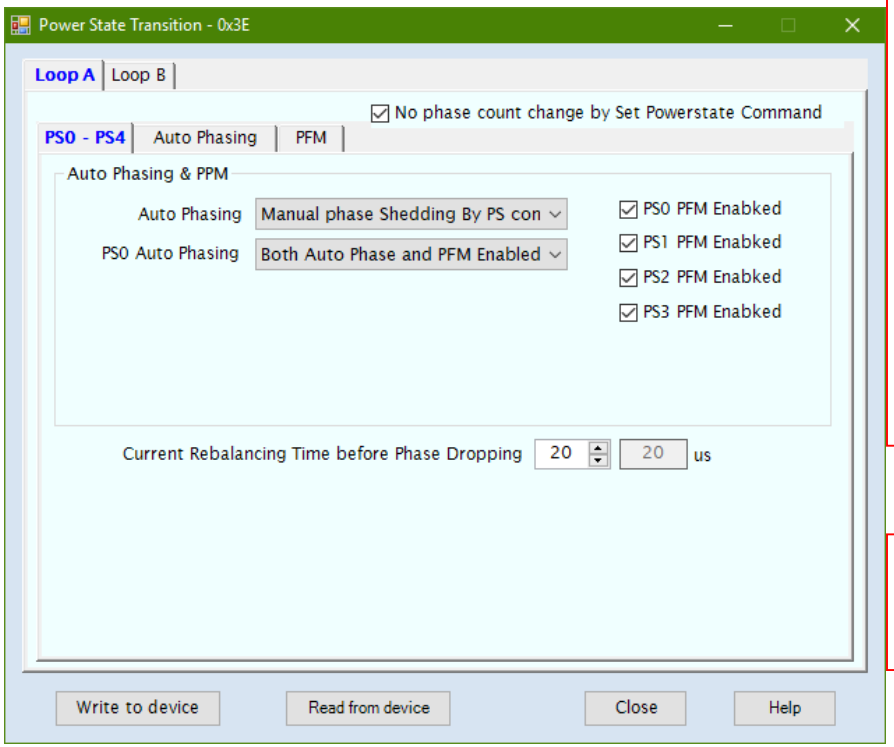
Power State Transitions...

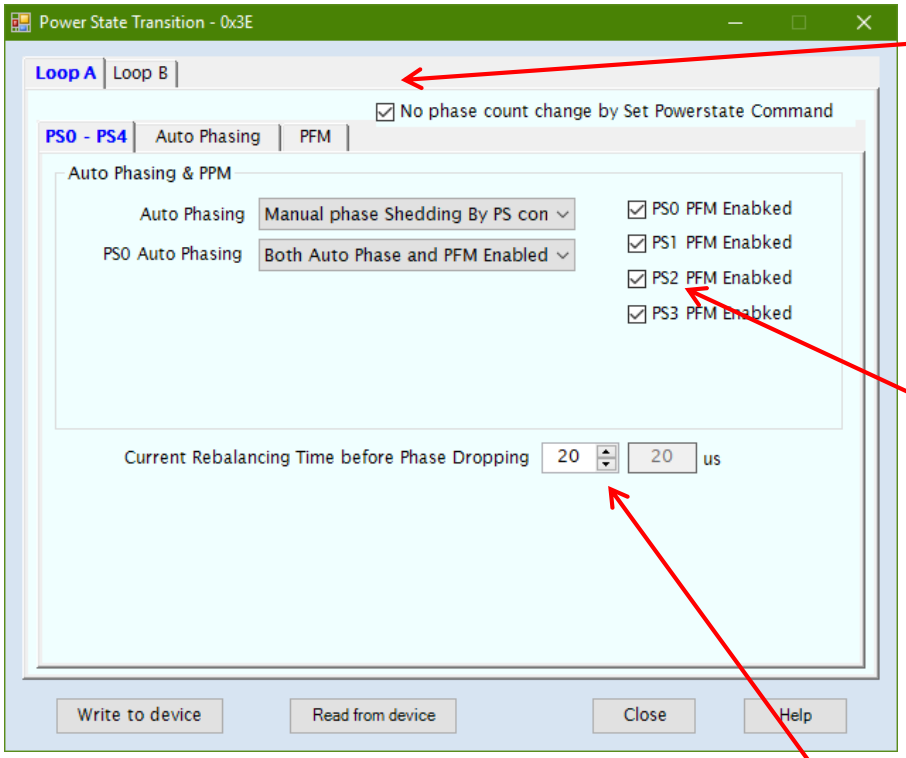


Auto Power State Definitions

- PS0→ more than 1 phase operation
  - IOUT is greater than the 'phase add' current threshold
- PS1→ 1 phase (or 2 phase) operation
  - IOUT is less than 'phase add' current threshold
  - IOUT is greater than PS2 threshold
- PS2→ Diode Emulation, Constant on-time, variable frequency
  - IOUT is less than PS2 threshold (typically set between 5A and ½ inductor ripple current)
- PS3
  - Same as PS2

Power State PS0
Is automatically selected when in Overclocking mode or manual selected Vout.

Power State Transitions...



No phase count change by set PowerState Command
When checked, the controller will always operate at PS0 mode. PS commands on the SVID bus are ack'd but will not be reacted to.

PS0/1/2 Auto Phasing
- Specifies the auto phasing function for PS0, PS1, or PS2
  - Disabled: Auto phasing and PFM are disabled
  - Auto phasing is enabled only
  - Auto phasing and PFM enabled

PS3 PFM
- Specifies if PFM is enabled for PS3 operation for extra power savings
  - Disabled –PFM is disabled

◆ When disabling/enabling auto phasing function, PID will get change. This is due to PID scaling function is enabled when auto phasing is enabled.
If PID for Max phase operation is changed, just change back to original value before again selecting auto phasing disabled.

Current Rebalancing Time before Phase Dropping
–This is used to set the delay before phase dropping (includes by PS command and auto phasing). During this period, the controller is trying to unload the current from the phase to be dropped

Power State Transitions... Auto Phasing

Thresholds for Dropping Phases:
–At which output current should a shift to less number of phases occur.
Example: As Iout current drop below 26A there will be a change from 4 phases to 3 phases.

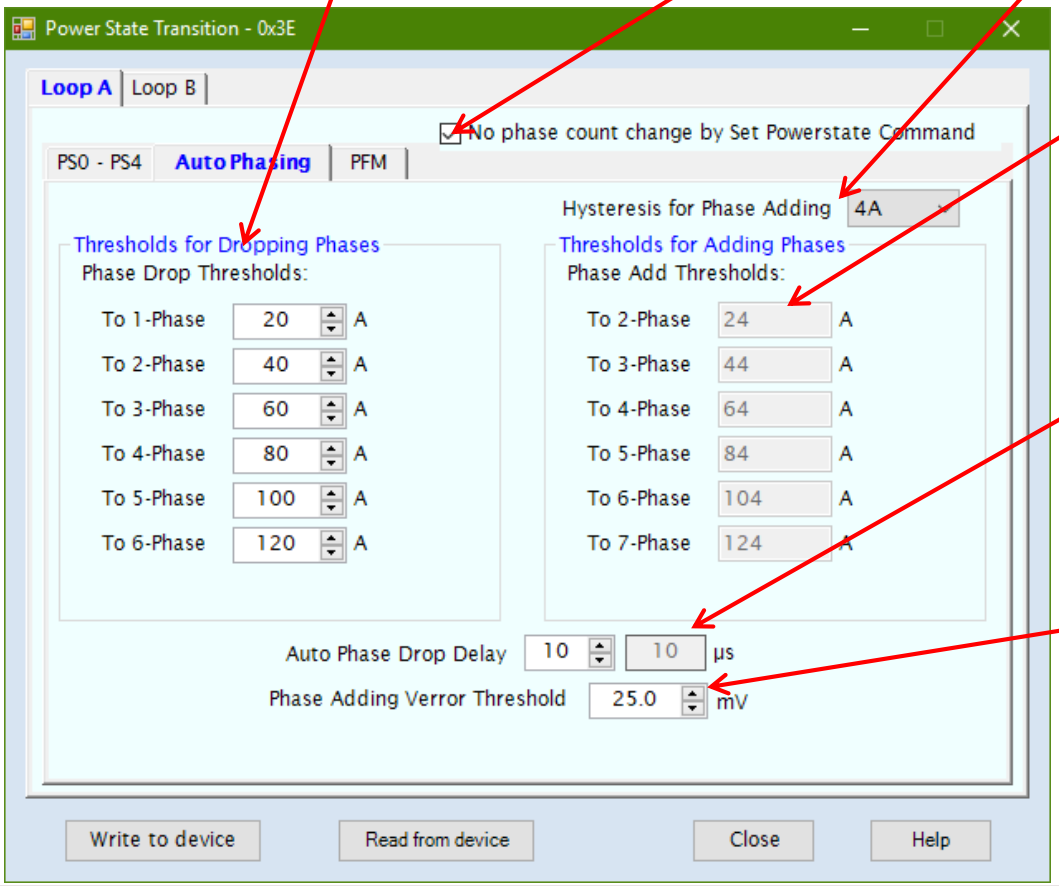
No phase count change by Set Powerstate Command:
–Do not change number of phases even if Powerstate is changed when box ticked

Hysteresis for Phase Adding:
–To avoid too many add/drop of phases a hysteresis can be set. This avoid a continuous change of number of phases if current is just at the set threshold

Thresholds for Adding Phases:
– Calculated from the Hysteresis and the set value for dropping phases. When Iout is higher than the shown current one phase is added

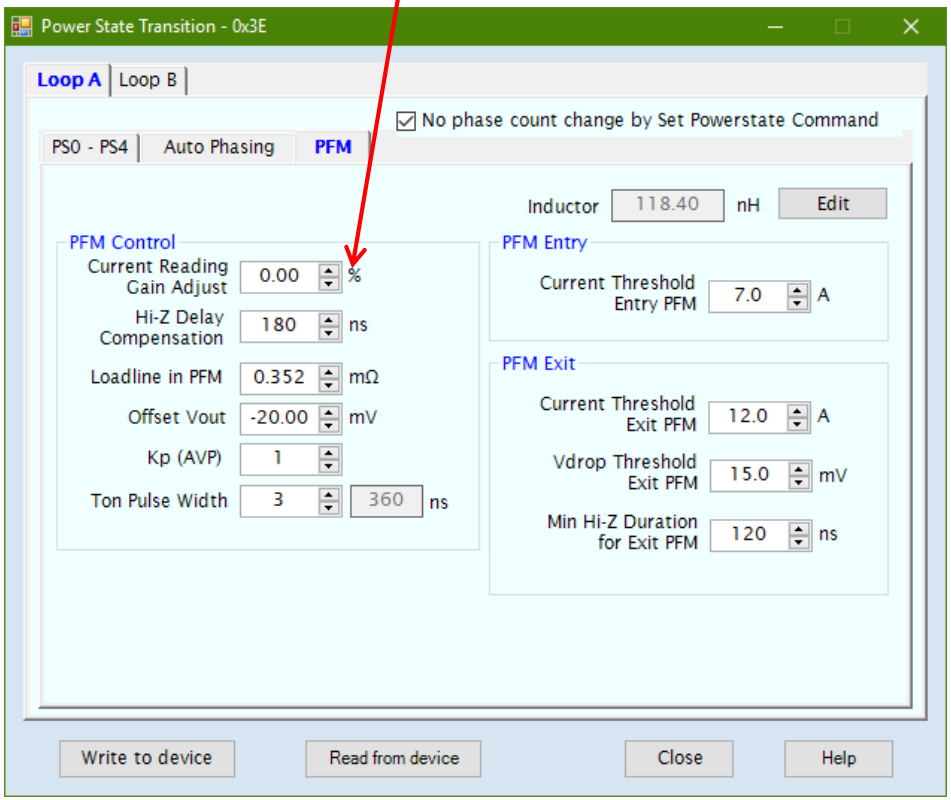
Auto Phase Drop Delay
–For autonomous phase dropping to occur, the output current needs to remain lower than the drop threshold for the entire period of time specified by the Auto Phase Drop Delay parameter.

Phase Adding Verror threshold
–When the error voltage is larger than the specified value, the controller will proceed to add all phases immediately.



Power State Transitions... PFM

If any of the selections for Autophasing select PFM function then a PFM tab is added in the window



Current Reading Gain Adjust
Adjustment to the current reading accuracy in PFM mode

Hi-Z Delay Compensate
Reduces the actual off-time of the PWM signal in order to compensate the power stage delay in transitioning from off to Hi-Z

Loadline in PFM
Define how much Vout is adjusted by load current in PFM from 12.5% to 100% of the load-line setting

Offset Vout
Adjust the threshold voltage for the PFM comparator to initiate a new PFM cycle (on/off pulse) when the Vout reaches or drops below this threshold. The threshold should be raised or lowered so that the PFM ripple stays well within the regulation window allowed under PFM.

Kp (AVP)
A delta-term to reduce the bandwidth of the AVP loop during PFM mode

Current Threshold Entry PFM
In 1-Phase PWM mode, the output current must reach this threshold in order to enter PFM mode

Current Threshold Exit in PFM
Exit from PFM under conditions of overcurrent (i.e. 2-3A above the PFM/PWM efficiency cross-over load)

Vdrop Threshold Exit PFM
The threshold at which a transient would trigger an exit from PFM to PWM operation
ATRH1 must be enabled for this function

Min. Hi-Z Duration for Exit PFM
Exit PFM if the Hi-Z time of 6 consecutive PFM cycles is less than this threshold
Configure this threshold such that an exit condition occurs at the PFM/PWM crossover efficiency load-level