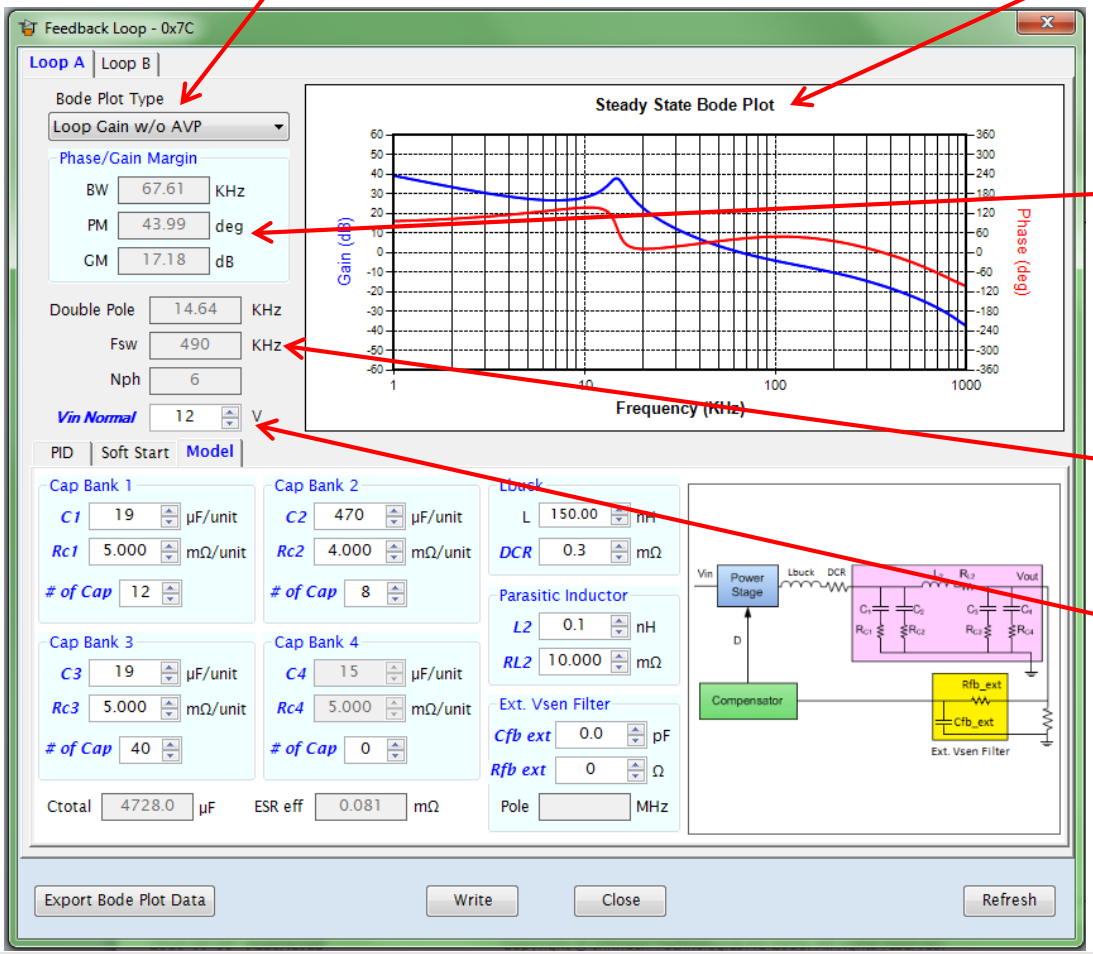
Feedback loop

Bode Plot Type:

Pull down menu where different types of Bode plots can be selected

Bode plot

Shown for the condition that is selected under the **Bode Plot Type** button



Phase /Gain Margin is calculated based on the parameters entered in **Model** tab

BW Bandwidth. Where gain passes 0dB

PM Phase Margin

GM Gain Margin

For Information these parameters are shown

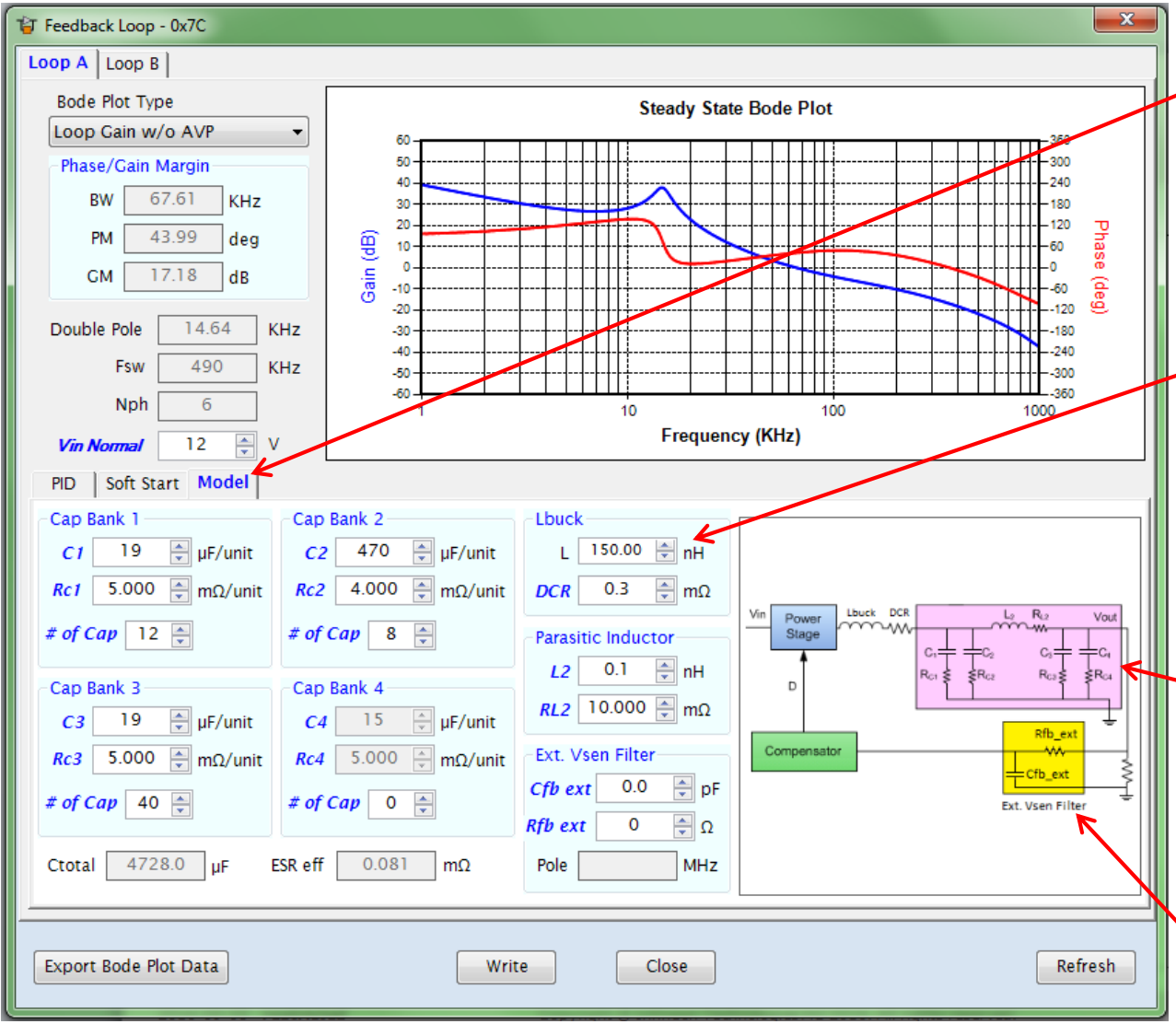
Double Pole: The pole due to output L and C

Fsw: Switching frequency

Nph: Number of phases

Input voltage: Used for calculations

Feedback loop Model



Recommend to start with the **Model** tab as Bode plot depends on Model being set up with what values used.

Any derating of Ceramic capacitors due to voltage must be considered before entering Capacitor values.

Lbuck:

Here the Inductor value is entered. This Inductance value is saved in a register inside the controller and important to set correct for calculations to be right.

Other L and C related values on this page is used by GUI only for Bode plot and simulations. They are not saved in controller

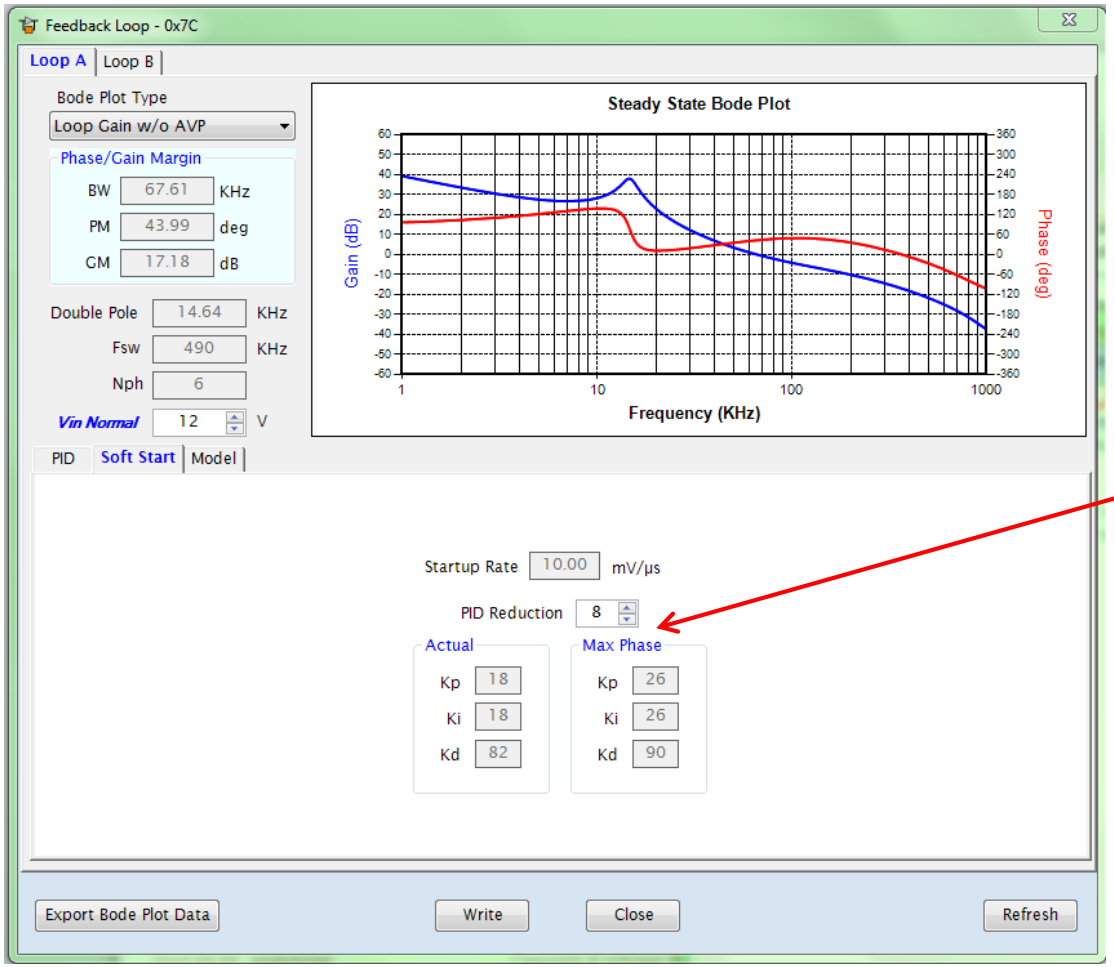
Model simulates a CPU in a socket. Cap bank 1 and 2 are MLCC and bulk capacitors after inductors. Bank 3 and 4 are MLCC capacitors inside the socket.

Parasitic inductor L2 and R_{L2} simulate the impedance of the copper traces into the socket

Ext Vsen Filter:

Simulates any resistance and capacitance in the feedback path. i.e. a 10ohm resistor that is used to inject signals for Bode measurements

Feedback loop Soft Start



Slew rate is for information and can be selected in another place.

During softstart the PID values can be reduced to slower settings.

They do not need to be as fast responding during soft start as during normal operation.

i.e. Not the same big transients to handle.

The lower settings allow a smoother monotonic ramp of Vout

PID compensation can be optimized during soft start.

Startup Rate

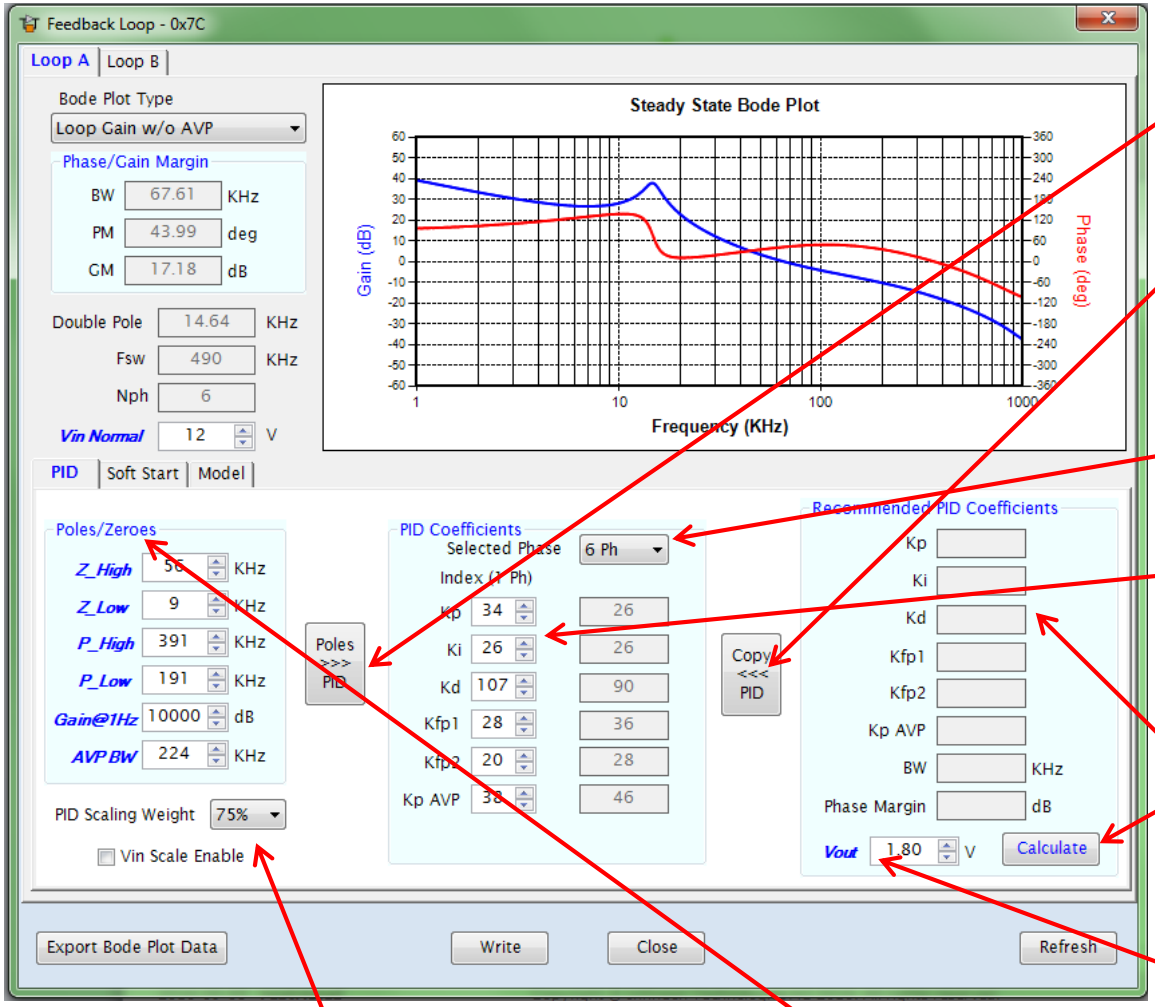
–Effective startup ramp rate

–The startup rate can be changed in the On/Off Settings dialog

PID Coefficients

–During start up: adjust the voltage feedback loop compensation during the initial start up period only

Feedback loop PID



Poles >>> PID button

Poles / Zeros can be converted to **PID Coefficients** by clicking this button

Copy <<< PID button: copies **Recommended PID Coefficients** to the **PID Coefficients**

Selected Phase: For information the PID coefficients for different number of phases can be shown for information.

PID Coefficients: the coefficients can be entered directly or calculated by the GUI using the buttons.

Recommended PID Coefficients

GUI can calculate a set of recommended coefficients

- **Calculate button**: displays the calculated PID coefficients based on the entered values in the **Model** tab, **Vin** and **Vout**

Vout: Output voltage Used for internal calculations of PID in the GUI

PID Scaling Weight
Vin Scale Enable See following slides for explanation. Typical setting 75%

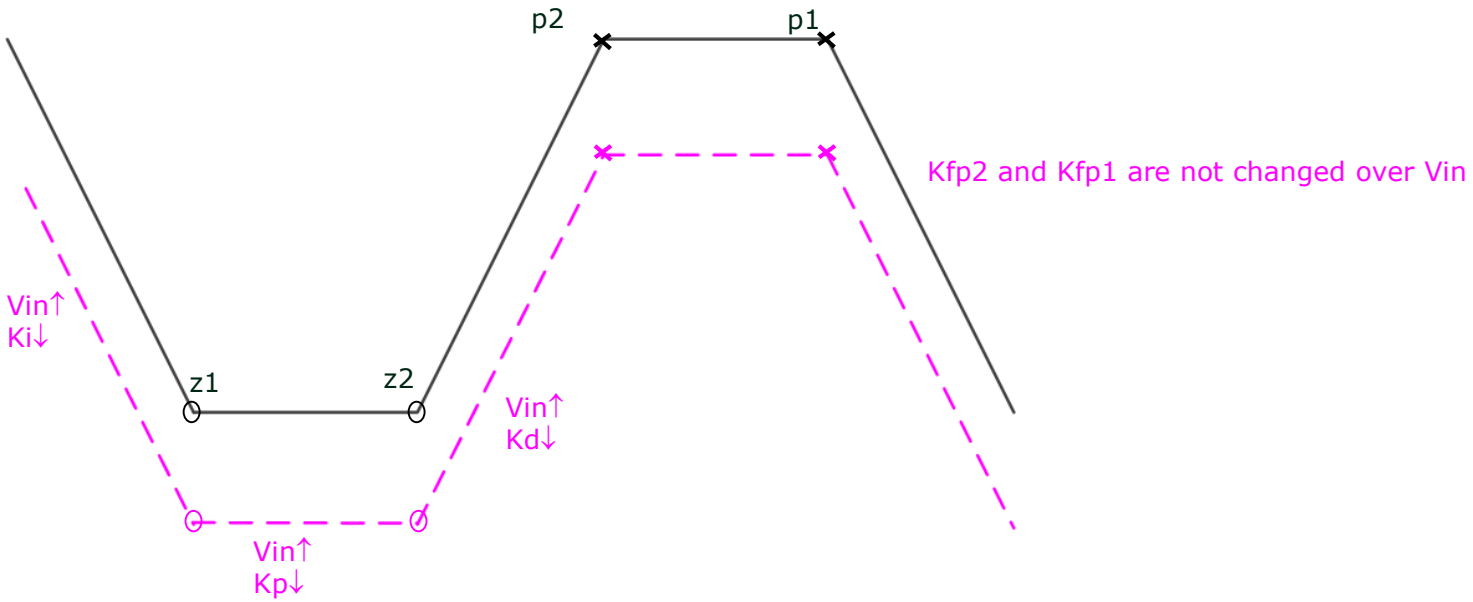
Poles / Zeros

Enter the parameters for the desired Poles and Zeros. GUI can convert this to PID coefficients

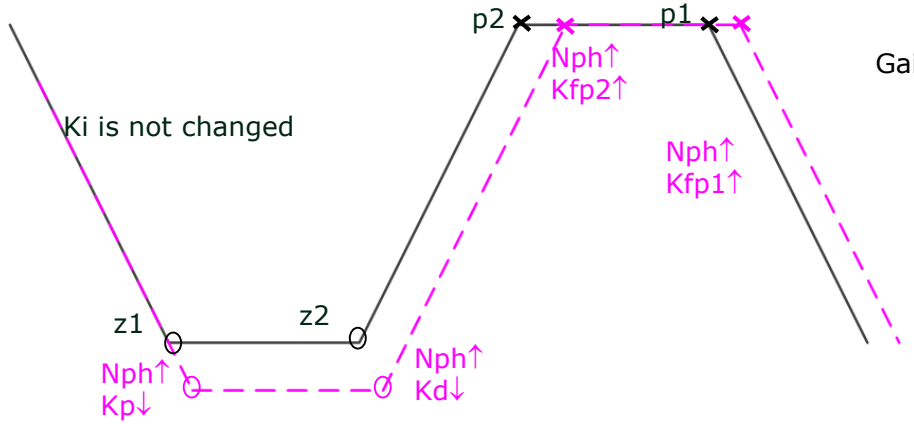
Vin scaled PID

- Kp, Ki, Kd can be programmed to be scaled over Vin to
  - Maintain the same zeros and poles location
  - Keep the same gain

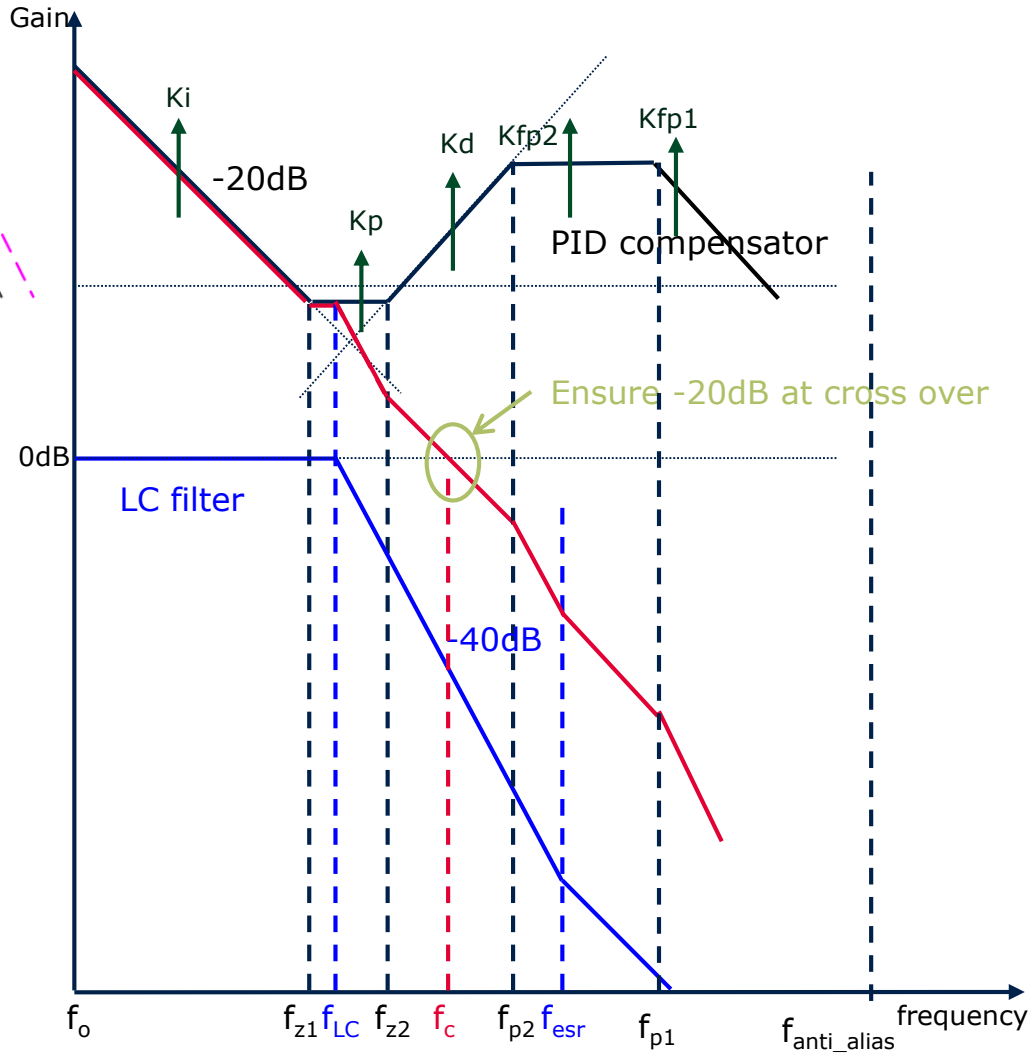
  Note: Kfp2, Kfp1 and Kp(avp) are unchanged over Vin



PID scaling over Nph change (1 of 2)



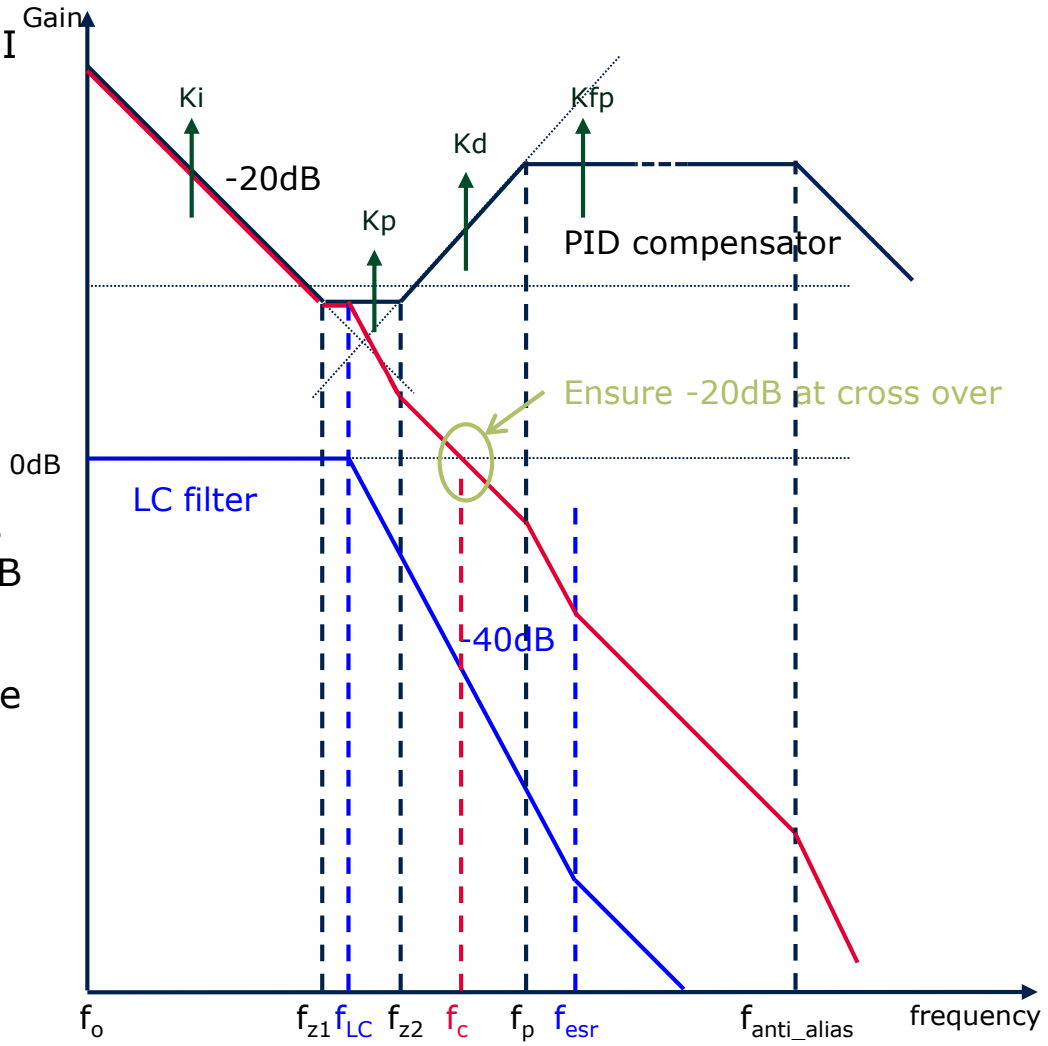
- Kp, Kd, Kfp2, Kfp1 and Kpavp will be scaled automatically as the Nph is being added or dropped. Note: Ki is not changed
- As Nph is increasing
  - Kp, Kd is decreasing
  - Kfp2, Kfp1, Kpavp is increasing
- Change of Kd is proportional to Nph and Kp, Kfp2, Kfp1 and Kpavp are proportional to square root of Nph
- z1, z2, p2, p1 are moved to the higher frequency when Nph is increasing because double pole location is moved to higher frequency



Feedback Loop PID: Compensator – Steady State (Voltage Loop)

PID coefficients

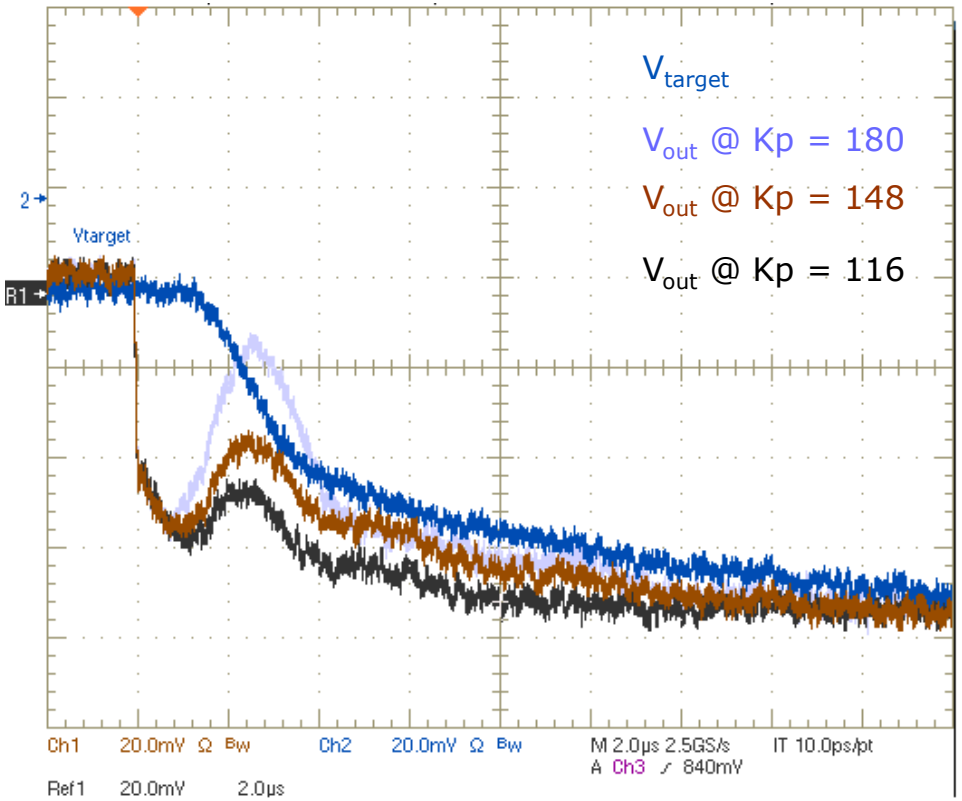
- PID compensator: similar to Type III compensator
  - f_{z1}: 1st zero of PID compensator (Ki and Kp intersection)
  - f_{z2}: 2nd zero of PID compensator (Kp and Kd intersection)
  - f_o: pole at origin (Ki)
  - f_p: high frequency pole (Kd and Kfp intersection)
  - f_{anti_alias}: high frequency anti-alias pole @ around 10MHz for LoopA/B
  - LC filter:
    - f_{LC}: output LC filter double pole
    - f_{esr}: ESR zero of C_{out}

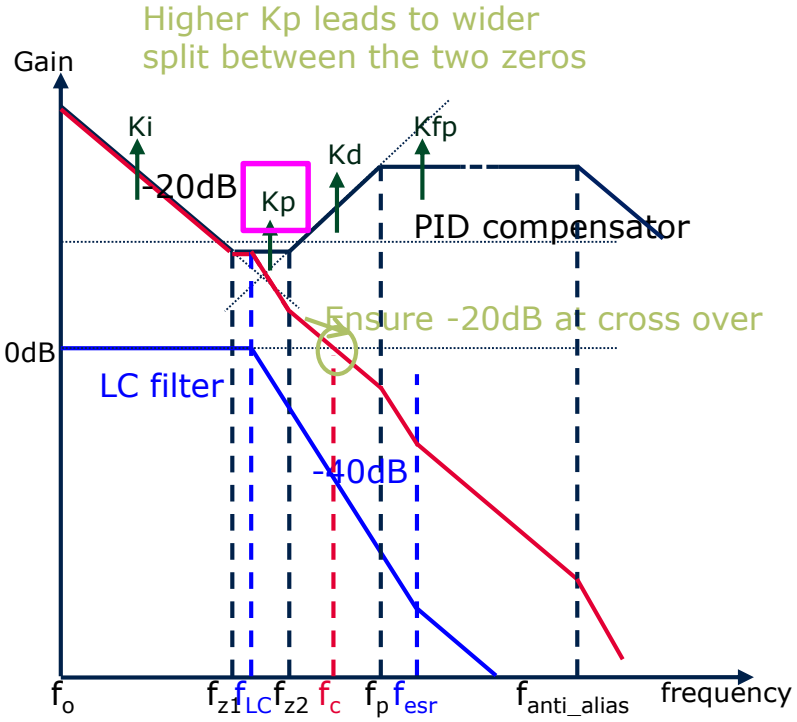


Feedback Loop PID: Recommendations for Designing a Stable Voltage Feedback Loop

- The first zero should be placed on the left side of the LC filter's double poles, and the second zero placed on the right side of the double poles
- The cross-over frequency (fc) or bandwidth (BW) should not exceed 1/4 of the switching frequency
- The Gain should cross the 0dB threshold with a slope of -20dB /dec
- **Kp**/**Ki**/**Kd**/**Kfp** values are larger for lower phase-count than that for higher phase-count
- PID coefficients are non-linear. Coefficient index delta of 32 is equivalent to 6dB change in gain
- **Kp(AVP)** should be smaller for VR's where a large DC load-line setting is required

Feedback Loop PID: Steady State Voltage Loop Compensation Kp impact on transient

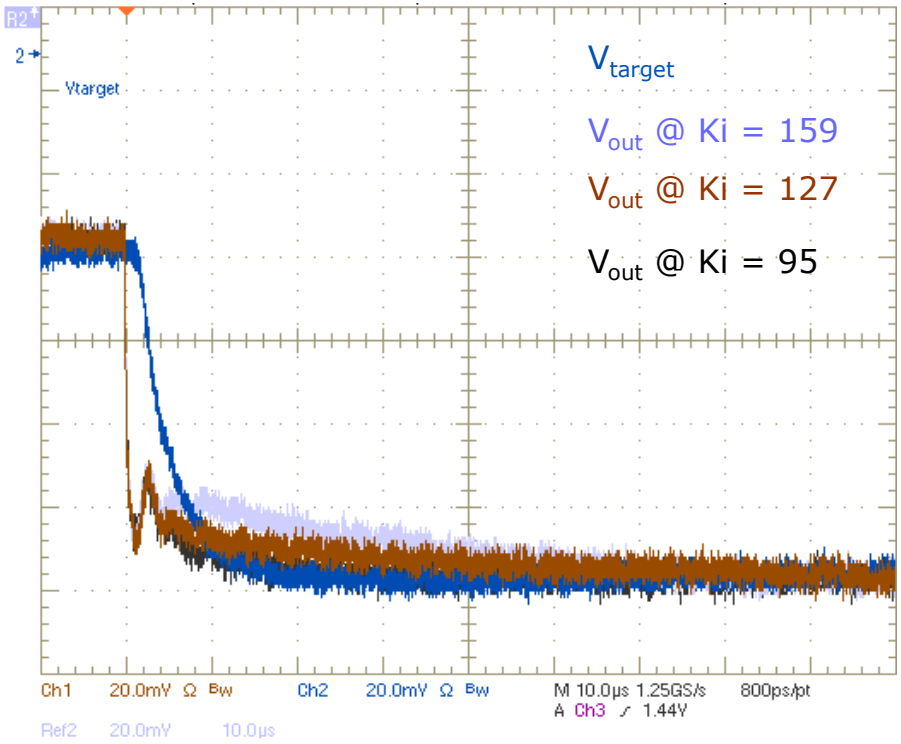


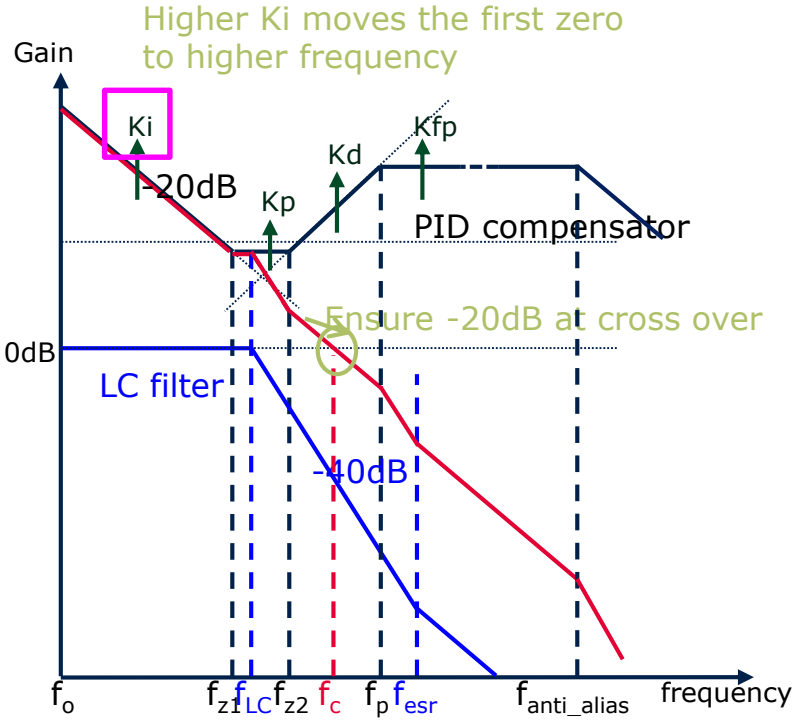


- P term is proportional to Verr. The higher the **Kp** the higher the BW, but the higher the ring back
- From the time domain transient response:
  - **Kp** mainly affects the first ring back amplitude
  - **Kp** has some impact on first undershoot beyond 100ns of load stepping

Note: **Kp** affects the transient response within the first 5us

Feedback Loop PID: Steady State Voltage Loop Compensation Ki impact on transient

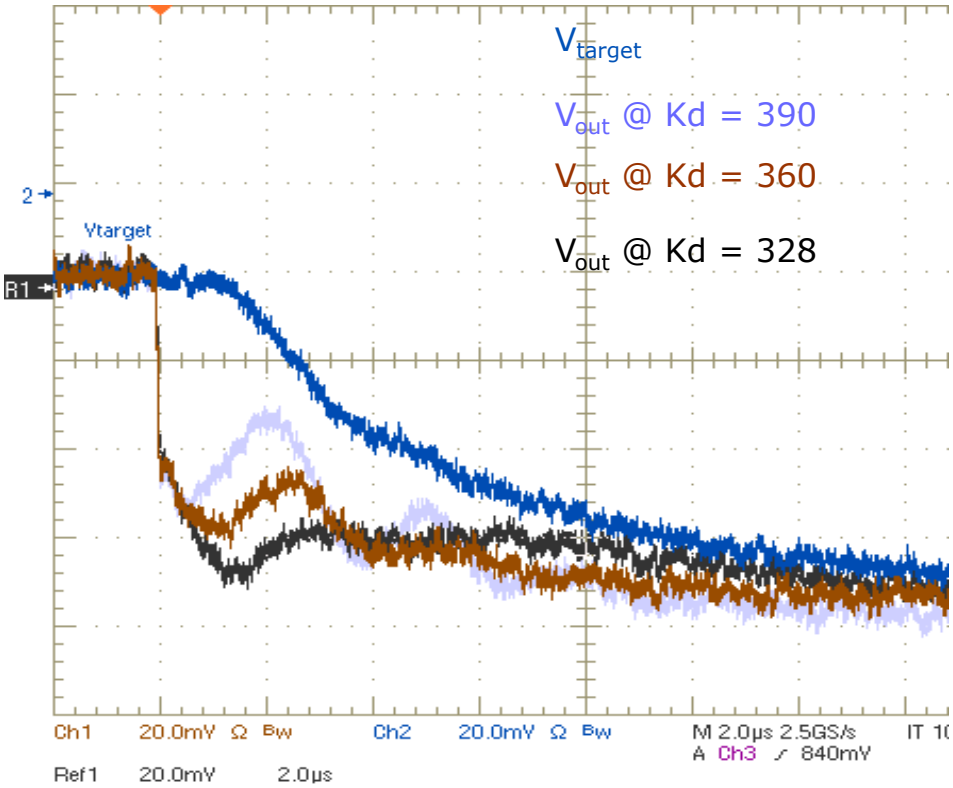


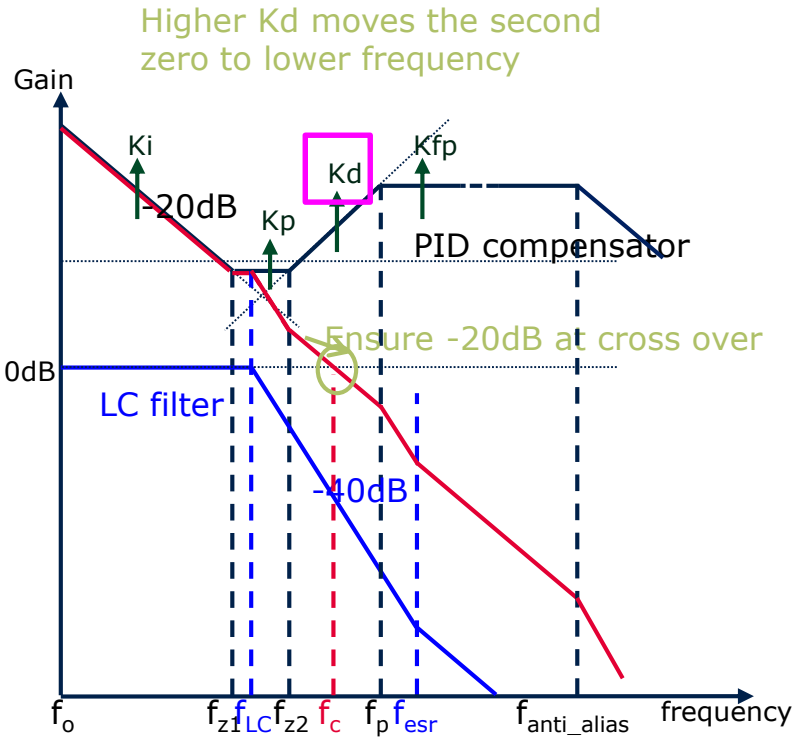


- I is the integral term used to drive the DC value of Verr to zero
- From the time domain transient response, **Ki** mainly affects:
  - The settling trend of V_{OUT} after the initial transient response
  - If **Ki** is too high, V_{OUT} overshoots V_{target} in the highlighted region
  - If **Ki** is too low, V_{OUT} may lag V_{target} in the highlighted region can cause extra undershoot

Note: **Ki** affects the transient response after the initial 10us to 40us

Feedback Loop PID: Steady State Voltage Loop Compensation Kd impact on transient

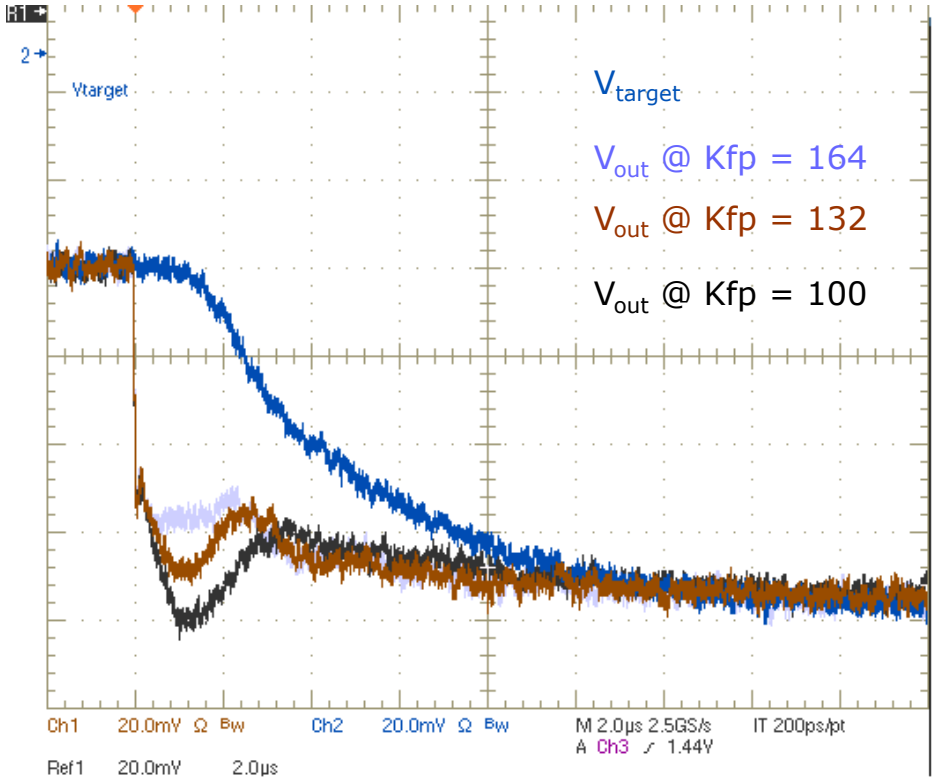


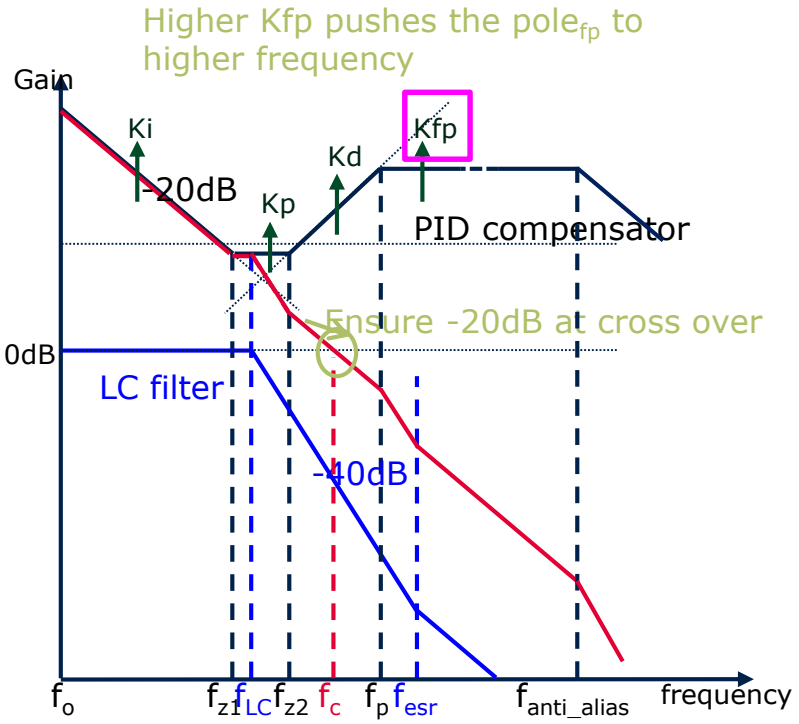


- D is the derivative term. The higher the Kd, the higher the BW but with less phase margin
- From the time domain transient response, **Kd** mainly affects:
  - The first undershoot beyond the 100ns of load stepping. The higher the **Kd**, the less the undershoot
  - But too high of **Kd** will cause V_{OUT} ringing due to insufficient phase margin

Note: **Kd** affects the transient response within the first 5us

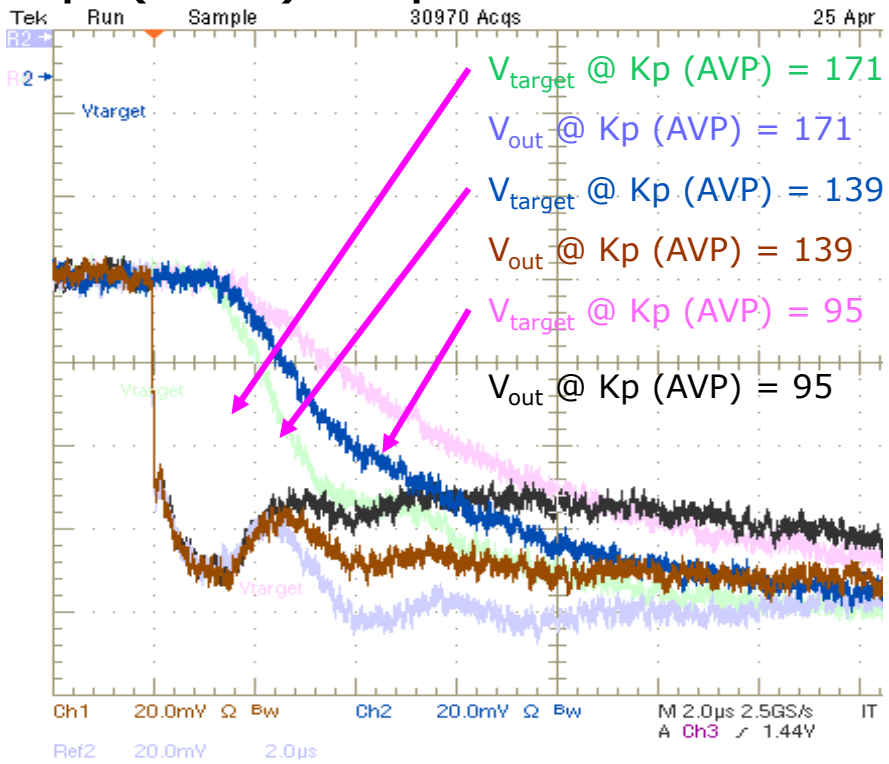
Feedback Loop PID: Steady State Voltage Loop Compensation Kfp impact on transient





- **Kfp** provides a high frequency pole to roll off the gain introduced by the P and D terms. If **Kfp** is too high, the D term gain at high frequency will not be attenuated and hence results in less phase margin
- From the time domain transient response, **Kfp** mainly affects:
  - The first undershoot beyond the 100ns of load stepping. The higher the **Kfp**, the less the undershoot
  - But if **Kfp** is too high it will lead to V_{OUT} ringing due to insufficient phase margin

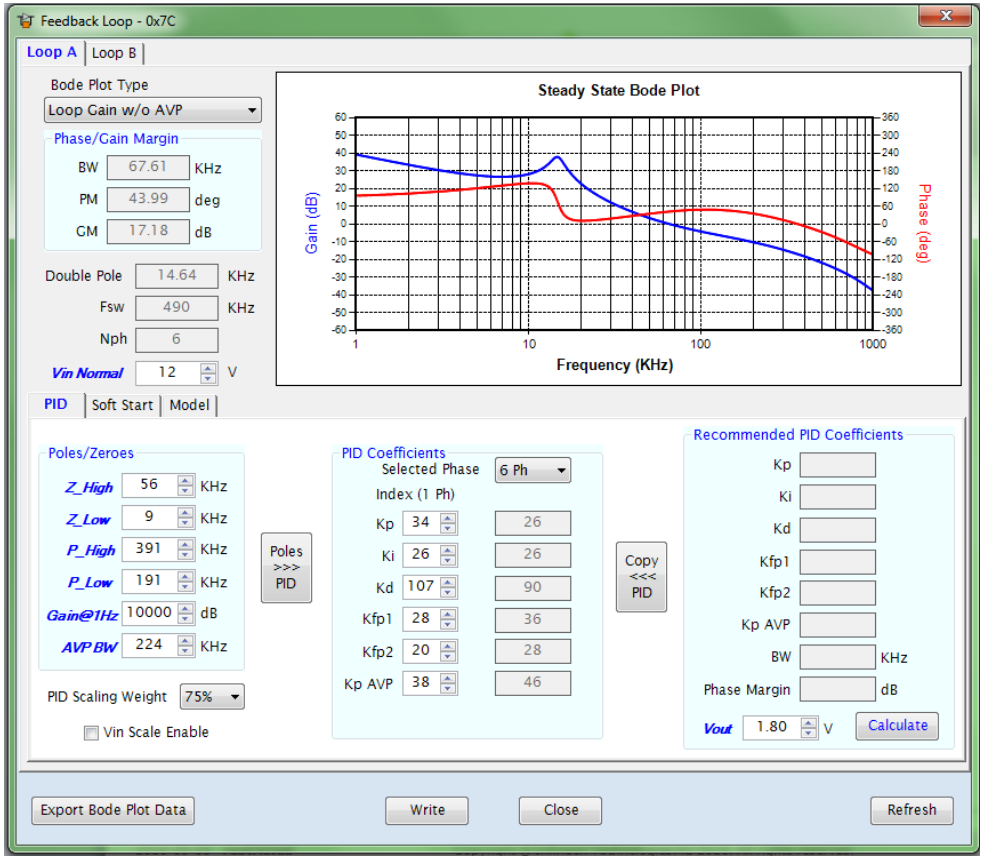
Feedback Loop PID: Steady State Voltage Loop Compensation Kp (AVP) impact on transient

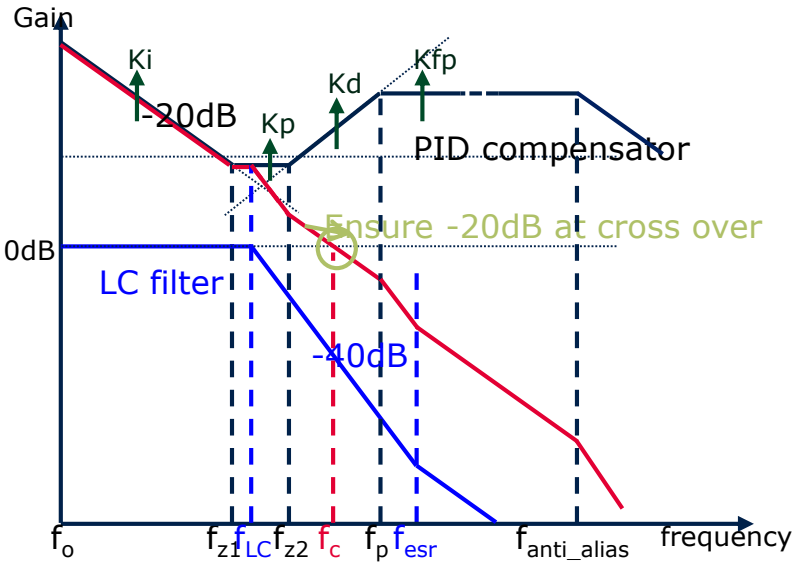


- **Kp(AVP)** is the low pass filter of the AVP loop.
- From the time domain transient response, **Kp(AVP)** mainly affects:
  - how fast the target voltage can track the changing inductor current during transient conditions
  - If **Kp(AVP)** is too low, V_{OUT} will take longer to settle to the final DC target
  - The higher the **Kp(AVP)** , the higher the AVP loop BW, and it may overlap with the voltage loop to induce extra undershoot or ringing at V_{OUT}

Note: **Kp(AVP)** affects the transient response in 5us to 20us

Feedback Loop PID: Compensator – Steady State (Voltage Loop)





Poles/Zeroes

- **Z1**: first zero at f_{Z1}
- **Z2**: Second zero at f_{Z2}
- **P_Low**: pole at fp
- **P_High**: pole at f_{anti_alias}
- **Gain @ 1Hz**: DC gain
- **AVP BW**: AVP bandwidth
- **Poles>>>PID button**: calculates and populates the desired PID coefficients based on Poles and Zeros information entered

Voltage Loop Compensation Procedure