PowerClient GUI User Guide

AN003-V2.0

Applications Team
April-20

IN PROGRESS BEEING UPDATED

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Purpose

- This document describes the steps and settings to create a configuration file for the XDPE122xx and XPDE142xx family of multiphase controllers.
- Both AMD, Intel, PWM-VID settings are shown. Different parts of the family support all or only a few of the settings.
- Each window in the GUI tool will be explained.
- Target audience: Design engineers with knowledge of tuning feedback loops for Intel and AMD settings.

Agenda

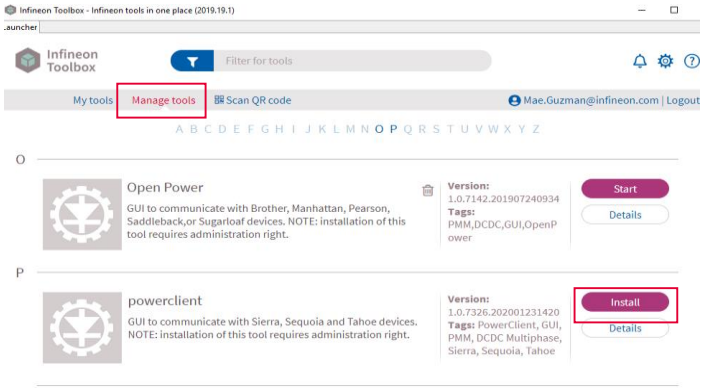
Supported Devices

Sierra B/C		Sequoia
XDPE12250	XDPE12283	XDPE14283
XDPE12254	XDPE12284	XDPE14284
	XDPE12286	XDPE14286

Agenda

Installation procedure

- Two ways to download/update the GUI
  - **Infineon Toolbox** available at http://www.infineon.com/toolbox
    - Follow the instructions listed to download and install the *Infineon Toolbox*
    - In the *Infineon Toolbox*, go to *Manage tools* and select PowerClient's *Install* or *Update* button.



  - **MyICP** (*My Infineon Collaboration Platform*)
    - Register and login to your MyICP account
    - Once logged in, go to https://myicp.infineon.com/sites/enterprise_power/

- There may be a need to install latest license file. Ask your Infineon FAE for the latest one
  - copy the license file *IR DPDC License.txt* into the installation directory

NOTE: Infineon toolbox is the fastest way to have access to the GUI as it doesn't need internal clearing of the user.

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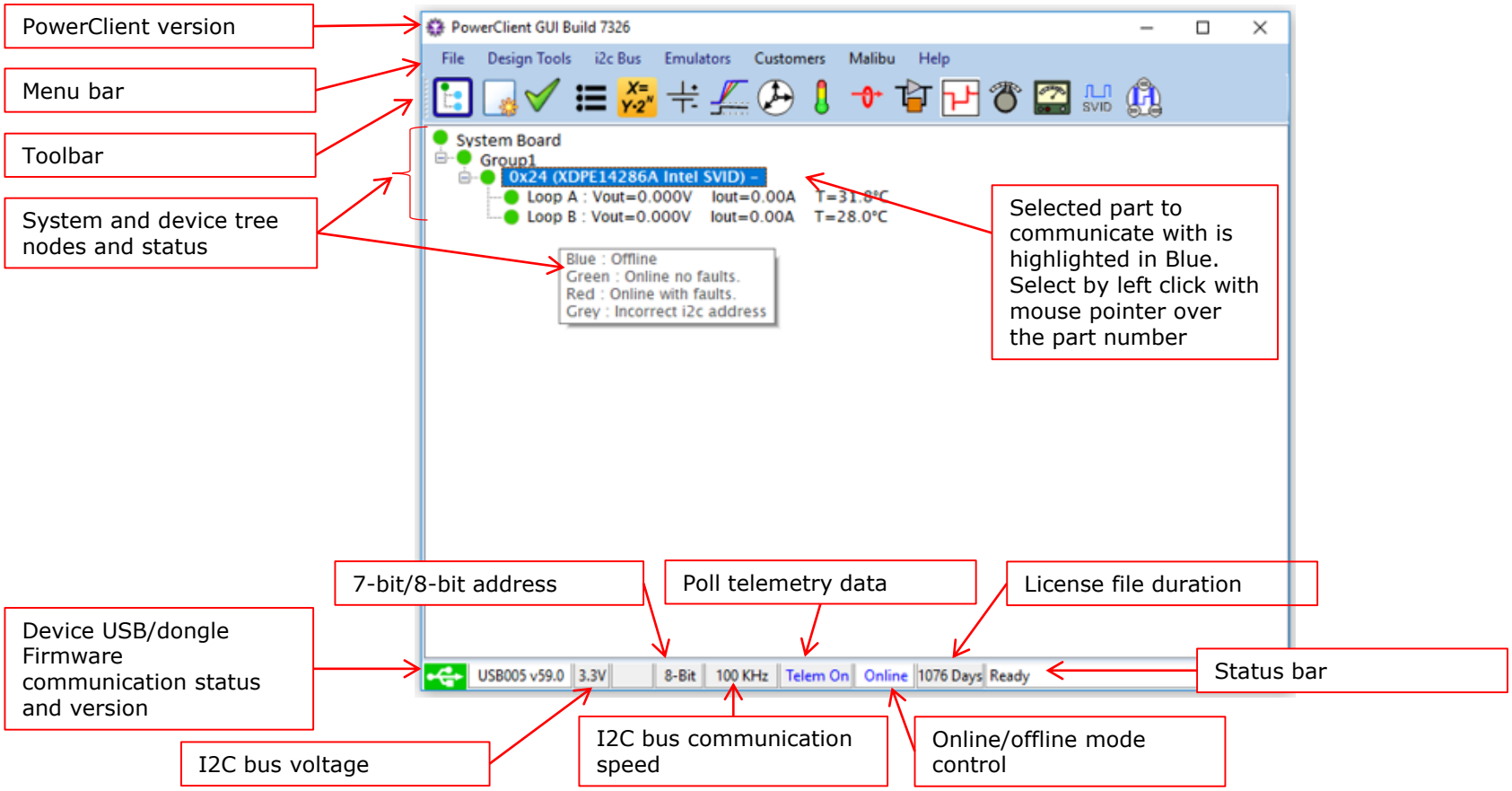
1. Purpose
2. Install GUI software
3. Main GUI window
4. General error messages and warnings
5. Start to create a configuration file
6. Phase & frequency
7. Input settings
8. Output settings

Main GUI window

› PowerClient main dialog displays and consists of GUI version, menu bar, toolbar, system and device tree nodes and status, USB/dongle Firmware communication status and version, I2C bus voltage, 7-bit8-bit address display, I2C bus communication speed, poll telemetry data status, online/offline status, GUI license file duration and status bar.

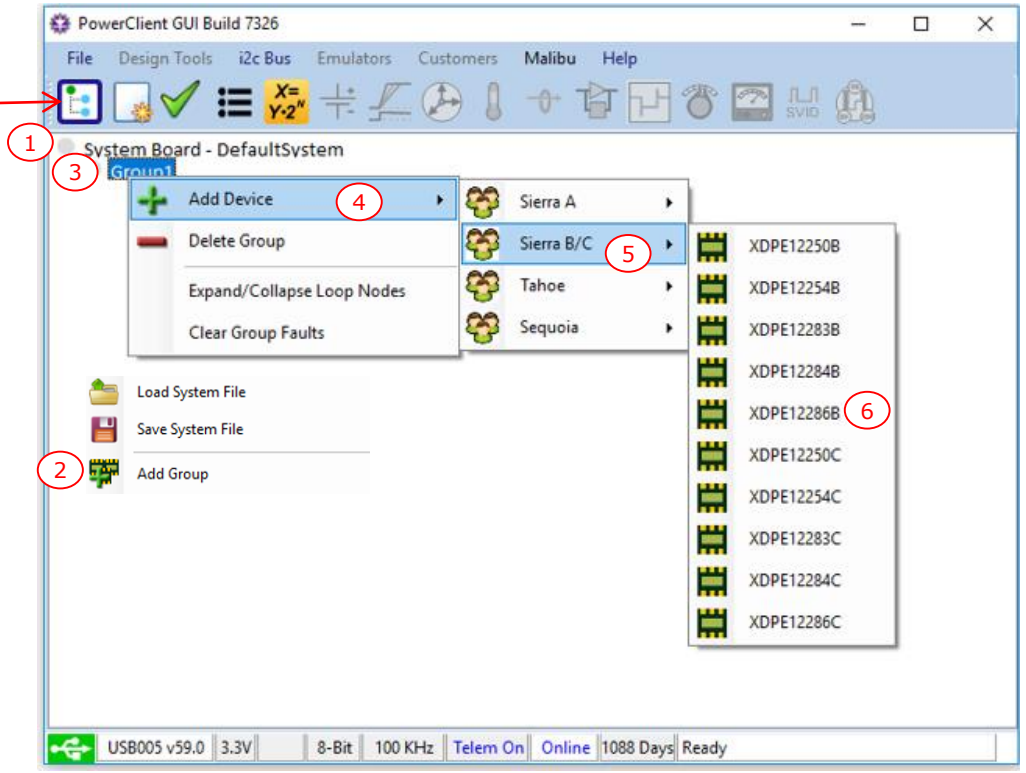


Main GUI window: Starting the GUI

- When you first launch the GUI after installation, it will have an empty System Board window.
- Adding parts can be done automatically or manually.

Automatic (Auto Populate Devices)
- in online mode, it will automatically scan and display all connected Infineon supported devices

Manual selection
1) Right click on the ***System Board Default System***
2) Select ***Add Group***
3) Right click on the ***Group1***
4) Select ***Add Device***
5) Select ***Sierra B/C*** (XDPE122xx) or ***Sequoia*** (XPDE142xx)
6) Select desired part number



- The GUI will use the last system tree node setup as a default in the next GUI launched.
- If the USB dongle is connected, it will try to sync available devices listed in the main GUI window.

Main GUI window: Menu bar (File)

Load System File...
- loads the whole system and device register configuration data

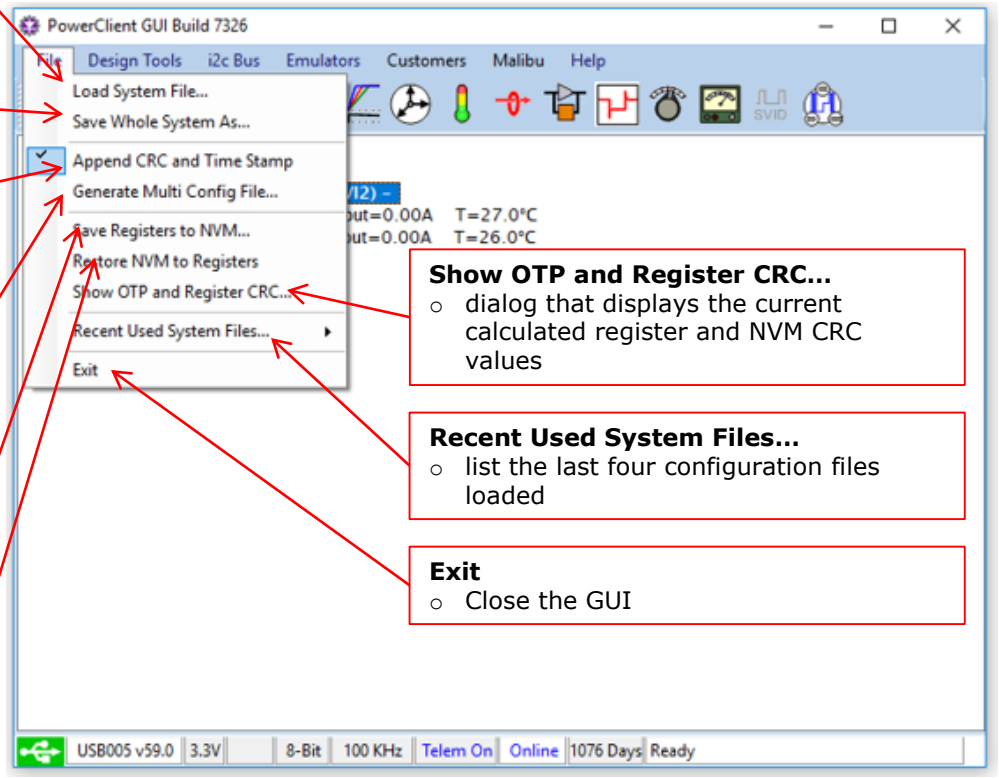
Save Whole System As...
- saves the whole system and device configuration data

Append CRC and Time Stamp
- if checked, it appends the CRC and time stamp to the file name when a configuration file is saved

Generate Multi-Config File...
- generates a multi-config file to simplify the need or ordering/keeping track of devices with different configuration files

Save Registers to NVM...
- dialog that will allow the user to perform a NVM upload

Restore NVM to Registers
- Dialog that will allow the user to perform a NVM upload



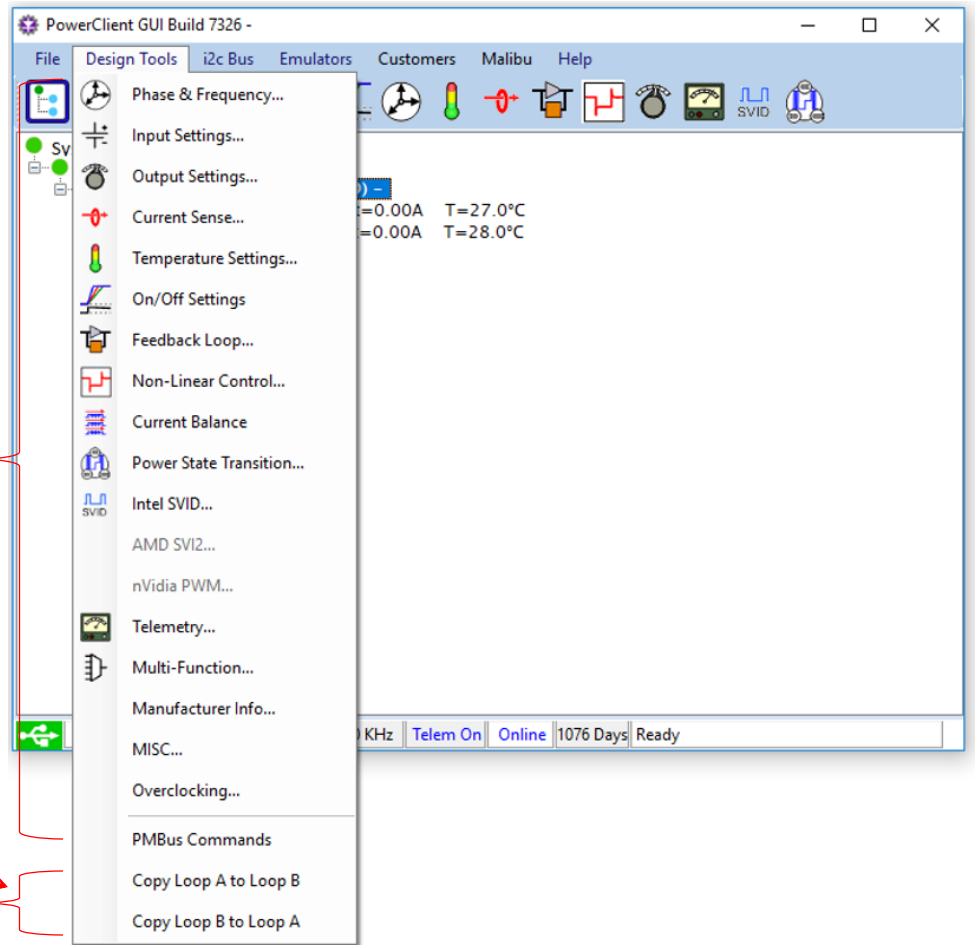
Show OTP and Register CRC...
- dialog that displays the current calculated register and NVM CRC values

Recent Used System Files...
- list the last four configuration files loaded

Exit
- Close the GUI

Main GUI window: Menu bar (Design Tools)

› Design tools contain all the tools and utilities needed to configure the device.



Please see each dialog specific section for a detailed information about these selections

Copy Loop A/B to LoopB/A
- copies LoopA/B register values to LoopB/A
- LoopA and LoopB must have the same number of phases to enable this feature

NOTE: User must have selected a part in Device Node (blue highlighted background) to be able to select any design tool.

Main GUI window: Toolbar

› Toolbar provides shortcuts of the most frequently use basic operations and control dialogs.

Auto Populate Devices
- in online mode, it will automatically scan and display all connected Infineon supported devices

New Design
- clears the current system tree nodes to start a new design

Configuration Comparator
- compares and generates a report that displays differences between two configuration files

Configuration Summary
- generates a report about the configuration file selected

Linear Format Calculator
- Calculates equivalent voltage value based on the linear format value

Input Settings

On/Off Settings

Phases & Frequency

Temperature Settings

Current Sense

Feedback Loop

Non-Linear Control

Voltage Settings

Telemetry

SVID

Power State Transition

NOTE: Some controls are disabled unless the device node (part at specific address)is selected.

Main GUI window: System tree nodes

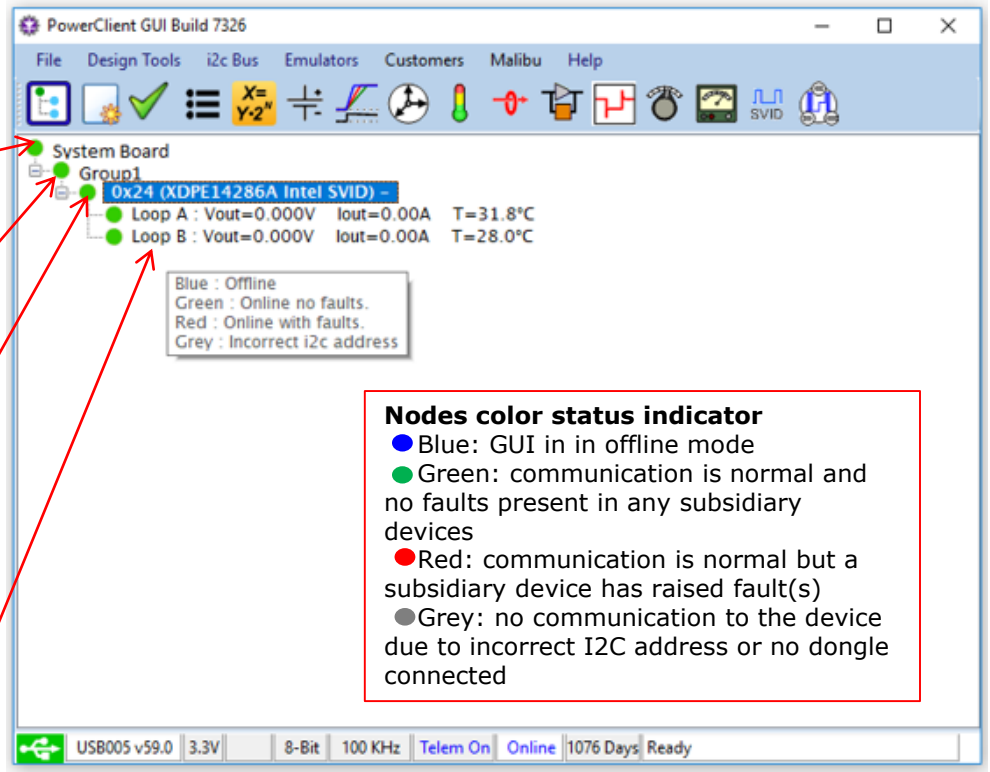
› System tree nodes list all the devices in the system and how they are arranged into groups.

System node
- root node that represents the entire system board
- user can add group(s), save and load board design, or do other board-level functions by right clicking on the node

Group node
- group of devices that may contain single or multiple devices
- user can add device(s), delete group, or do other group-level functions by right clicking on the node

Device node
- individual device that specifies device slave address, part number and operational mode
- user can load and save specific device configuration file, delete device, or do other device-level functions by right clicking on the node

Loop node
- displays device's output voltage, output current and temperature per loop



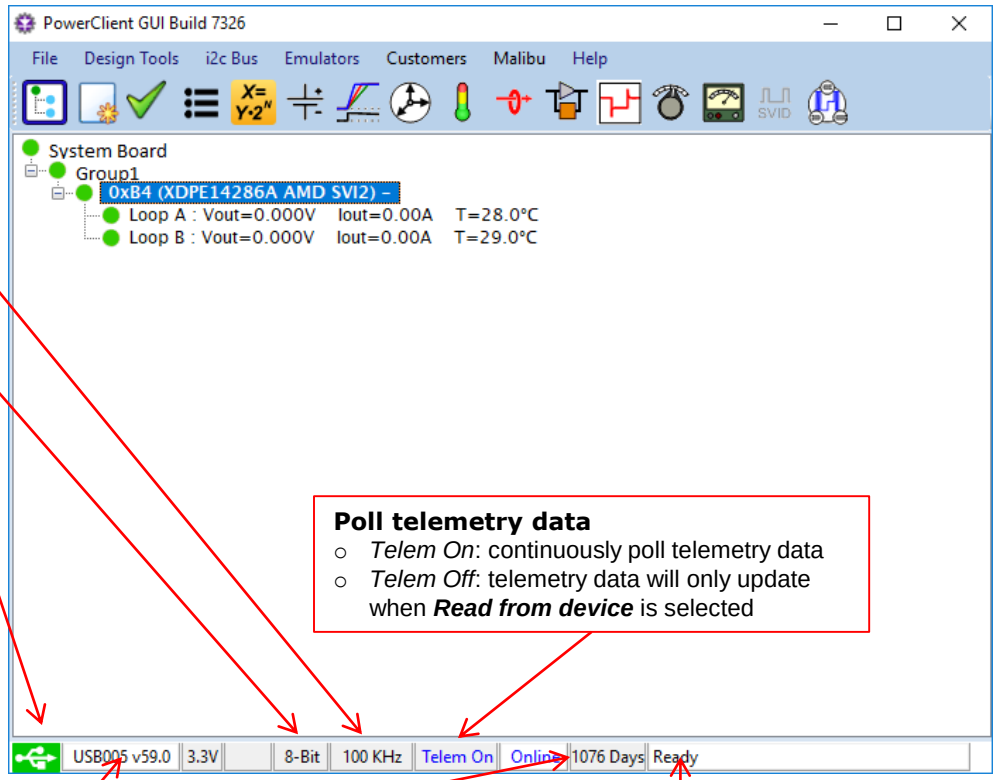
Main GUI window: Communication and license

I2C bus communication speed
- base speed is 100KHz
- can be change in the ***i2c Bus → i2c Address Scanner***
- ensure that the target device(s) show up in the list to verify that the communication is stable at the selected speed after the *Scan i2c/PMBus Address* button is selected

7-bit/8-bit I2C address
- 8-bit is the base i2c address display
- can be change in the ***i2c Bus → Use 8-bit i2c Address***

USB/Dongle FW status
- Green: dongle is detected
- Red: either the dongle is not connected or the driver is not correctly installed

USB/Dongle FW version
- if the dongle is detected and communicating correctly, it will display the hardware and Firmware version.
- if the version is **v0**, there may be an issue with the driver
- user needs to update its Firmware version if a newer USB dongle firmware is available



Poll telemetry data
- *Telem On*: continuously poll telemetry data
- *Telem Off*: telemetry data will only update when ***Read from device*** is selected

License file duration
- list remaining days before the GUI license will expire
- Contact your Infineon FAE

Status bar
- Displays if the current communication status between the GUI and the device

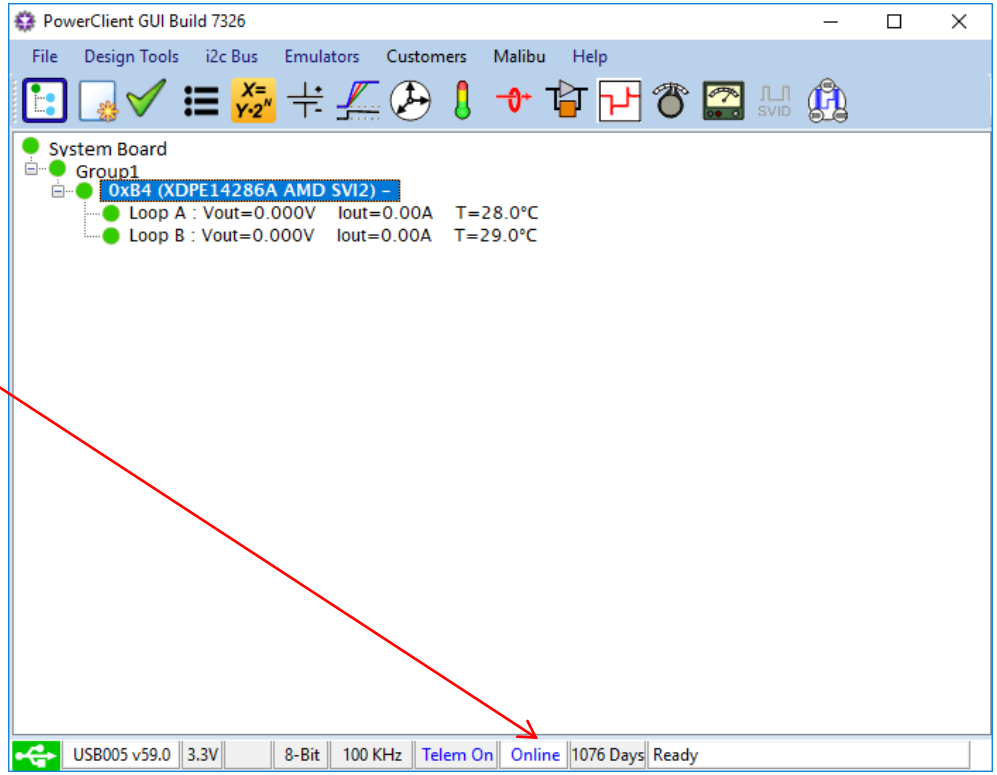
Main GUI window: Online/offline mode control

Online mode

- GUI will attempt to communicate to the device
- If device is detected, user can
  - modify contents of the device
  - load contents of a configuration file into the device
  - Save contents of the devices' registers into NVM
  - Restore NVM contents into the registers
  - Poll telemetry data
- If device cannot be detected
  - Write and read from the device will be disabled

Offline mode

- Write to internal cache register only and not to the device, regardless of the connection status
- Can be use as a system file editor or a system file viewer



Agenda

General errors, warnings and reminders

- When a change is made in a dialog
  - **Write to device** button will change to **Write to device*** to indicate that changes have been made to the dialog.
    - **Write to device*** needs to be selected to commit the changes.

  - In online mode, all changes made will be written into the device.
  - In offline mode, all changes made will be written to the internal cache register only and not to the device.

- Error checking to make sure no design rule is violated
  - Error: red indicator flags an error
    - An example is a value entered it out of range.
    - Write button is disabled when error(s) is present.
    - Tabbed dialog name will also turn red when error is active to show which tabbed dialog has the error.
  - Warning: yellow indicator flags a warning
    - A warning means the input value may cause non-optimal performance.
    - Warnings do not prevent the GUI from committing changes to the device.
  - Hovering the cursor over the error sign will display explanation of the warning.

- **Blue** dialog fieldnames
  - It indicates that there is no register associated with it.
  - Values are only save as a system configuration data.
  - It is only use for simulation and/or calculation.

- Disabled or greyed out dialog fields
  - It is for information only and maybe a calculated data from another window.
  - It can also be enabled/disabled depending on the part number.

NOTE: Data must be entered and written one dialog at a time. If data is being modified on two or more dialogs, pressing the **Write to device** button will only write data on the current dialog. Other change(s) data made on the other dialog(s) will be gone.

Often used selection

- **Write to device**
  - In online mode, all changes made will be written into the device.
  - In offline mode, all changes made will be written to the internal cache register only and not to the device.
- **Read from device**
  - In online mode, it will restore and refresh dialog field values based on its current associated register value.
  - In offline mode, it will restore and refresh dialog field values based on its associated internal cache register value.
- **Close**
  - Close the window
- **Help**
  - Open up the GUI user guide

- **Shutdown Response** / **Response**
  - ***Ignore***: fault is ignored
  - ***Latch***: Shuts down the HS and LS FETs
  - ***Hiccup***: Shuts down HS and LS FETs and controller will attempt to restart the system in hiccup manner

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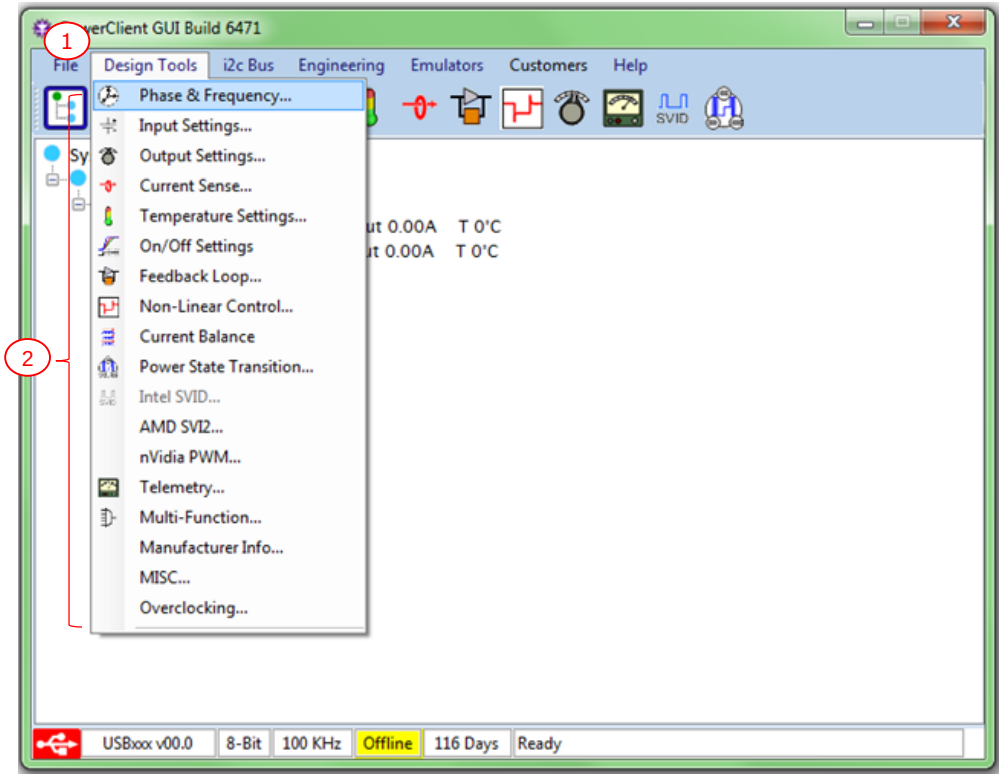
Steps to create a start-up configuration file

- Easiest is to start by using an existing approved config file and modify the parameters that differ.
  - Ask your Infineon FAE for a reference config file.
- If no existing approved config file is available, user can manually create one.

1) Select Design Tools menu
2) Open each listed selections
- Open each dialog and set all the register settings desired.



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Phase & Frequency

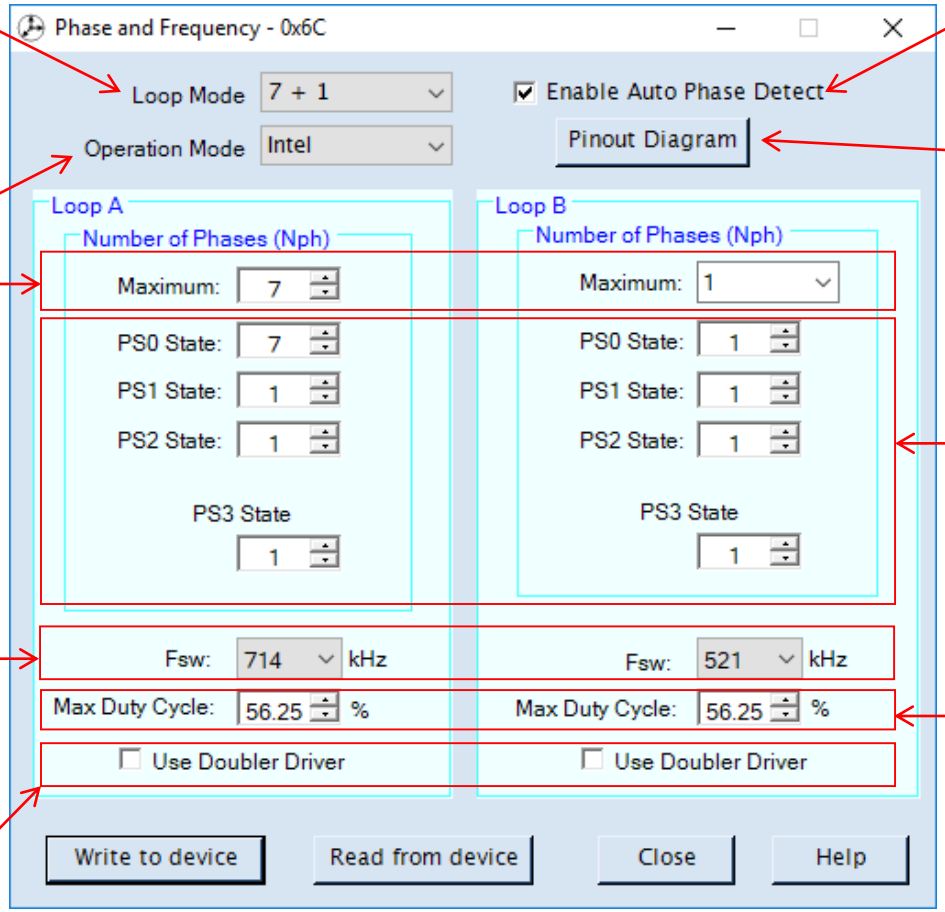
Loop Mode
- maximum number of phases supported
- depending on which part number, there will be more or less combinations to select from

Operation Mode
- type of application
- POL/telecom is intended for ASIC and FPGA loads that does not follow Intel standards

Maximum (Nph)
- number of phases populated for the respective loop
- value mostly depends on the full load current rating of the application and current capability per phase
- the controller uses the Nph value to set the internal phase timing relationship for the loop
- for normal applications, **Maximum = PS0 State**

Fsw
- switching frequency
- depending on NPH in a loop, available frequencies may differ slightly due to internal division ratios

Use Doubler Driver
- enable to use 2 power stages per phase in doubler configuration. Causes the PWM frequency at the PWM pin to double as the driver will divide the PWM again.



Enable Auto Phase Detect
- automatic detection of number of mounted phases on a board
- recommended to always have box marked

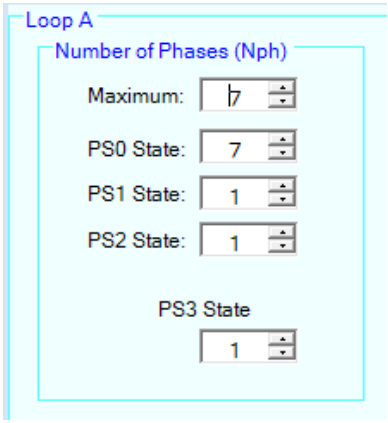
Pinout Diagram
- displays pinout diagram of the device

- **PSx State**
- number of phases enabled during specific power states
- Should be set based on load current requirement for the system and current capability per phase. This is usually limited by the power device used.
- ***Maximum*>=*PS0*>=*PS1*>=*PS2*>=*PS3***
- For normal applications, ***PS0 State* = *Maximum***
- if not used, set all **PSx State** = ***Maximum*** phases
- typically used for Intel applications
- for AMD, see note on next page

Max Duty Cycle
- Maximum duty cycle allowed for PWM signal
- calculate for minimum Vin and Max Vout operation
- May need to be higher (50% or more often used) to allow for transient condition during steps in load

Phase & Frequency

- For AMD, the power states translate to
  - PS0 State=normal operation
  - PS1 State=PSI0_L
  - PS2 State=PSI1_L
  - PS3 State= Not Used (set to same as PS2)



Note: GUI does not change the text for different modes like AMD. It always uses the Intel names.

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Input Settings… Vin Sense

Vin Sense Type
- Vin Sense method that can be modified in the **Iin Sense/Input Power** tab

Vin Source
- *Measured*: Vin telemetry will be based on the sense result on the Vin sense pin
- *Vin Fixed*: Vin telemetry will be a fixed value entered in the **Vin Fixed** dialog field

Vin Sense Network:

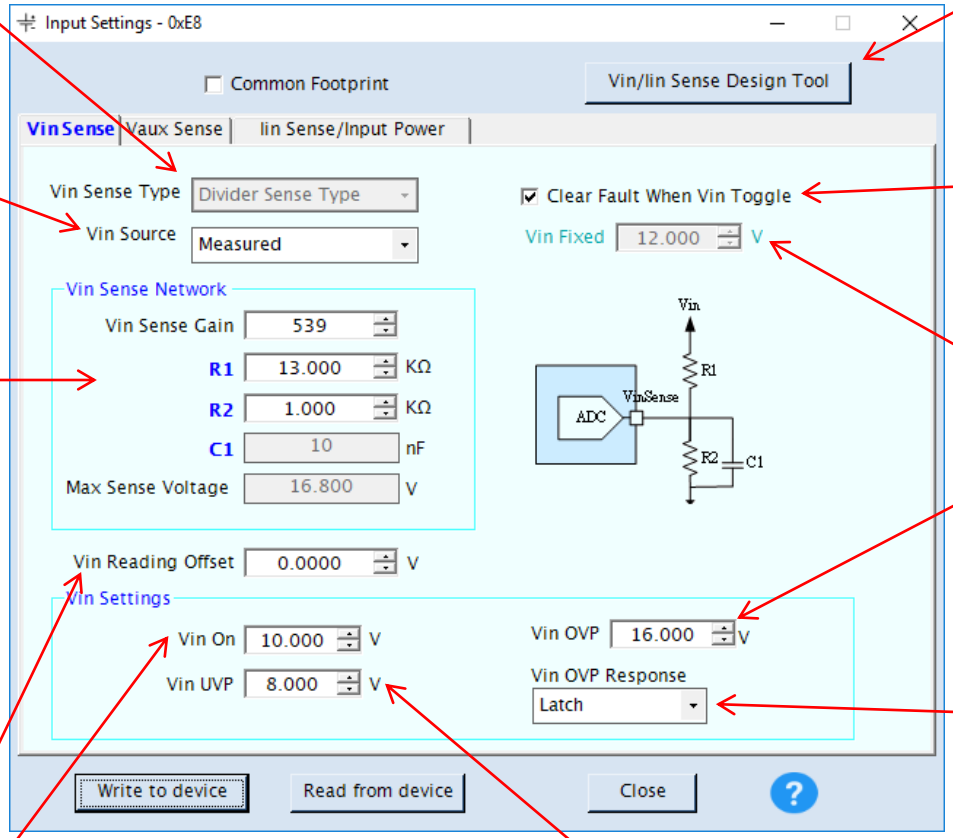
When Vin is set to *measured,* an external resistor divider is needed.

Vin Sense Gain
- gain factor and will depend on the resistor divider resistance

R1, R2
- Typical values are 19.1kΩ/1.54kΩ or 13kΩ/1kΩ

Max Sense Voltage
- Default should be ~16V for a 12V nominal VIN application
- Value depends on the resistor divider resistance

Vin Reading Offset
- Used to compensate for offset error in the VIN sense for a more accurate VIN telemetry



Vin On
- Voltage level on when will Vout regulation start

Vin UVP (Undervoltage protection)
- Voltage level on when to turn off Vout

Vi/Iin Sense Design Tool
- Opens the **Input Sense Design Tool** that helps calculate settings

Clear Fault When Vin Toggle
- *Checked*: Vin toggle (Vin go away and comes back) can reset fault conditions just like the action of toggling VR_EN can reset fault conditions
- *Unchecked*: only toggling VR_EN can reset fault conditions

Vin Fixed
- Vin telemetry value when **Vin Source** is set to *Vin Fixed*

Vin OVP (overvoltage protection)
- Voltage level on when the regulator stop switching to protect power stages and load
- Maximum value is based on the "Max Sense Voltage" value

Vin OVP Response
- *Ignore*: Vin OVP fault is ignored
- *Latch:* Shuts down HS and LS FETs * enable pin or Vin need to be toggled to restart
- *Hiccup:* Shuts down HS and LS FETs and will automatic retry once fault is gone

Input Settings... Vaux Sense

Vaux Enabled for
- Options to enable it in LoopA, LoopB and both LoopA/B
- If this function is not used, set it to disabled

Vaux Source
- pin to be used to sense the Vaux voltage

Vaux Sense Network

Vaux Sense Gain
- Gain factor to get correct voltage reading
- Typical value is 515 but depends on the resistors and board layout

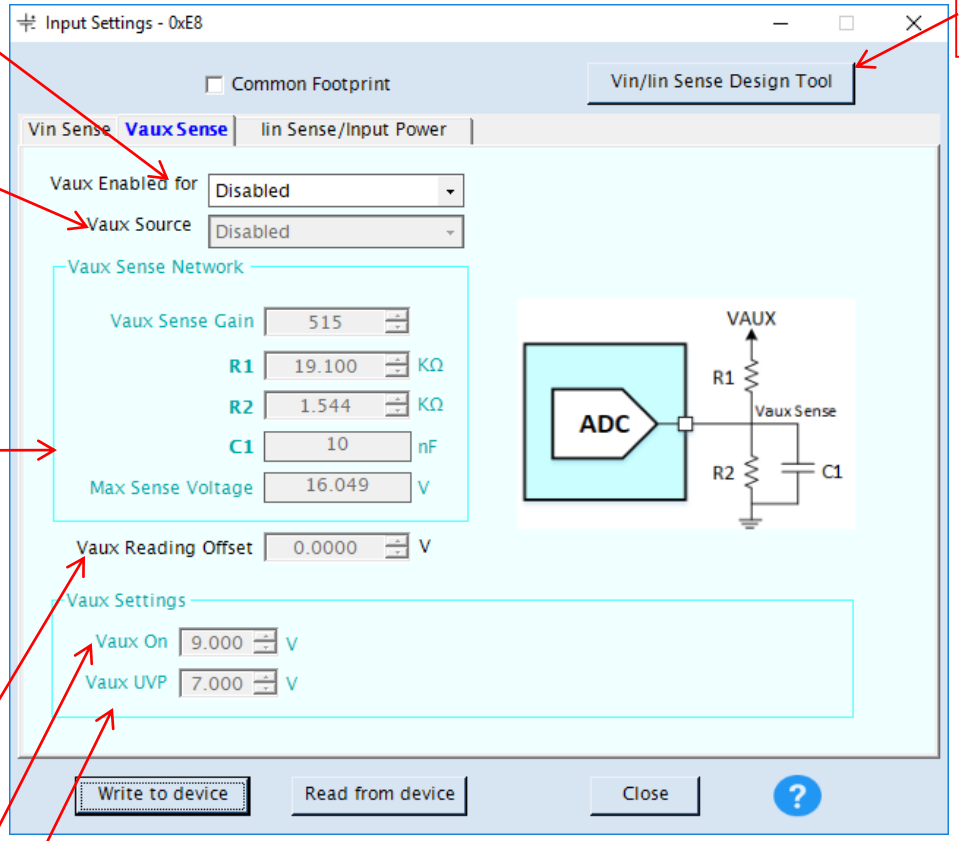
R1, R2
- Typical values are 19.1kΩ/1.54kΩ

Max Sense Voltage
- Default should be ~16V for a 12V nominal VIN application
- Value depends on the resistor divider resistance

Vaux Reading Offset
- Used to compensate for offset error in the Vaux sense for a more accurate Vaux telemetry

Vaux On
- Voltage level on when will Vout regulation start assuming Vin also is above its threshold

Vaux UVP
- Voltage level on when to turn off Vout



Vi/Iin Sense Design Tool
- Opens the **Input Sense Design Tool** that helps calculate settings

Input settings... Iin Sense/Input Power

Common Footprint

(XDPE14284 device only)

- When selected,
  - pin36: dedicated for Isys
  - pin37 dedicated for Vsys
  - pin38: Vin
  - Enables *Vsys Sense* tabbed dialog

Source

- Selection of how input current is measured
- Disabled, Calculated, PI Sense,...
- Selection list is based on the selected part numbers.

Iin Estimate Settings

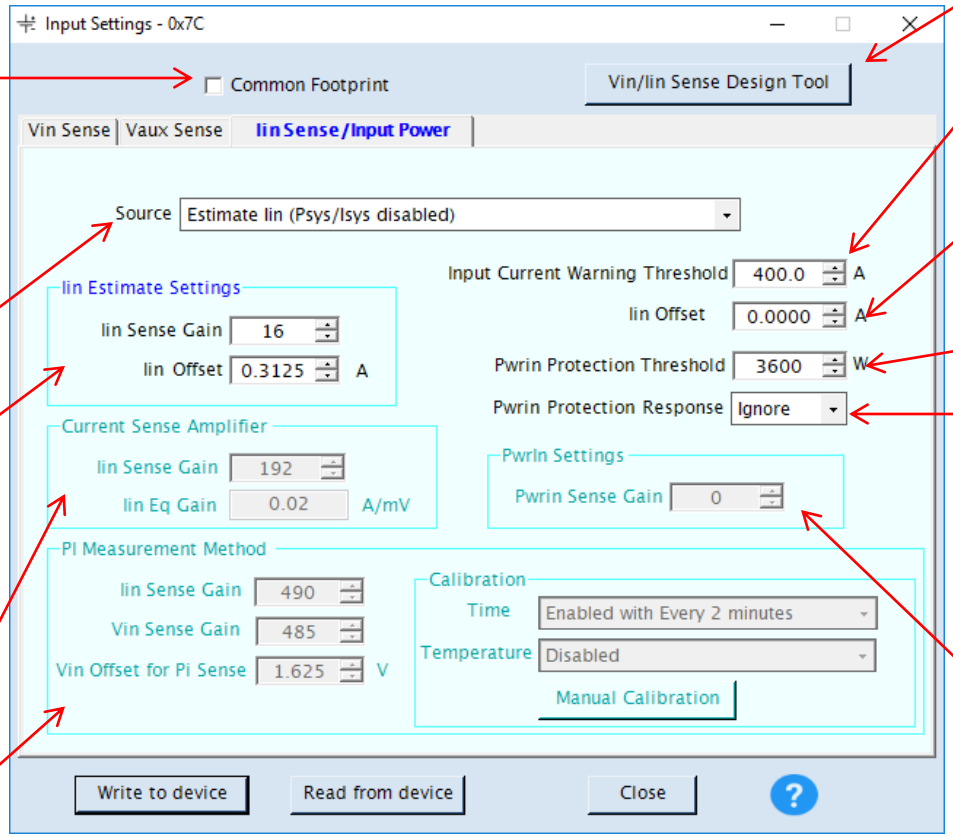
- Calculates the input power that depends on real efficiency, Iout, Vin, duty cycle and losses.
- Values should be changed to make reported Iin match the external measured Iin.

Current Sense Amplifier

- Gain adjustments for the sensed signal when **Source** selected is set to *be Iin Sense Amplifier*.

PI Measurement Method

- Gain adjustments for the sensed signal when **Source** selected is set to *be PI Sense*.
- **Calibration**: sets the calibration cycle and can compensate temperature drift and more.



Vi/Iin Sense Design Tool

- Opens the **Input Sense Design Tool** that helps calculate settings

Input Current Warning Threshold

- Input current threshold when warning happen

Iin Offset

- Compensate any offset error in the Iin sense for a more accurate Iin telemetry

PwrIn Protection Threshold

- Power level when input power protection will trigger

PwrIn Protection Response

- *Ignore*: PwrIn protection fault is ignored
- *Latch:* Shuts down HS and LS FETs
- *Hiccup:* Shuts down HS and LS FETs and will automatic retry once fault is gone

PwrIn Settings

- Gain adjustment when **Source** selected is PwrIn Sense.

Input settings... Vsys Sense (XDPE14284 only)

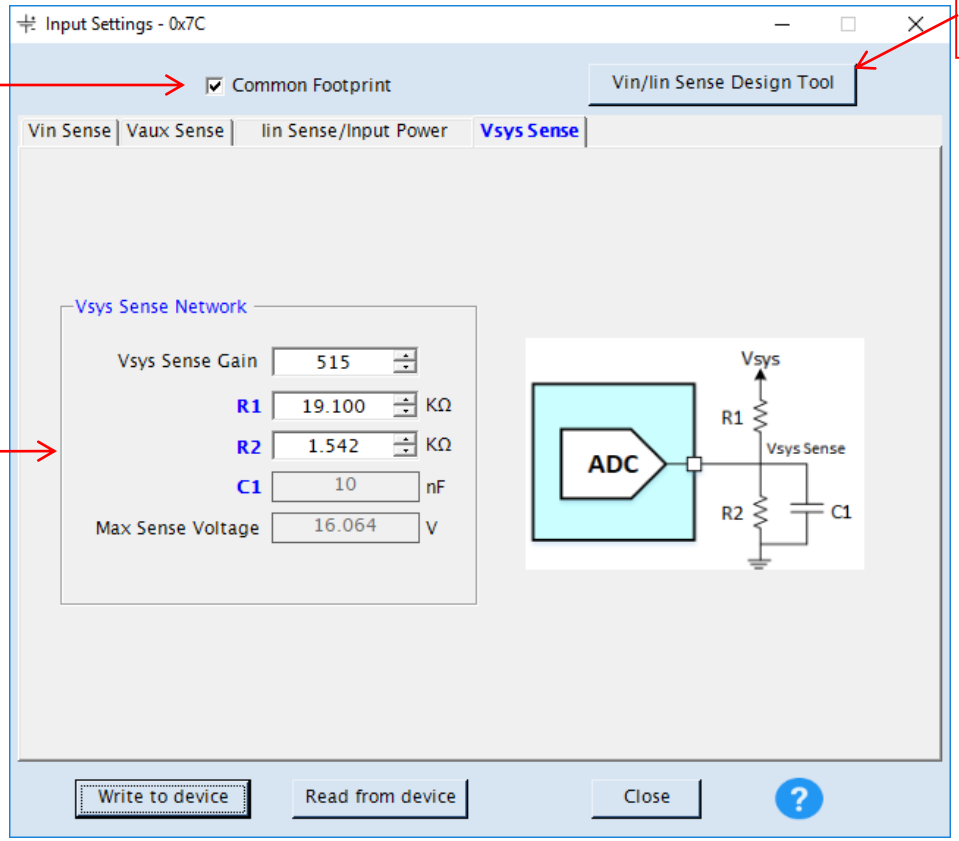
Common Footprint
(XDPE14284 device only)
- When selected,
  - pin36: dedicated for Isys
  - pin37 dedicated for Vsys
  - pin38: Vin
  - Enable *Vsys Sense* tabbed dialog

Vsys Sense Network

Vsys Sense Gain
- Gain factor to get correct voltage reading
- Typical value is 515 but depends on the resistors and board layout

R1, R2
- Typical values are 19.1kΩ/1.54kΩ

Max Sense Voltage
- Default should be ~16V for a 12V nominal VIN application
- Value depends on the resistor divider resistance



Vi/Iin Sense Design Tool
- Opens the **Input Sense Design Tool** that helps calculate settings

Note: This tabbed dialogue is only visible on a XDPE14284 device and when **Common Footprint** is selected.

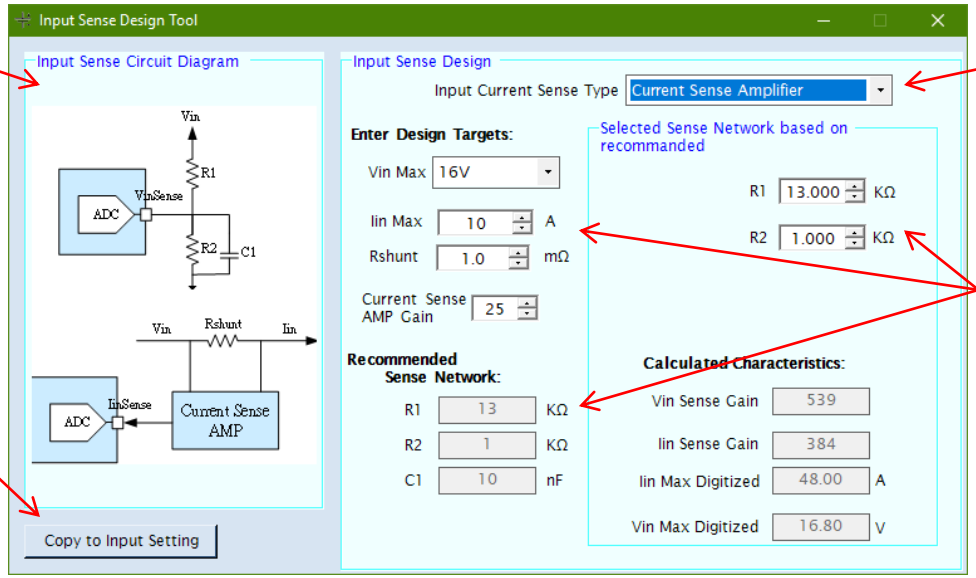
Input settings… Input Sense Design Tool

Input Sense Circuit Diagram

- External components for the different sense schemes.

Copy to Input Setting

- Copies calculated values and settings in the *Input Settings/Vin Sense* tabbed dialog.



Input Sense Type

- Selects which type of input current sensing will be use.

- Depending on selected configuration entered design target numbers and calculation of recommended values for the external components will be shown.
- Enter the resistor values that will be used. Typical the recomended values.

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Output Settings... Vout

- Displays **Loop A** or **Loop B** information
- 3 tabbed dialogs for each loop
- Active tab is highlighted in bold blue text font
  - Screenshot has **Loop A** and **Vout** information displayed

VID Table

- Selection of VID voltage step

Vboot

- Boot voltage

For Intel application, **VID Table** and **Vboot** can be changed in the SVID dialog

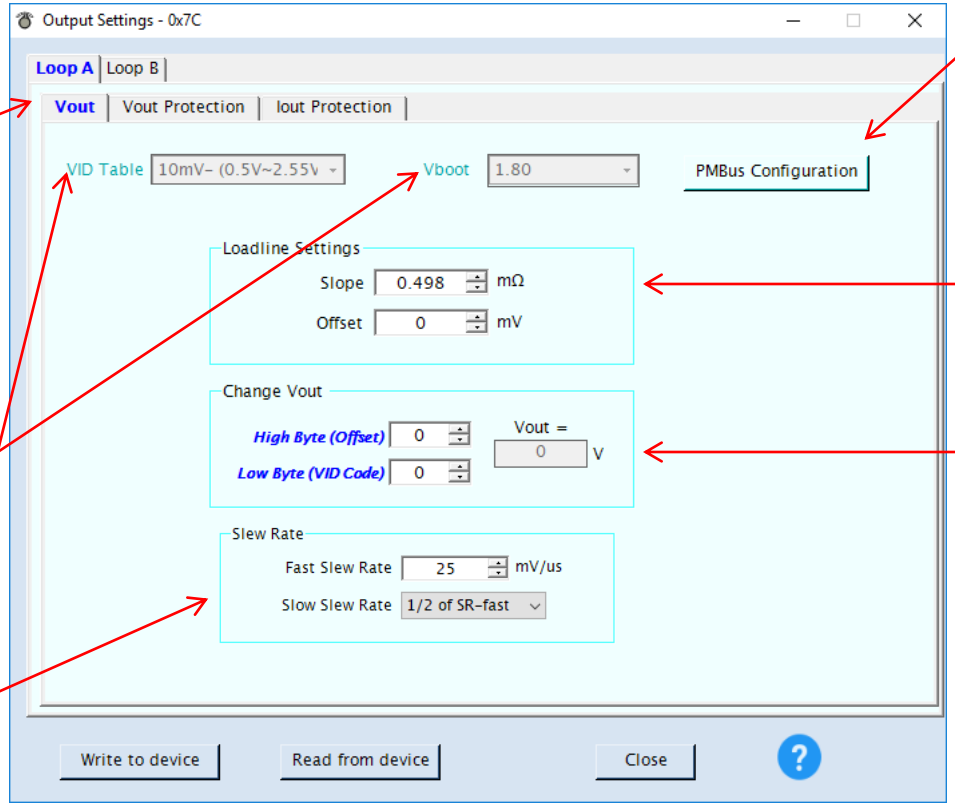
For AMD application, , **VID Table** is automatically changed to 6.25mV

For POL/Telcom or PWM-VID application, **VID Table** and **Vboot** can be change in this tabbed dialog

Slew Rate

- Rate on how fast voltage changes

For Intel application, Slew Rates can be changed in the SVID dialog



PMBus Configuration

- Opens the PMBus Configuration dialogue that is use to send PMBus commands to set Vout.

Loadline Settings

Slope

- Use to define how much Vout is adjusted by load current

Offset

- Use to position the Vout with a fixed offset over the all load currents
- Typical value is 0mV

Change Vout

- Manual control of Vout

High Byte (Offset)

- Adds an offset to existing Vout
- Values >80 count converts to a negative number

Low Byte (VID Code)

- Sets a VID code for a specific Vout
- Any settings that is not 0 will override other voltage commands

Output Settings... Vout Protection

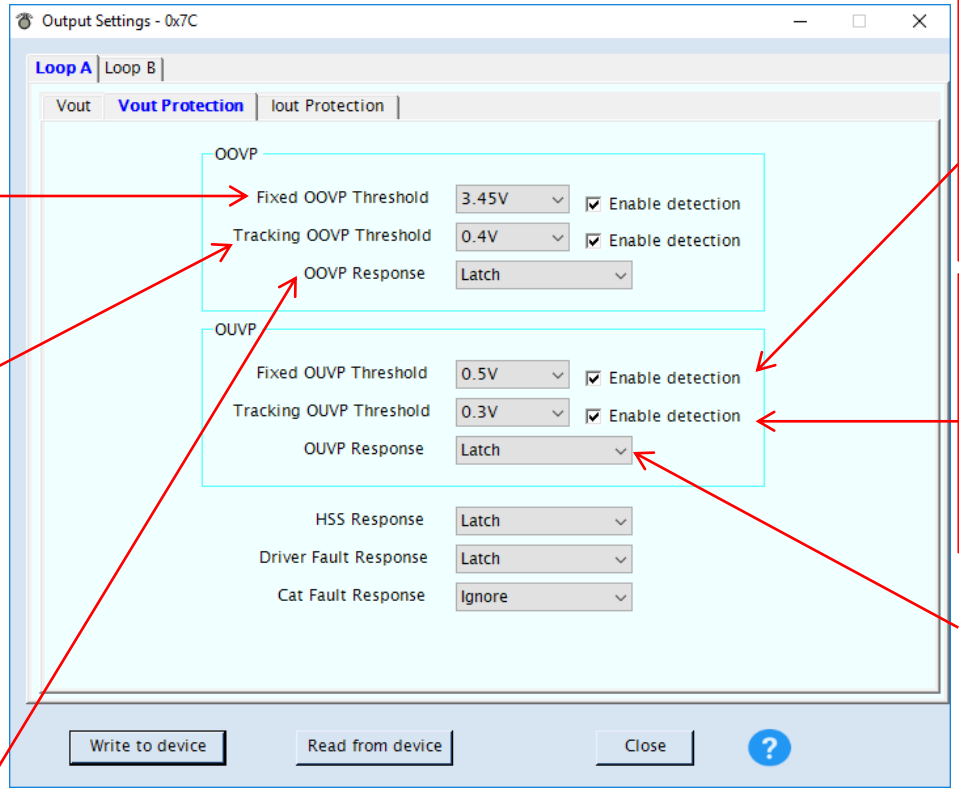
Enable detection (Fixed OOVP)
- Enable/disable Fixed OOVP Threshold detection

Fixed OOVP Threshold
- Threshold that determines if Vout is over voltage
- Triggered when Vout > Fixed OOVP Threshold
- Always active after the initialization state except during open sense line fault detection
- Recommended setting is <output cap rating and >Vout_Max

Enable detection (Tracking OOVP)
- Enable/disable tracking OOVP Threshold detection

Tracking OOVP Threshold
- Threshold is based on the difference between Vout and Vtarget.
- Triggered when (Vout – Vtarget) > Tracking OOVP threshold
- Enabled during soft start, calibration, active regulation and shutdown states
- Disabled during DVID ramping
- Recommended setting is 0.4V

OOVP Response
- Response when Vout exceeded any of the fixed or tracking OOVP threshold and when any of the OOVP enable detection is enabled
- Response time: flagged on 4 consecutive samples at a rate of 50MHz are over the threshold



Enable detection (Fixed OUVP)
- Enable/disable Fixed OUVP Threshold detection

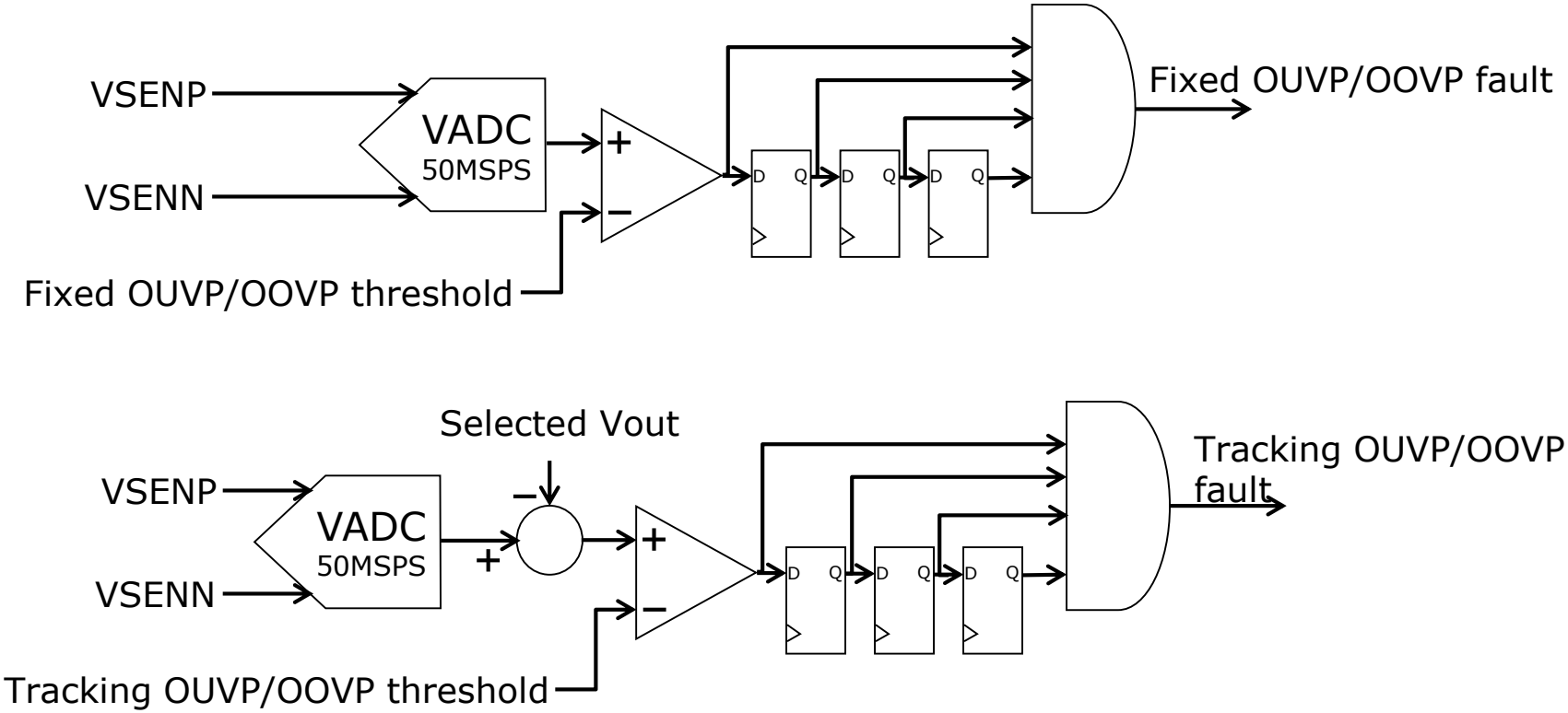
Fixed OUVP Threshold
- Output under-voltage protection
- Triggered when Vout < Fixed OUVP Threshold
- Only enabled during the active regulation state
- Recommended setting is < system required min Vout and > fixed OUVP disable threshold

Enable detection (Tracking OUVP)
- Enable/disable tracking OUVP Threshold detection

Tracking OUVP Threshold
- Triggered when (Vtarget - Vout) > Tracking OUVP threshold
- Only enabled during the active regulation state
- Recommended setting is 0.3V

OUVP Response
- Response when Vout exceeded any of the fixed or tracking OUVP threshold and when any of the OUVP enable detection is enabled
- Response time: flagged on 4 consecutive samples at a rate of 50MHz are over the threshold

Output Settings...
Fixed/Tracking OOVP/OUVP fault



4 consecutive samples over/under the limit will trigger the fault.

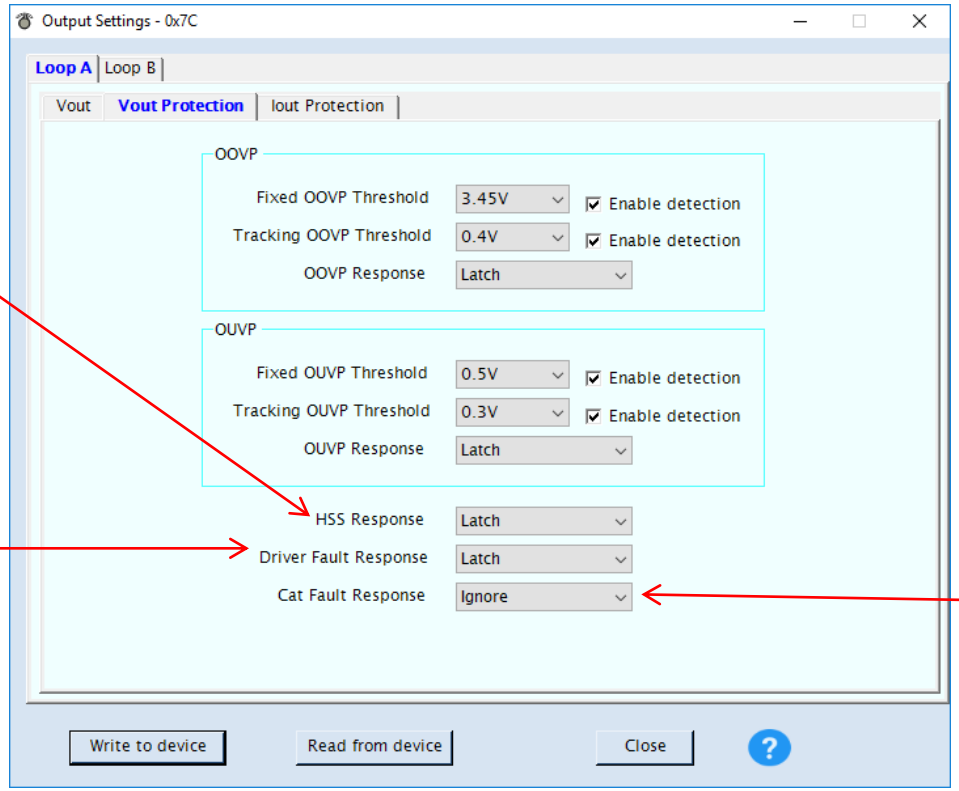
Output Settings... Vout Protection

HSS Response

- Response on high side short fault (i.e. High side MOSFET is shorted and Vout is raising by itself)
- Input: phase current sampled at 50Mhz rate
- Default threshold: 1.6 x P2CL
- Response time: 80ns; 4 consecutive samples at 50Mhz rate greater than threshold

Driver Fault Response

- Response on driver fault signal from power stages
- Input: Tmon Voltage signal
- Detection is enabled all the time
- If Tmon voltage is higher than 2V, a **Driver Fault** will be reported
- Response time:
  - Tmon have to be high for minimum 200ns before fault is flagged
  - Shutdown response at 60ns after fault is flagged



Cat Fault Response

- Response on catastrophic fault

Output Settings... Iout Protection

Note: The different thresholds for OCP and warning have an relationship and GUI may limit or round possible settings and change the other limits to match.

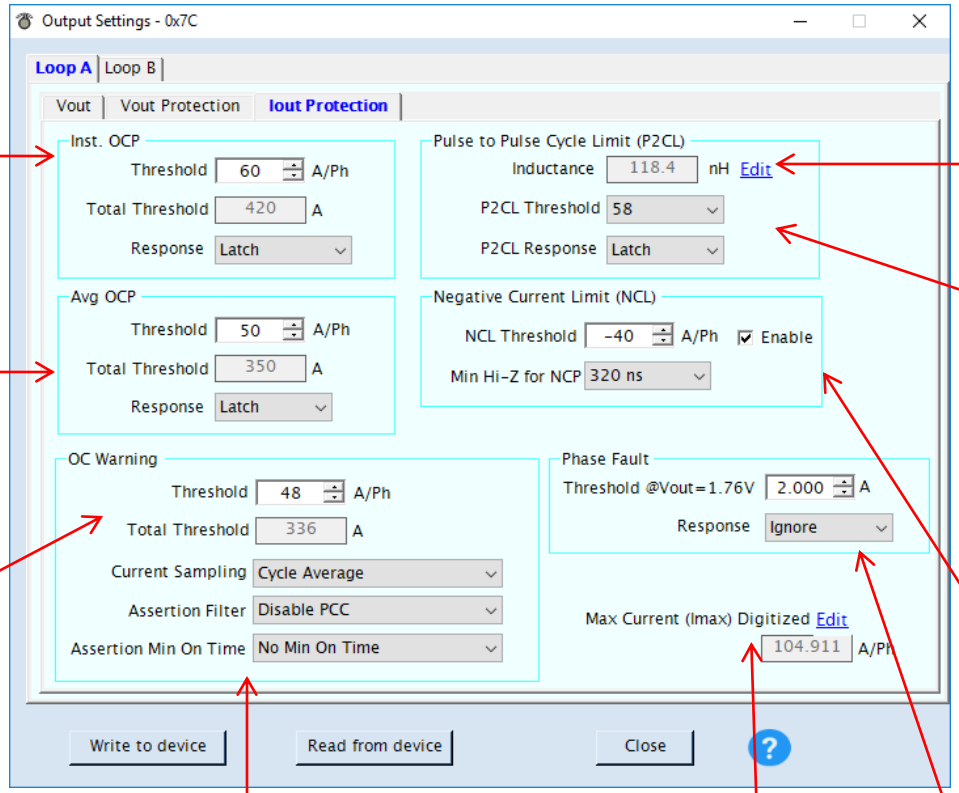
Inst. OCP (Over Current Protection)
- This looks at the instant peak current in each phase
- There is a 5 switching cycles delay before any action is taken
  - See next page for diagram
- **Response** will determine what action to take when the instant peak current exceeded its limit

Avg OCP (Over Current Protection)
- This looks at the average current in each phase
- Recommended settings per ph:
  - Icc Max * 1.15 / Nph Max
- **Response** will determine what action to take when the average current exceeded its limit

OC Warning (Over Current)
- This looks at the average filtered current in each phase
- Fault will be triggered if the average filtered current exceeded this limit

The function Peak Current Control in Sequoia that can be selected can be set to either cycle average that is the same as Sierra or instant current which is a faster but noisier detection mode

Total threshold
- Threshold that represents the total output current where the warning will be triggered



OC warning (PCC in AMD applications)
- A fast lightly filtered Over Current warning signal. Filter can be selected for how long over current have to be before it activates the output. The output can be selected for how long it will stay on after detection. It will reset itself after selected time if no more OC is detected.
- It uses the same threshold current as set in OC warning.

Max Current Digitized
- Highest phase current that can be measured
- Can be changed in the Current Sense dialogue

Inductance
- Output inductor for the buck converter that can be edited in the Feedback Loop/Output Model dialogue
- Use in the calculation for the P2CL function

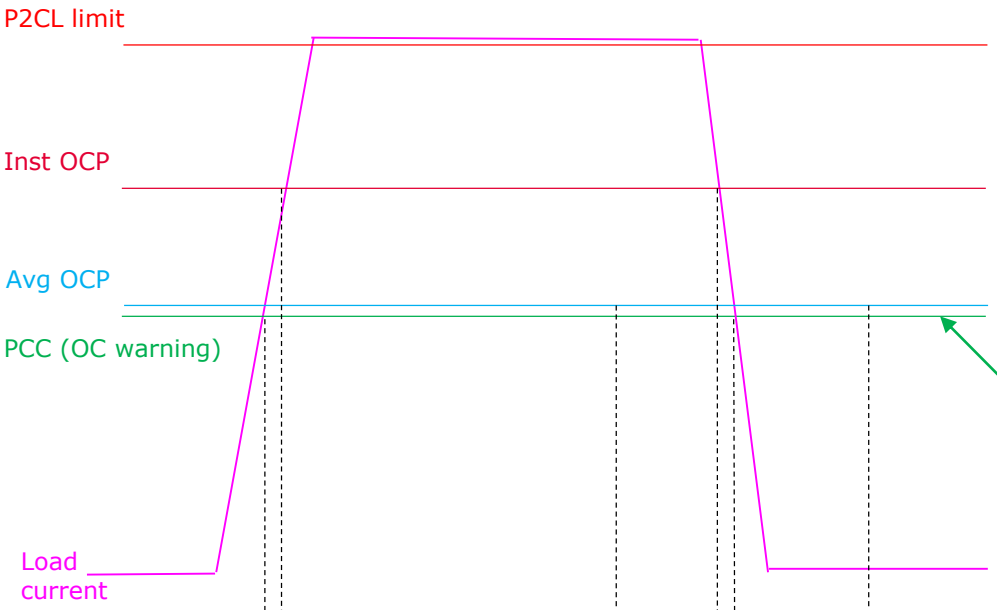
P2CL (Pulse to Pulse Cycle Limit)
- Per phase current limit designed to prevent inductor saturation by monitoring peak inductor current per phase and limit PWM pulse width cycle by cycle
- Recommended value is Isat @ 125 deg C in inductor datasheet minus 1 or 2A.
- **Response** will be triggered if current exceeded this limit for 255 consecutive switch pulses

Negative Current Limit (NCL)
- If the current in one phase goes too much negative, its PWM output will go to High Impedance (Hi-Z) for a specified minimum time.
- This function can be enabled by marking the box next to Enable. See explanation on following pages for function

Threshold @ vout=1.76V
- Maximum difference in phase current to trigger a phase fault. It change a little depending on Vout.

Response
- Response when phase fault signal comes from power stage

Output Settings...
The different current limits in Sequoia/Sierra



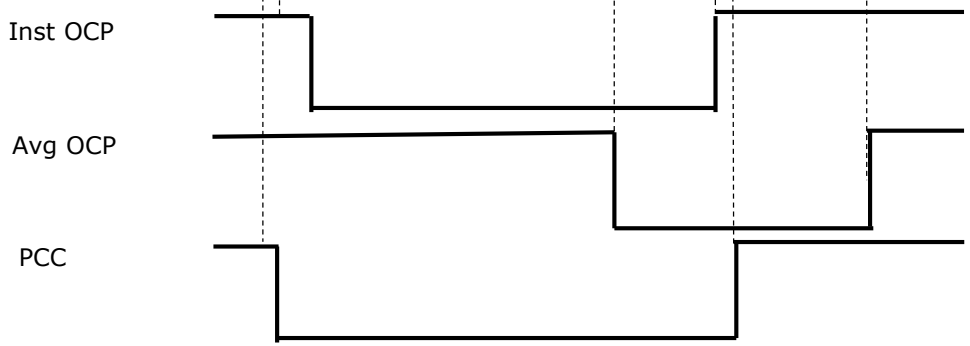
Look at each phase current pulse by pulse to protect against inductor saturation

Looks at total load current. Reaction time Typical 10us. Typical set according to system allowed max current

Looks at filtered average total current. Will react with some delay set by the filter. Typical 2ms Typical setting is the thermal limit current

Fast reacting (2-4us) peak current warning PCC. Typically set close to Avg OCP In XDPE122xx typical 4-6us delay. XDPE142xx 1-3us delay

Fault and Warning signals



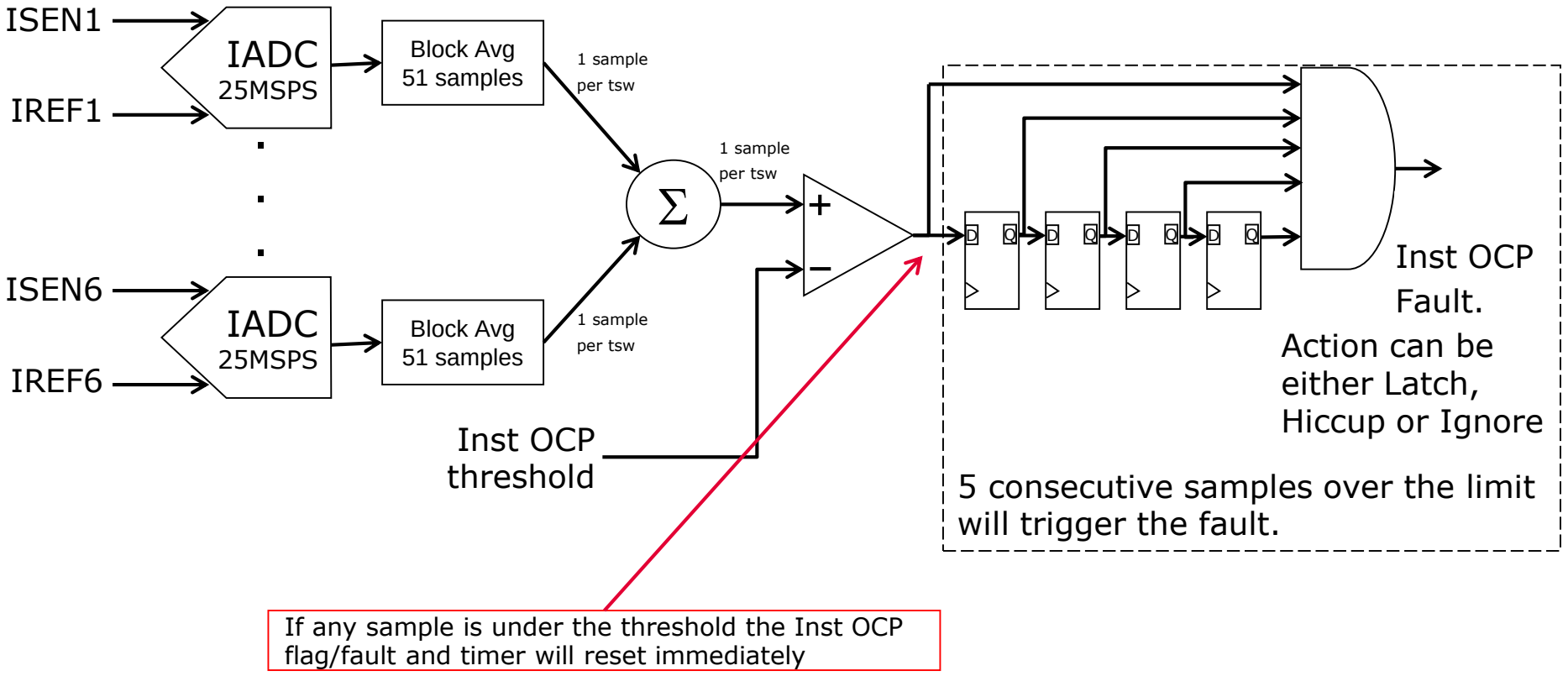
Inst OCP and AvgOCP can be selected to Turn off (Latch) or give a Warning.

PCC only give Warning

Active low signals

Output settings…
Inst OCP behavior

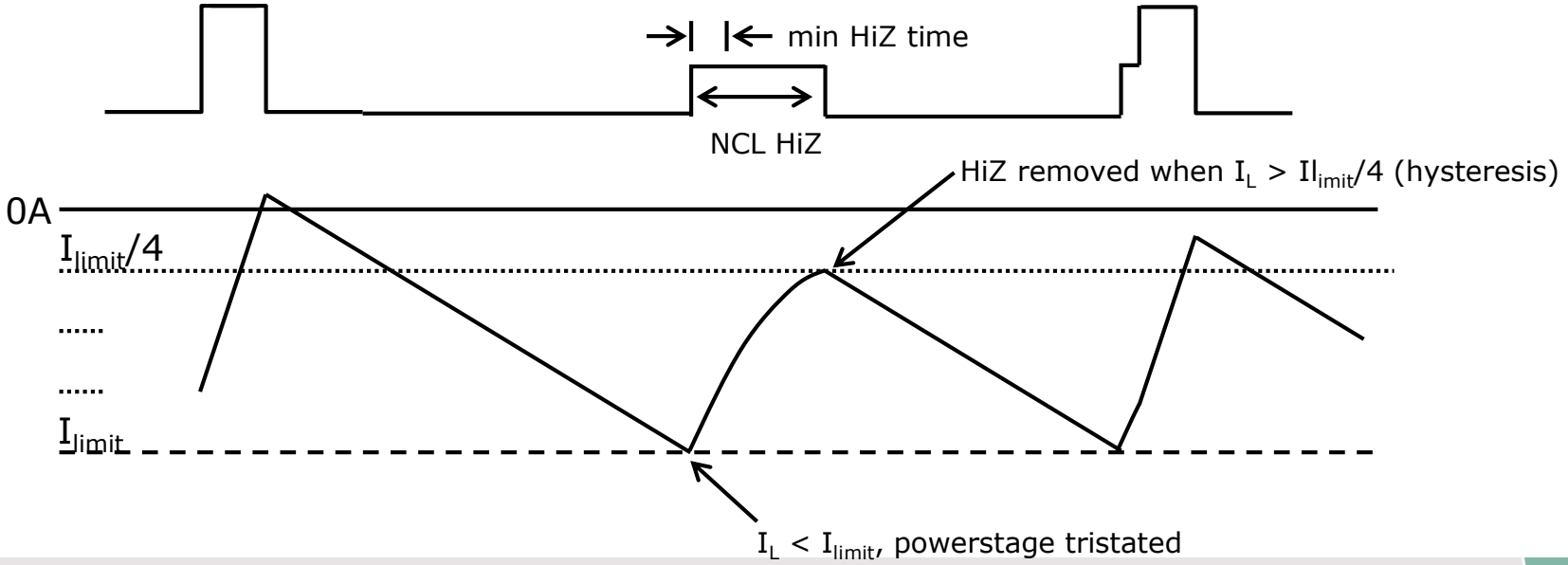
Notice that the current measured is the inductor current and not the direct load current. Inductor current rises slower than the load current and will add a delay that depends on variables like Inductance, Input voltage, output voltage and more.



If any sample is under the threshold the Inst OCP flag/fault and timer will reset immediately

Output Settings...
NCL function explanation

- Input: Iout
- Response time: 5ns; No shutdown response available
- Recommended settings: amplitude should be greater than the negative current induced by Cdv/dt during DVID down.
- Shutdown response: Not available
- If inductor current is too negative, highside FET may fail during the dead time between lowside off and highside on due to too much current going into the highside body diode.
- NCL will set lowside to off once the inductor current reaches the negative current limit
- To avoid chatting, the hysteresis level is set to release the HiZ only when the inductor reaches ¼ of the negative current limit and a minimum HiZ on time is satisfied.



Output Settings... limitations in OCP settings

- There is a limitation in what values Avg OCP and OC Warning/PCC can have.
- They can be set in steps of 2A and the range is 0-30A/phase less than Inst OCP.

- When changing Inst OCP the AvgOCP and PCC will change the same amount. i.e. Change Inst OCP 7A and both other will also change 7A

- InstOCP is not influenced by changes in AvgOCP or PCC

- Example Inst OCP =70A /phase AvgOCP = 60A and PCC =46A
- Change Inst OCP to 69A and that will make AvgOCP=59A and PCC=45A

Output Settings...
Avg OCP or Avg OC Warning behavior

Filter

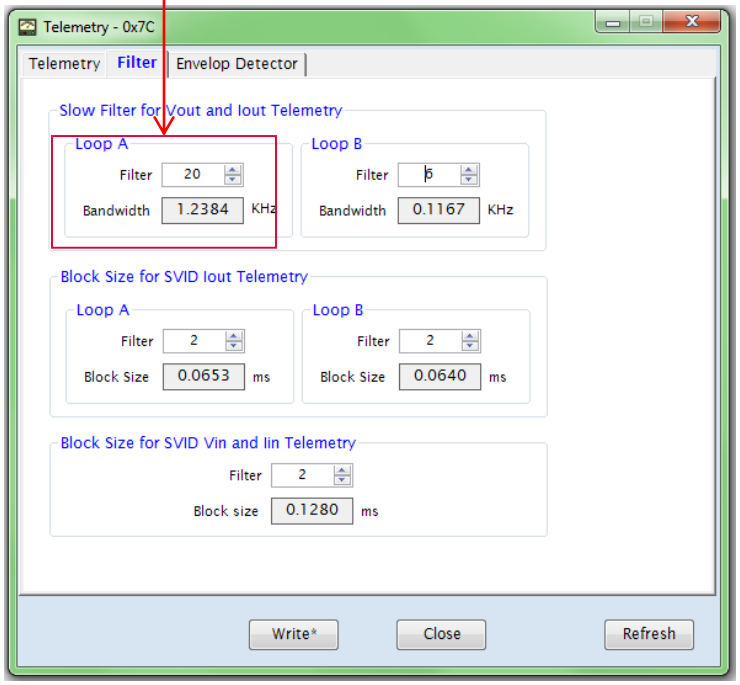
Filter frequency can be selected.

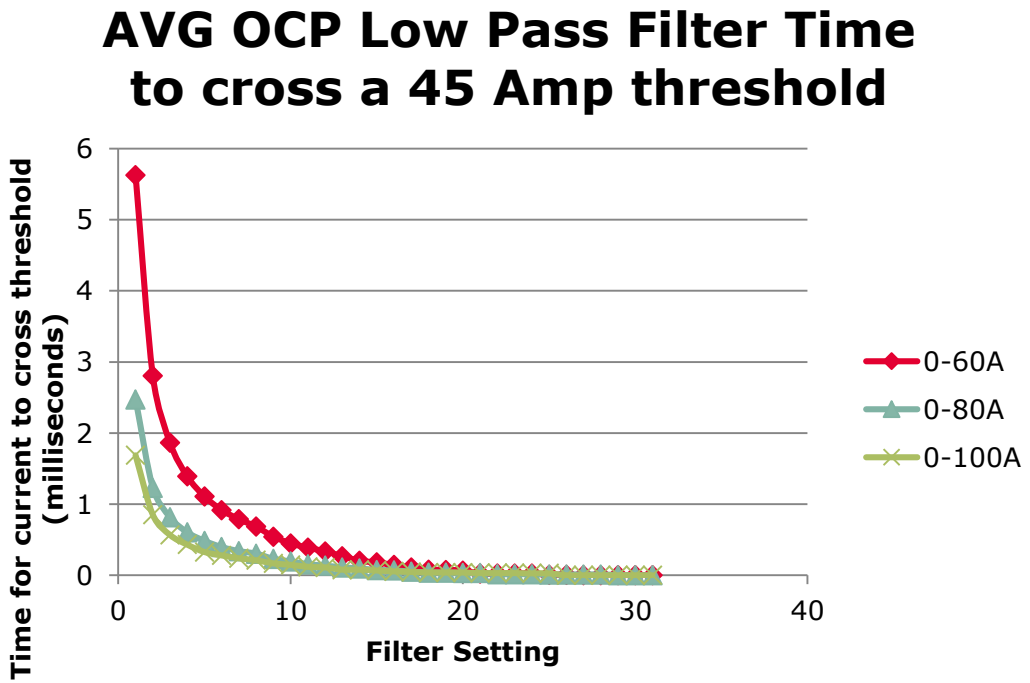
Time for a overcurrent signal to pass through the filter will depend on how much overcurrent.

Like for any low pass filter a small current step take longer time to get to the threshold than a large overcurrent. See graph for example where limit is selected to 45A and different current steps.

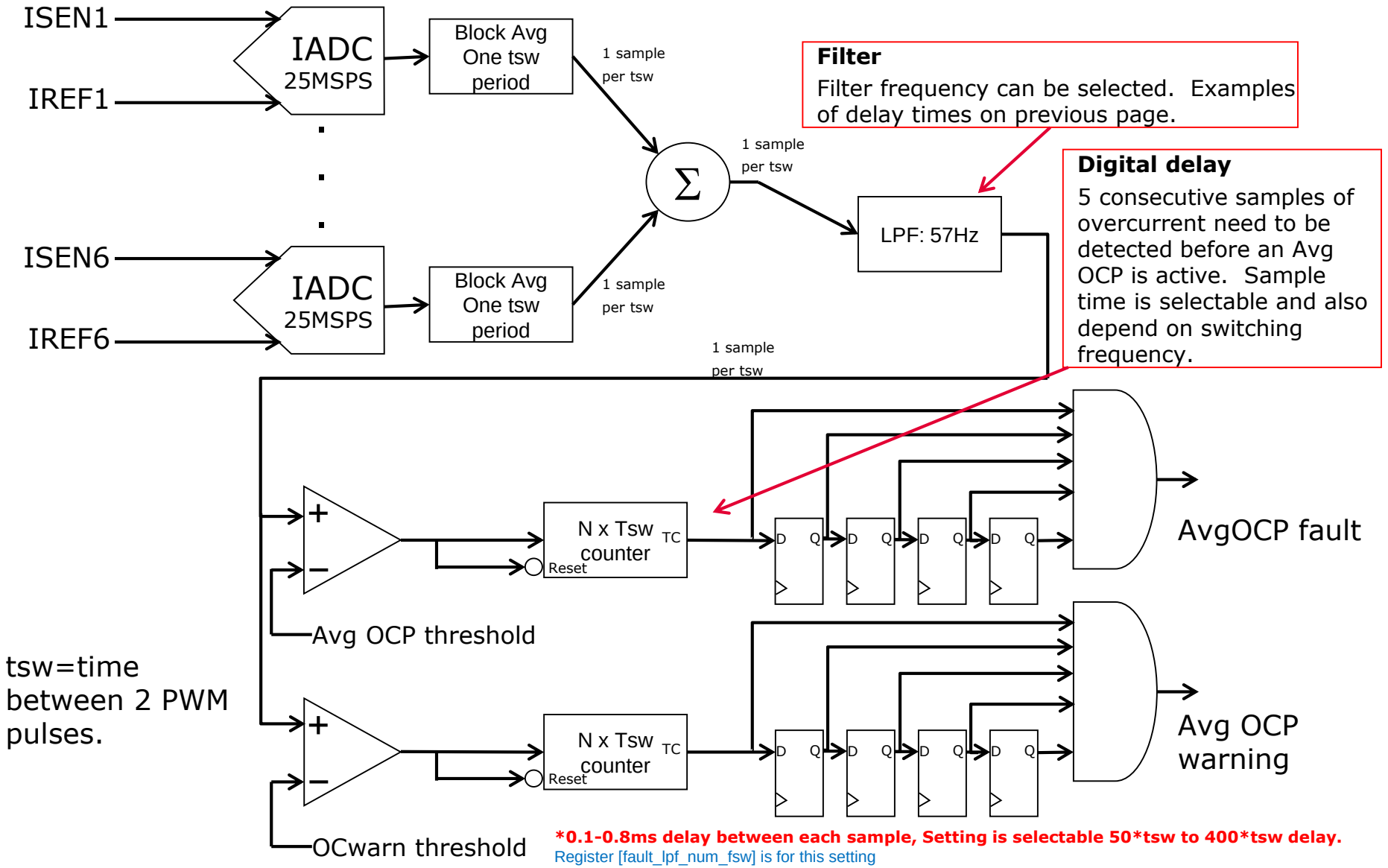
Total delay times from an Overcurrent to fault response is the sum of Filter frequency selected and the corresponding delay time and also depend on switching frequency as there is an 5 consecutive sample digital delay after the filter. This digital delay makes higher filter frequencies insignificant to total time delay.

See block diagram on next page for more details.

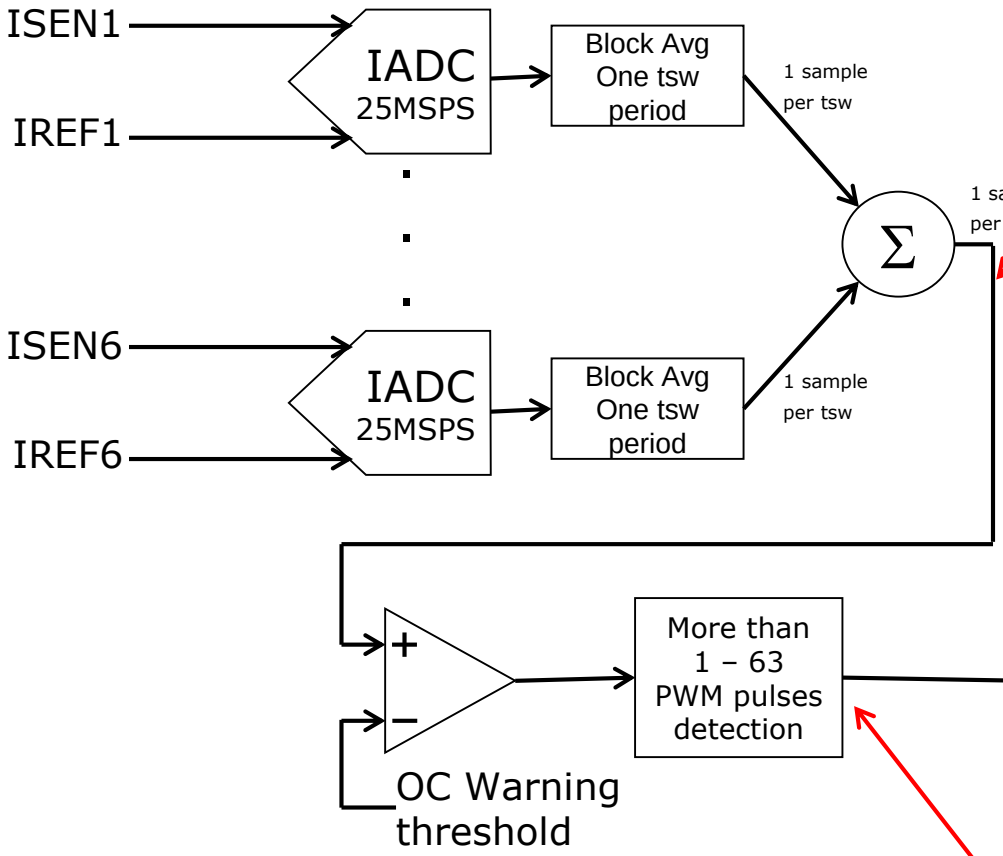




Output Settings...
Avg OCP and Avg OCP warning



Fast OC warning Sierra and Sequioa Cycle sampling. AMD PCC peak current control



Delay time
1-2 full PWM cycles
Notice the sampling need at least one full PWM cycle to pass through the Block average filter and depending on how fast load current rises and when in time it happens it may need one more sample to reach the threshold level.

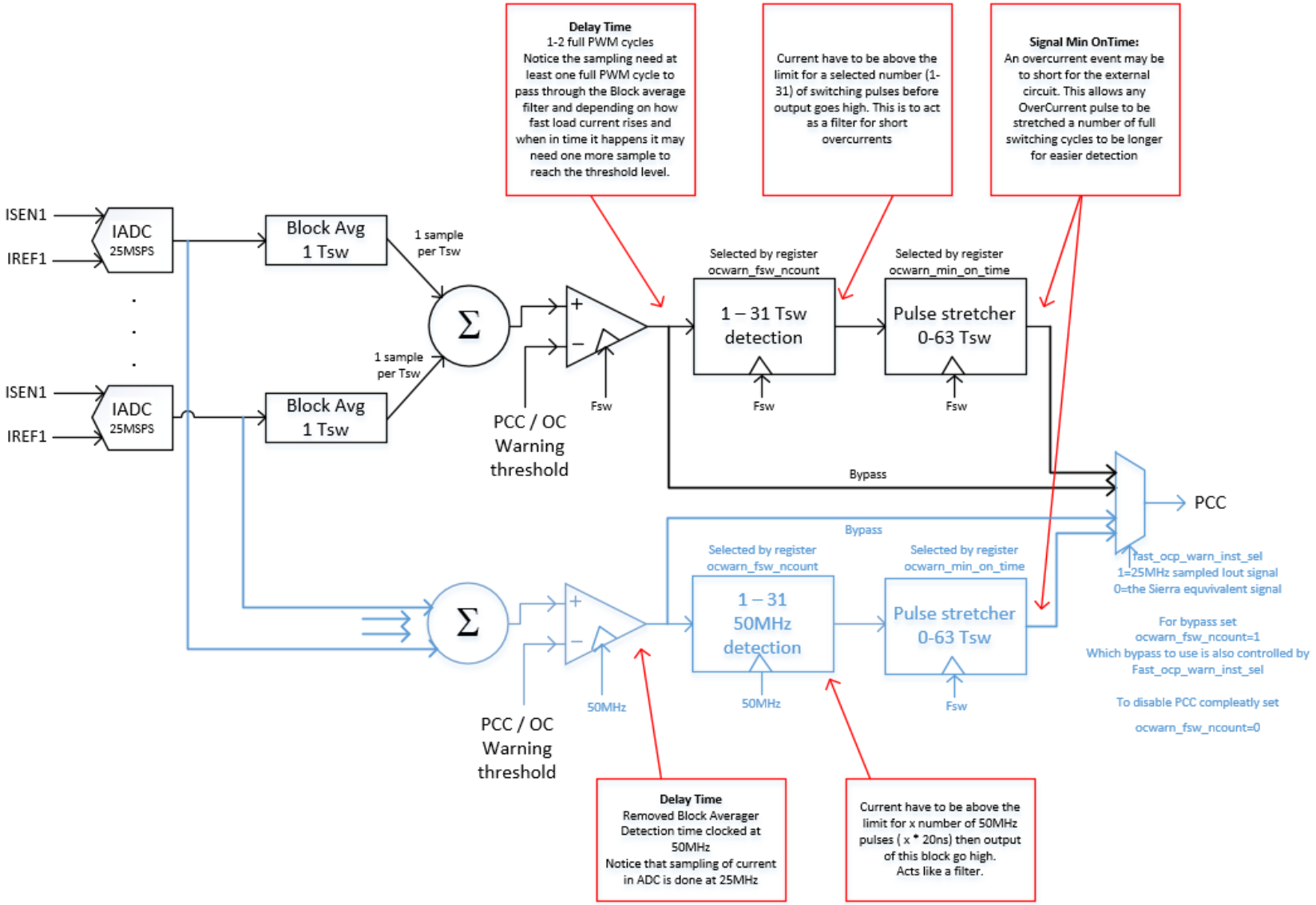
Notice that the current measured is the inductor current and not the direct load current. Inductor current rises slower than the load current and will add a delay that depends on variables like Inductance, Input voltage, output voltage and more.

tsw=time between 2 PWM pulses.

Current have to be above the limit for a selected number of switching pulses before output goes high. This to act as a filter for short overcurrents

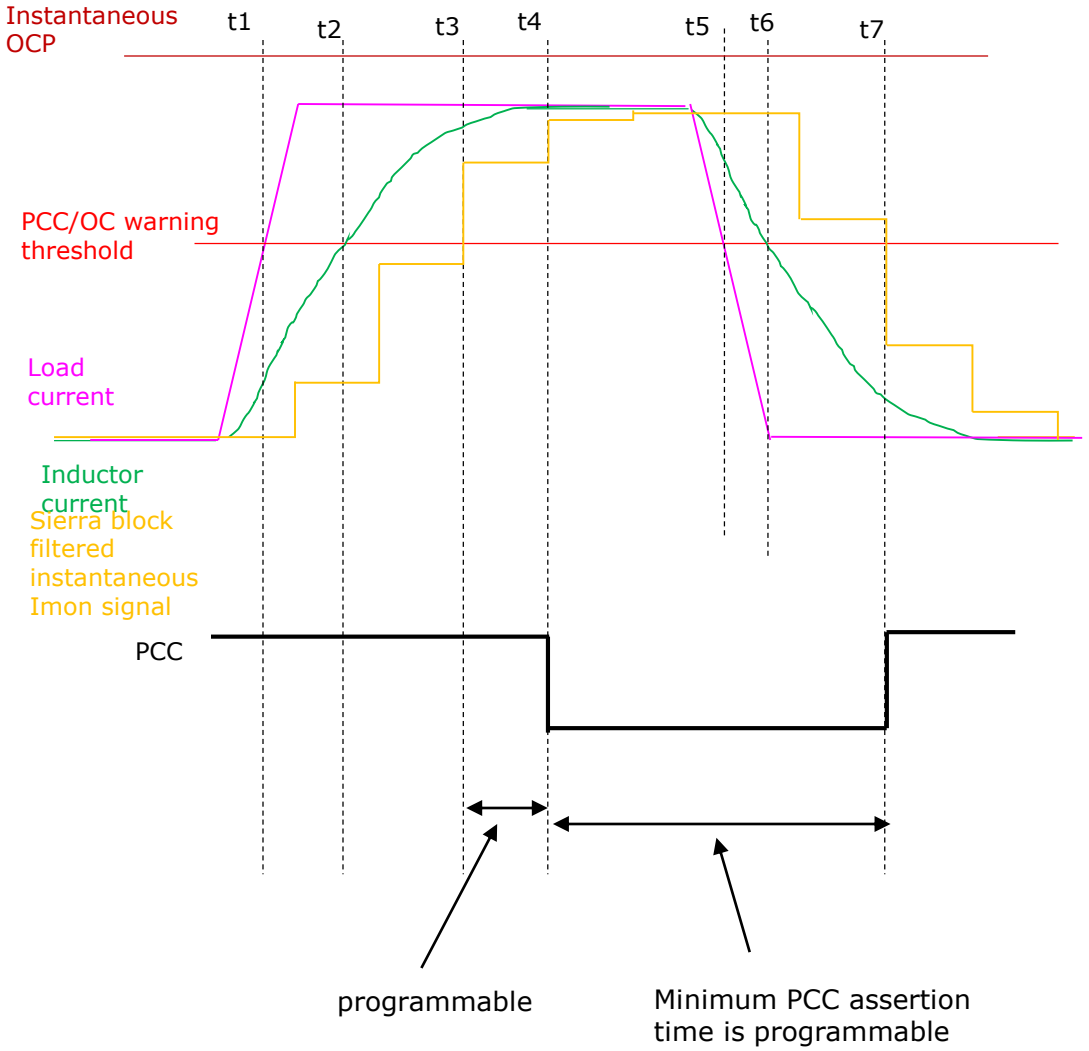
Signal Min OnTime:
An overcurrent event may be to short for the external circuit. This allow any OverCurrent pulse to be stretched to be longer for easier detection

Fast OC warning Sequoia Inst. Current sampling AMD PCC peak current control



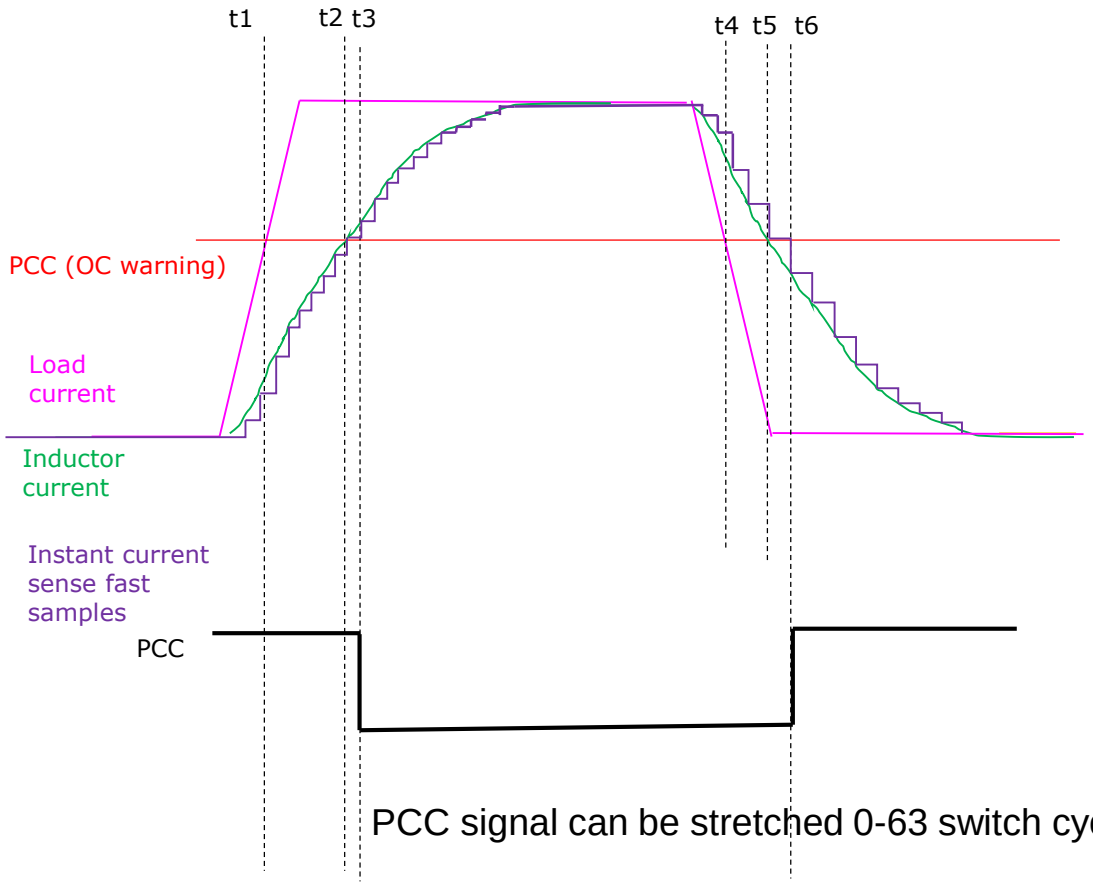
Symbols in Blue is the new faster PCC path added in Sequoia

OC warning Sierra and Sequoia AMD PCC peak current control



- t1: load current reaches OC warning threshold Some of the current comes from the output capacitors while inductor current takes time to increase
- t2: Inductor current reaches OC warning threshold. Contribution to the delay between t2 and t1:
  - Output inductance (Higher=slower)
  - Input voltage (higher=faster)
  - Loop bandwidth (higher=faster)
- t3: Instantaneous Imon (switching cycle block averaged inductor current) reaches OC warning threshold. Delay between t3 and t2 is <=two switching cycles
- t4: PCC is asserted. Delay between t4 to t3 is programmable in range of 1~63 switching cycles
- t5:load current decreases and reaches OC warning threshold
- t6: Inductor current decreases and reaches OC warning threshold
- t7:Instantaneous Imon follows inductor current and goes below OC warning threshold which de-assert PCC signal. Note: the assertion time should be >minimum assertion time which is programmable in range from 0~63 switching cycles

Faster PCC only Sequoia XDPE142xx
AMD PCC peak current control

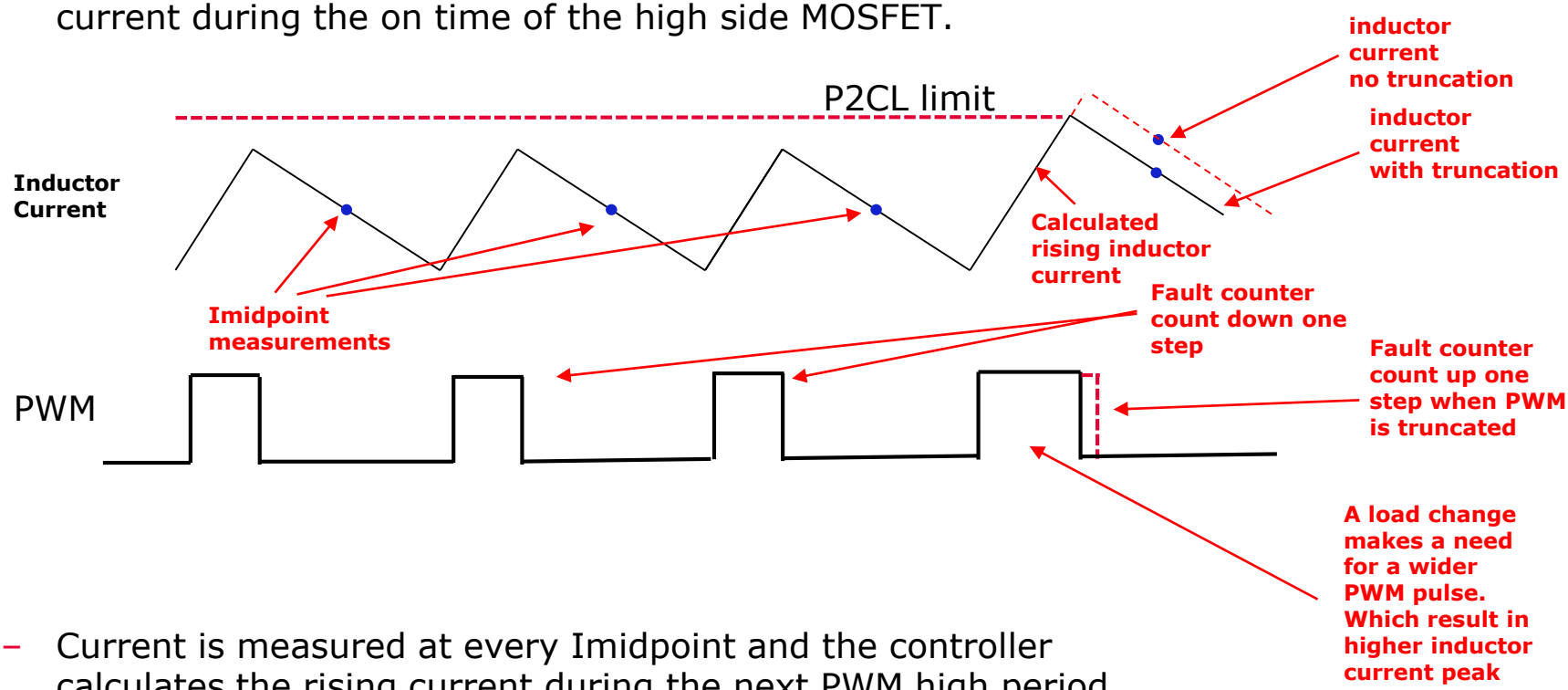


- t1: load current reaches OC warning threshold
- t2: Inductor current reaches OC warning threshold. Contribution to the delay between t2 and t1:
  - Output inductance
  - Input voltage
  - Loop bandwidth
- t3: Current sampled at 25Mhz reaches OC warning threshold.
- t4:load current decreases and reaches OC warning threshold
- t5: Inductor current decreases and reaches OC warning threshold
- t6:Current sampling follows inductor current and goes below OC warning threshold which de-assert PCC signal.

PCC signal can be stretched 0-63 switch cycles Shown with 0 stretch

P2CL Pulse to pulse cycle limit

- Internal Calculation of phase current
  - Inductor value , Measured Vin, Vout and Imidpoint are used to calculate the inductor current during the on time of the high side MOSFET.



  - Current is measured at every Imidpoint and the controller calculates the rising current during the next PWM high period.
  - When the calculated current reaches the P2CL limit the PWM will be truncated

P2CL Pulse to pulse cycle limit

Response :

- Each PWM pulse will immediately be truncated when the phase current exceed the P2CL limit
- Fault flagged after 255 switching cycles above limit.
  It uses an up/down counter.
  It will count down for all pulses that are below threshold and up again if new pulses exceed threshold.
  When number of accumulated above threshold pulses reaches 255 a fault signal is generated.
- A single pulse under threshold will not reset counter to 0 like the other current limit functions
- Counter do not go below 0

› Recommended settings: Inductor saturation current or 1-2A below saturation current

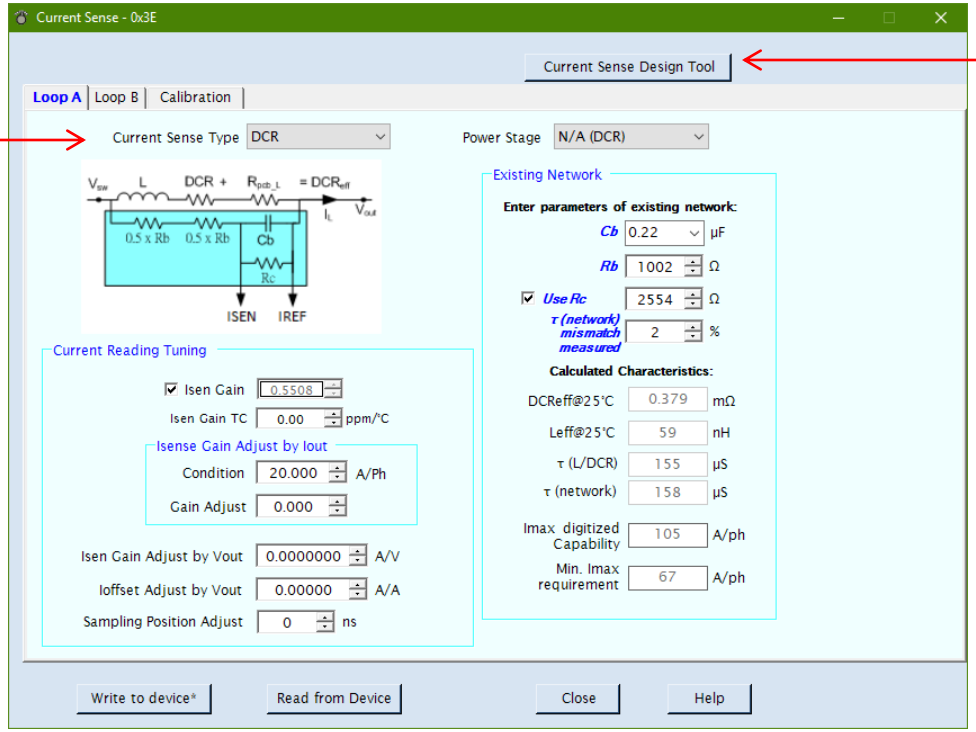
› Shutdown response: Shutdown/Ignore/Hiccup

Agenda

Current sense...

Current Sense Type

- For XDPE1x286 and XDPE12550 part, selection can be *DCR* sense (as shown), *DCR Shunt* or *Non-DCR* (i.e. power stage with internal current sense)
- For other parts, current sense type will automatically change to *Non-DCR*
- Graphical figure will change to match selection made



Current Sense Design Tool

- Dialog that helps calculate the settings and any resistors needed

Current sense... DCRsense

Isen Gain
- Gain factor for the measured voltage across Cb that represent the current through the inductor
- Tune this value such that the current reading gain is accurate from 0A to 2/3 of TDC with **Isen Gain TC** set at 3906.25ppm/°C when temp change in inductor is small
- To get a starting value set the gain=0.15mV/DCR

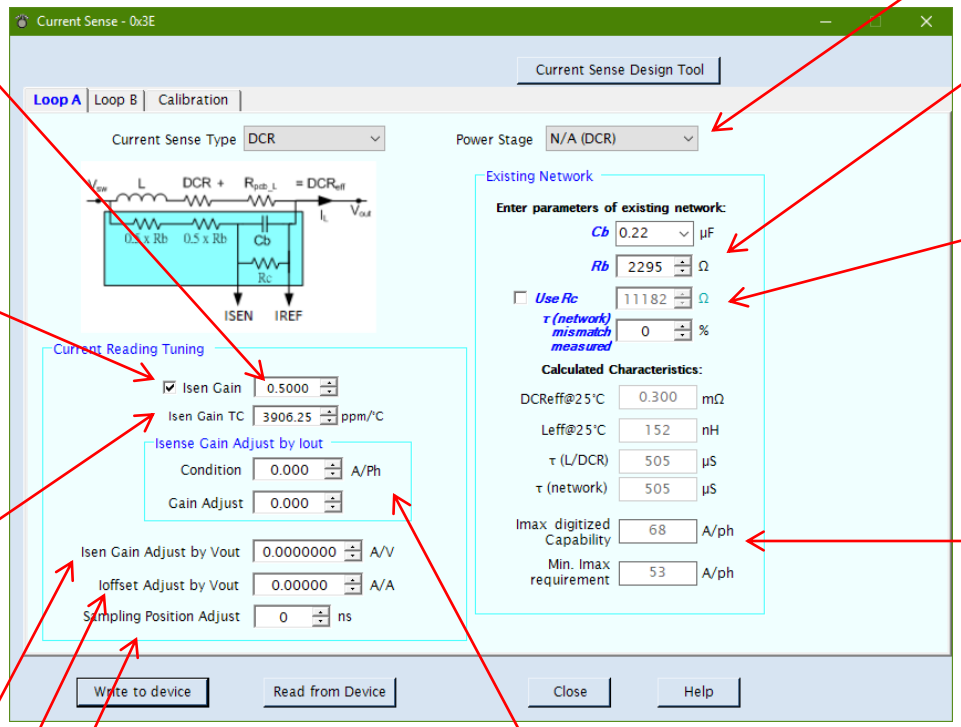
Isen Gain checkbox
- Checked: override calibrated gain settings from the *Calibration* tab
- Unchecked: gain will use values from the *Calibration* tab

Isen Gain TC
- Temperature Coefficient for gain
- Typically between 2000 ~ 4000 ppm/°C
- Use the ideal copper TC=3906.25 first and then based on temperature compensation result of inductor DCR to trim this value
- This value could be different by layout.

Isen Gain Adjust by Vout
- Linear current sense gain compensation based on Vout

Ioffset Adjust by Vout
- Offset f the current sense based on Vout

Sampling Position Adjust
- Adjustment of reported phase current in the ***Telemetry*** window
- See next page for explanation



Power Stage
- When **Current sense Type** is *DCR*, selections are *DCR* and *Sense Resistor*

Cb and **Rb**
- Enter the real values used on the PCB for capacitor and resistor
- Cb typical 0.22uF

T (Network) mismatch measured
- This is the mismatch in the two time constants Rb*Cb and L/DCR for the real components
- Typical put a value 1-2%
- Explanation follows on the next pages

Imax Digitized and **Min. Imax requirement.**
- Check that the calculated **Imax Digitized** capability is equal or higher than **Min Imax Requirement**
- If not try to add more Rc to get a lower voltage on the ISEN-Iref signals. This to not exceed the 30mV input range for the current sense input for DCR.

Isen Gain Adjust by Iout
- Optional gain adjustment to the current sense based on Iout
- Compensate for a non-linear behavior in current reporting for small currents
- For load currents greater than the specified A/ph Condition, the specified **Gain Adjust** value will be applied
- Recommended setting for **Condition** is 16~20A/ph

$$Isen\ Gain\ @\ I_x\ per\ phase = Isen\ Gain * (I_x - I_{condition}) * (1 + GainAdjust)$$

Current sense... Sense resistor

Isen Gain
- Gain factor for the measured voltage across Cb that represent the current through the inductor
- Tune this value such that the current reading gain is accurate from 0A to 2/3 of TDC with **Isen Gain TC** set at 3906.25ppm/°C when temp change in inductor is small
- To get a starting value set the gain=0.15mV/DCR

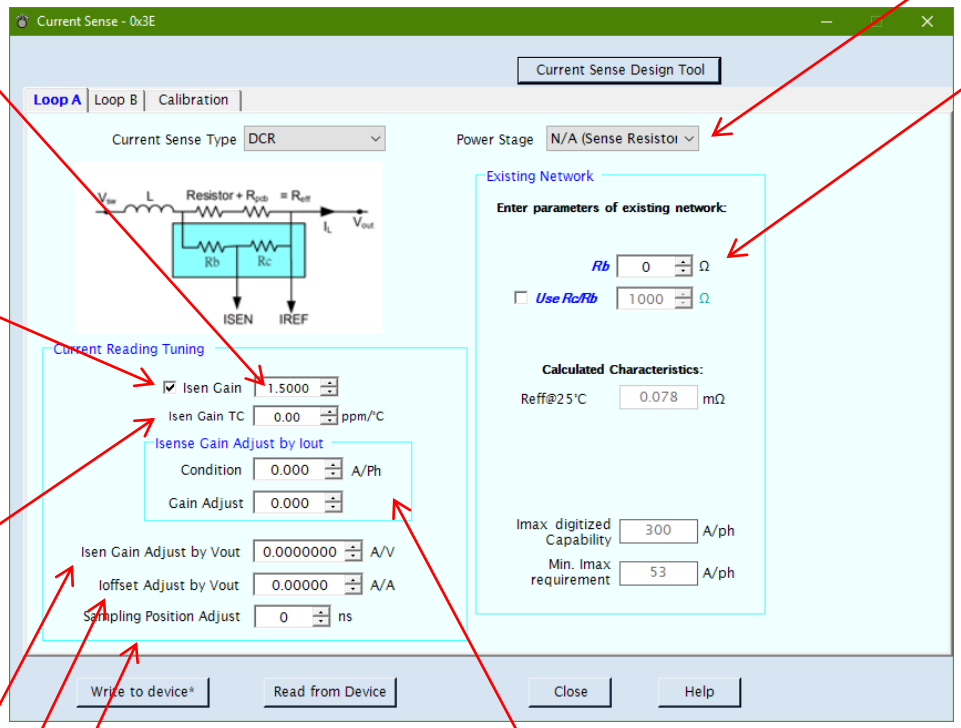
Isen Gain checkbox
- Checked: override calibrated gain settings from the *Calibration* tab
- Unchecked: gain will use values from the *Calibration* tab

Isen Gain TC
- Temperature Coefficient for gain
- Typically between 2000 ~ 4000 ppm/°C
- Use the ideal copper TC=3906.25 first and then based on temperature compensation result of inductor DCR to trim this value
- This value could be different by layout.

Isen Gain Adjust by Vout
- Linear current sense gain compensation based on Vout

Ioffset Adjust by Vout
- Offset f the current sense based on Vout

Sampling Position Adjust
- Adjustment of reported phase current in the ***Telemetry*** window
- See next page for explanation



Power Stage
- When **Current sense Type** is *DCR*, selections are *DCR* and *Sense Resistor*

With a sense resistor instead of DCR sense, the resistor divider is often 0ohm.

Typically temperature dependance TC is much less than for DCR. See resistor vendors datasheet for value.

Isen Gain Adjust by Iout
- Optional gain adjustment to the current sense based on Iout
- Compensate for a non-linear behavior in current reporting for small currents
- For load currents greater than the specified A/ph Condition, the specified **Gain Adjust** value will be applied
- Recommended setting for **Condition** is 16~20A/ph

$$Isen\ Gain\ @\ I_x\ per\ phase = Isen\ Gain * (I_x - I_{condition}) * (1 + GainAdjust)$$

Current sense... Non-DCR

Isen Gain
- Gain to use for all phases for the signal from the power stage
- To get a starting value, set the gain=0.35 when using a power stage like TDA21460

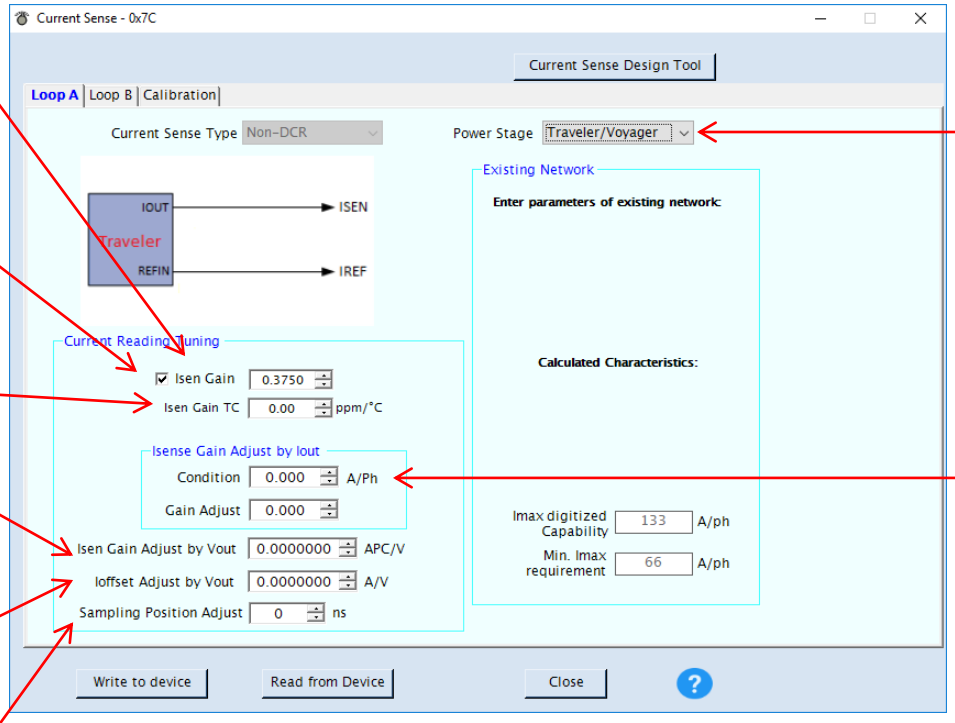
Isen Gain checkbox
- Checked: override calibrated gain settings from the *Calibration* tab
- Unchecked: gain will use values from the *Calibration* tab

Isen Gain TC
- Temperature Coefficient for gain
- Typically set to 0

Isen Gain Adjust by Vout
- Linear current sense gain compensation based on Vout

Ioffset Adjust by Vout
- Offset f the current sense based on Vout

Sampling Position Adjust
- Adjustment of reported phase current in the ***Telemetry*** window
- See next page for explanation



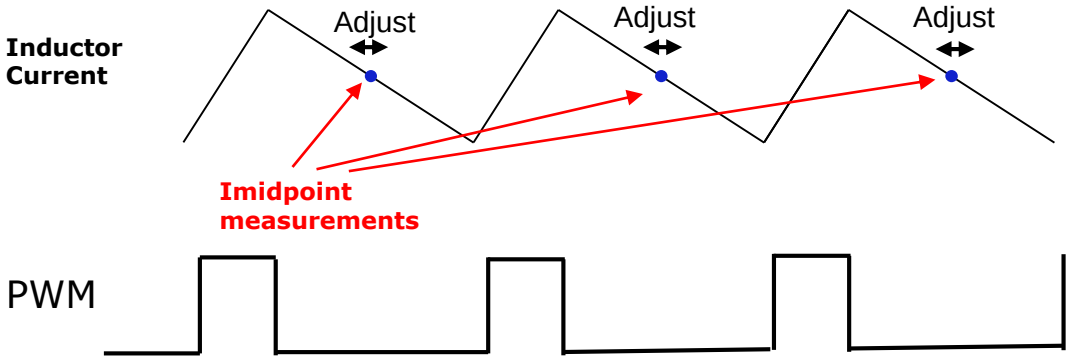
Power Stage
- When **Current sense Type** is *Non-DCR,* select device name family depending on the power stage being used
- *Traveler/Voyager*
- *Big Rock*
- *Sapphie/Denali*

Isen Gain Adjust by Iout
- Optional gain adjustment to the current sense based on Iout
- Compensate for a non-linear behavior in current reporting for small currents
- For load currents greater than the specified A/ph Condition, the specified **Gain Adjust** value will be applied
- Recommended setting for **Condition** is 16~20A/ph

$$Isen\ Gain\ @\ I_x\ per\ phase = Isen\ Gain * (I_x - I_{condition}) * (1 + GainAdjust)$$

Current Sense…

- Sampling Position Adjust. Will influence the Phase current in Telemetry window
  - Current is measured at every Imidpoint of the falling edge of inductor current and the controller use this for current balance function and report the per phase current in telemetry window
  - Sometimes the inductor current curve is not perfect. Delays in powerstage and distortion shift the curve and the reported phase current will not be the actual average phase current.
  - This setting allow for some adjustment to get closer to the mid point of inductor current that is then reported in Telemetry window as phase current.
  - Current balance is not influenced as it still compare all phases at same point in time.



With Adjust as negative the sampling occur earlier equals higher reported current
Positive number delays the sampling and reports a lower phase current

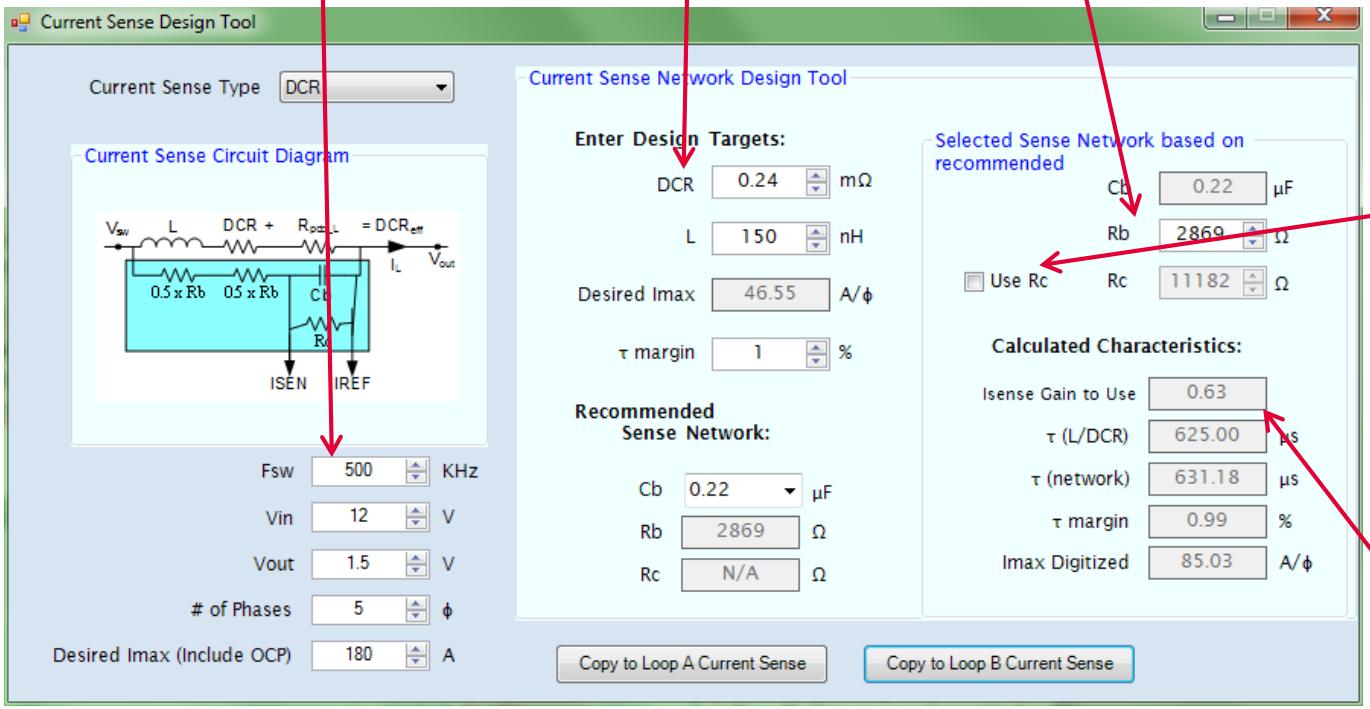
Current sense... Current sense design tool

A tool to help calculate current sense parameters. Use knowledge from the 3 following theory slides to find suitable numbers to enter.

First enter some basic numbers for the design

2nd step. Enter Data for inductor used
And the Cb capacitor 0.22uF recommended.
T margin typical 2%

3rd step. Enter Data for Rb resistor



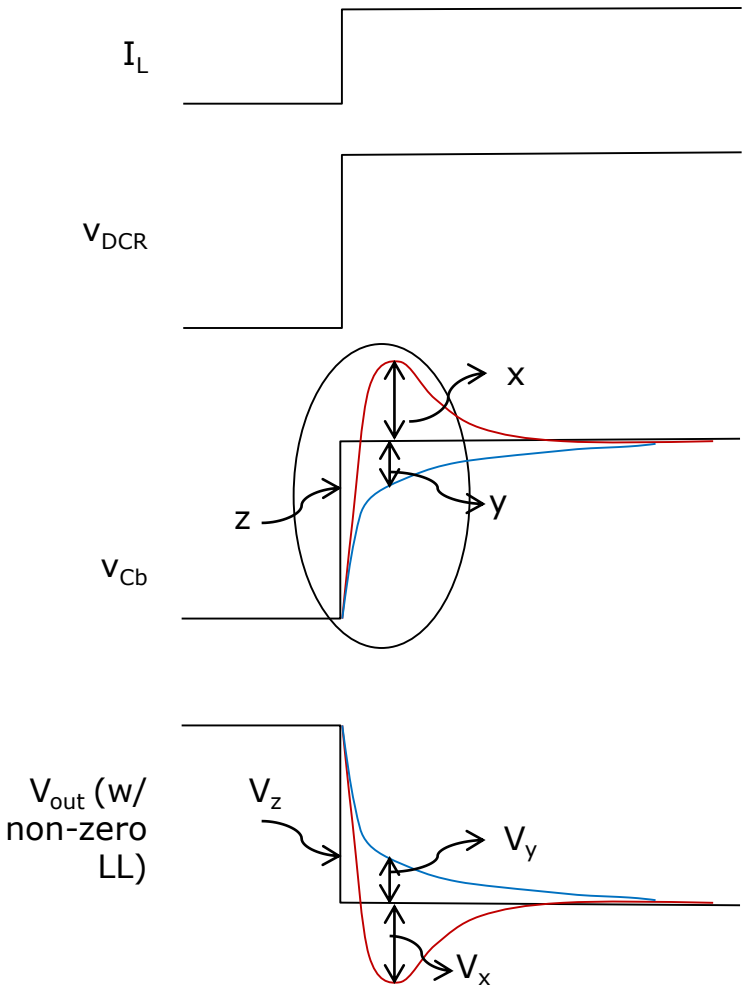
Use Rc. If there is a high DCR value the sense voltage may be needed to be divided down by using resistor Rc. If this is used mark the box and enter a number in the **Rc** field

Isense gain. Calculated value that can be used as Isense gain in the current sense window.

It is to be used as starting point as final gain is determined by testing.

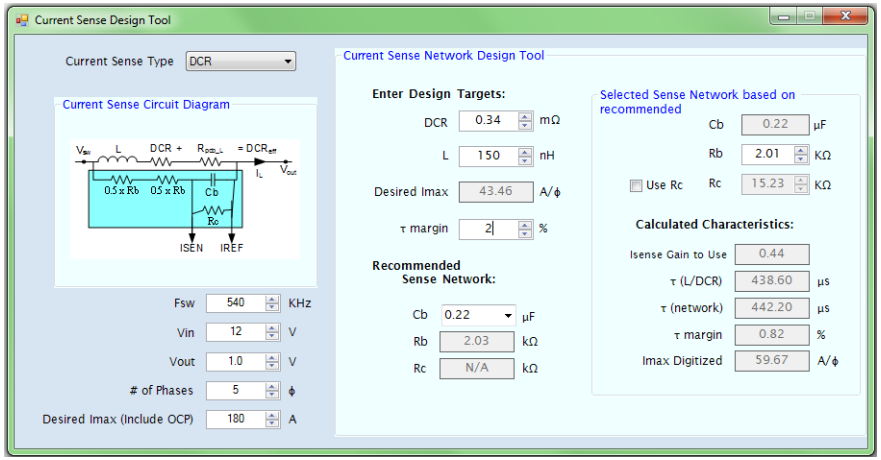
Current sense... dynamic response: Rb*Cb time constant

$$v_{Cbx} = v_{DCRx} * \frac{L/DCR}{R_b * C_b}, \quad s \to \infty$$



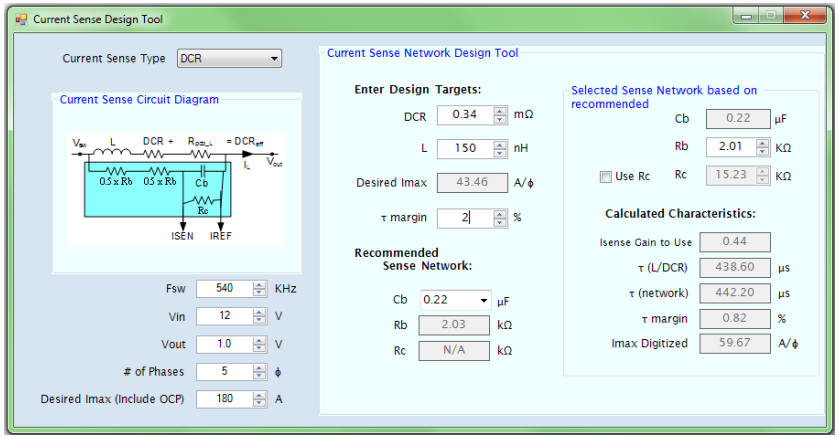
- Impact of how Rb*Cb compared to L/DCReff:
  - If R_b*C_b = L/DCReff, v_{Cb} will be the same v_{DCR} at any frequency
  - If R_b*C_b < L/DCReff, v_{Cb} will underdamp v_{DCR} which leads to overshoot/undershoot during transient when LL is non-zero. To adjust time constant:
    - $(R_b*C_b)_{new} = (R_b*C_b)_{orig}*(1+x/z)$
  - If R_b*C_b > L/DCR, v_{Cb} will overdamp v_{DCR}. To adjust time constant:
    - $(R_b*C_b)_{new} = (R_b*C_b)_{orig}*(1-y/z)$

Current sense... Adjust DCR sense network time constant – method 1: using transient waveforms with non-zero LL slope (1 of 2)



- The DC current sense gain must be tuned before adjusting time constant → actual DCR on board $DCR_{eff@25degC} = DCR_L + DCR_{trace}$ can be calculated
- Step 1: enter C_b and R_b values used on the board
- Step 2: set up transient load from 5% TDC to 55% TDC and measure z and x or y in previous page
- Step 3: if V_{Cb} overshoots V_{DCR}, enter x/z to "τ mismatch measured"; otherwise, enter –y/z to "τ mismatch measured" → actual L can be calculated

Current sense... Adjust DCR sense network time constant – method 1: using transient waveforms with non-zero LL slope (2 of 2)



- Step 5: Select the desired C_b value and then R_b will be calculated automatically
  - Tip: recommend to keep the same C_b value and only adjust R_b value to minimize modifications on board
- Step 7: change the R_b or C_b to the new values on the board and verify DC current reading and time constants matching again
  - Iteration of DC current reading and time constant adjustments might be necessary

Current sense... Calibration

- Partly automated calibration of offset and gain per phase.
- Optimizes the reported current and compensate for variations between phases.
- It is also possible to manually enter values into the **Register Value** section.

Calibration Procedure

1. Check the **Phx** checkbox to select which phase(s) to calibrate.
2. Click **Begin Calibration** button
   - A series of pop up windows will guide the user when to turn on/off the load.
   - Note: max of 30A per phase
   - GUI will measure telemetry values in each phase in sequence with no load and with load and will calculate offset and gain for each selected phase.
   - Calculated calibrated values will be displayed in the *Calibration Values* column.
3. Click on the **Copy Calibration Values to Registers** button to copy the values to the register section.
4. Click the **Write to device** button to write them into memory of the controller.

Phx

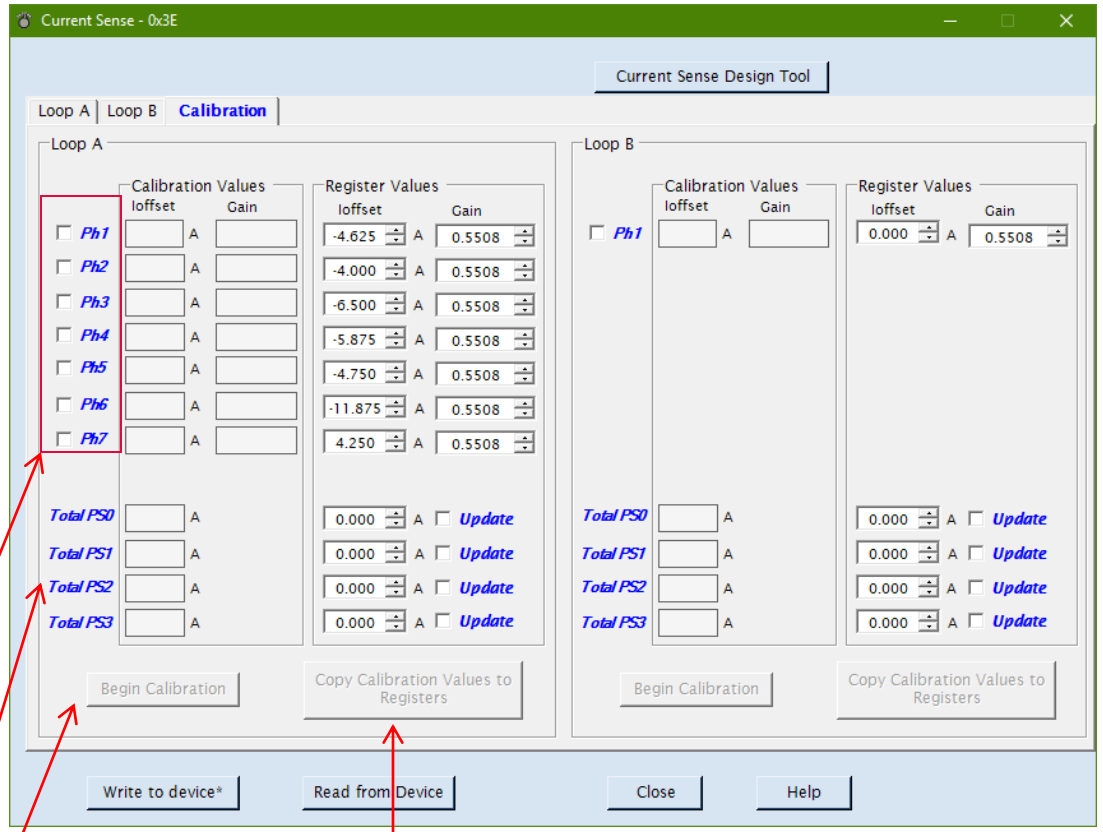
- When checked, phase x will calculate the suggested calibration values for Ioffset and Gain.

Total PSx - Ioffset

- Total Ioffset for each PS states.
- During calibration, calibrated values are automatically changed to 0
- Selecting the **Update** checkbox will copy these values to its equivalent Register Values dialog fields when **Copy Calibration** button is selected

Begin Calibration

- When selected, it will start the calibration process.
- Only enabled when at least 1 **Phx** checkbox is selected.



Copy Calibration Values to Registers

- This will copy the calculated *Calibration Values* column to the *Register Values* column.
- **Write to device** button needs to selected to write to the actual registers

Current sense... Calibration

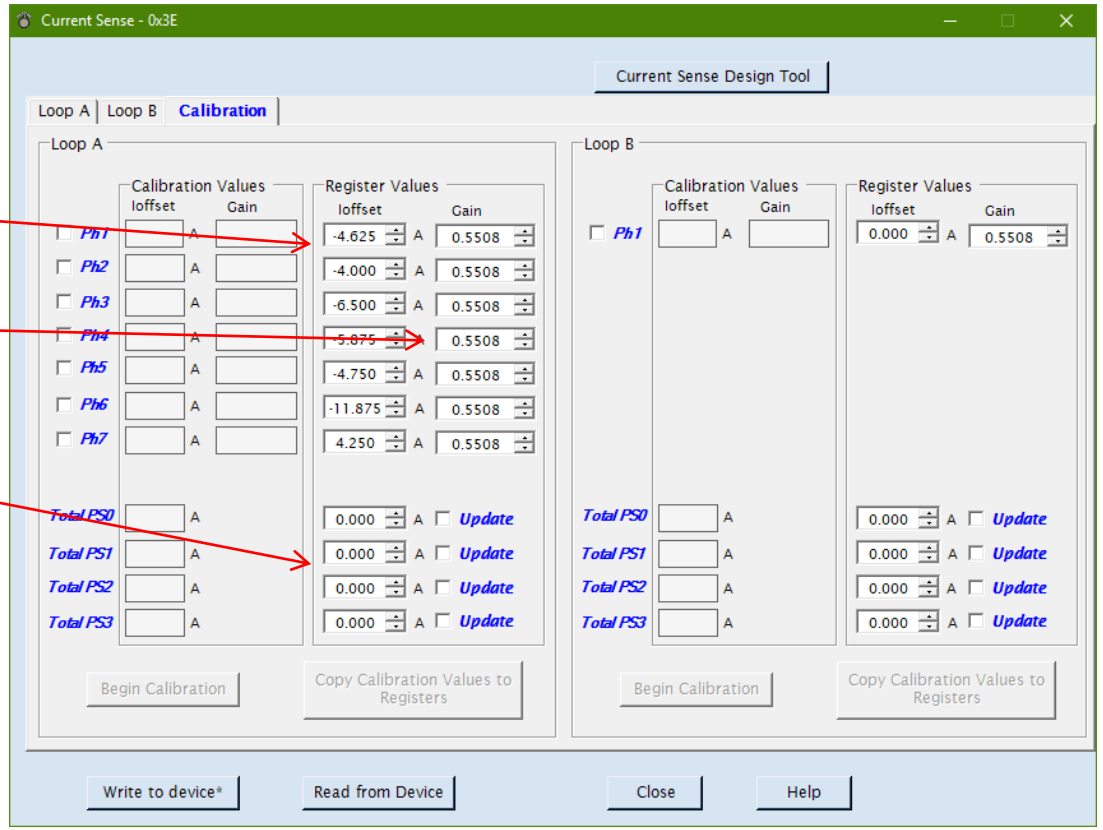
Differences in DCR sense, power stages or layout can make each phase differ slightly in **Gain** and **Ioffset**.

Gain will be locked against changes if the "hook" on Loop A or B tab is marked as then all Gain is forced to the same setting as entered in Loop tab.

Ioffset
- Offset current for each phase.
- Can be entered manually or automated by the calibration function

Gain
- Gain for each phase.
- Can be entered manually or automated by the calibration function.

Total PSx Ioffset
- Adjustment of reported current for different PowerStates.
- As PowerStates may use different number of phase, the reported current may change and can be compensated by adding an offset.



Agenda

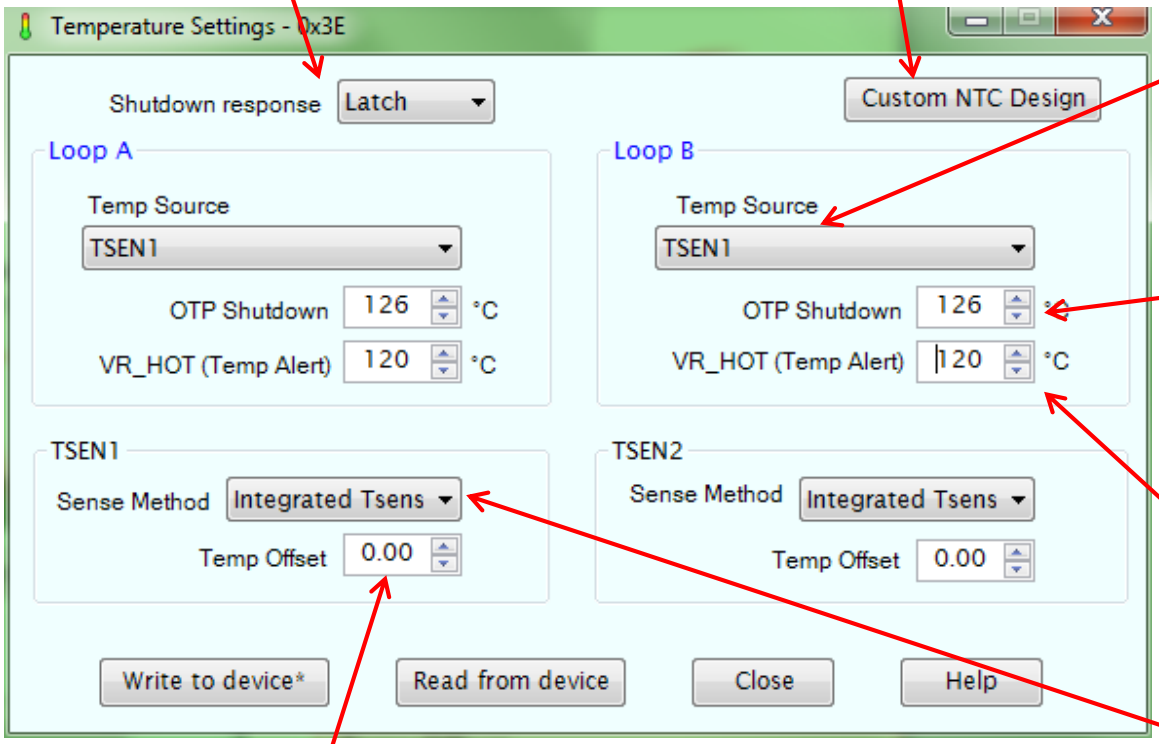
Temperature Settings

Shutdown response :

What to do when an OTP Shutdown temperature threshold is passed

Custom NTC design :

This button open a new window where calculations can be done when a non standard NTC is used



Temp Source:

Temperature signal comes from :

-TSEN1

-TSEN2

It is possible to have same Sensor input for both loops

OTP Shutdown:

Select the temperature for when Over Temperature Shutdown is to be activated.

VR_HOT :

Select the temperature for when VR-HOT fault and pin to be activated. This function have a 3% hysteresis. i.e. When set to 100C the VR_HOT warning will be set when temperature goes above 100C and stay on until temperature drops 3% (97C) then the fault flag reset itself.

TSEN1 and TSEN2:

-NTC: Use an external NTC resistor to measure temperature. Typically the NTC is placed near output inductors.

-Integrated Tsense: Available if the power stage(s) provide an integrated temperature sense measurement

-Disable: Do not use the temperature function

Temp Offset:
Allow an offset to be entered to compensate for any measurement errors or offset due to location of temperature sensor.

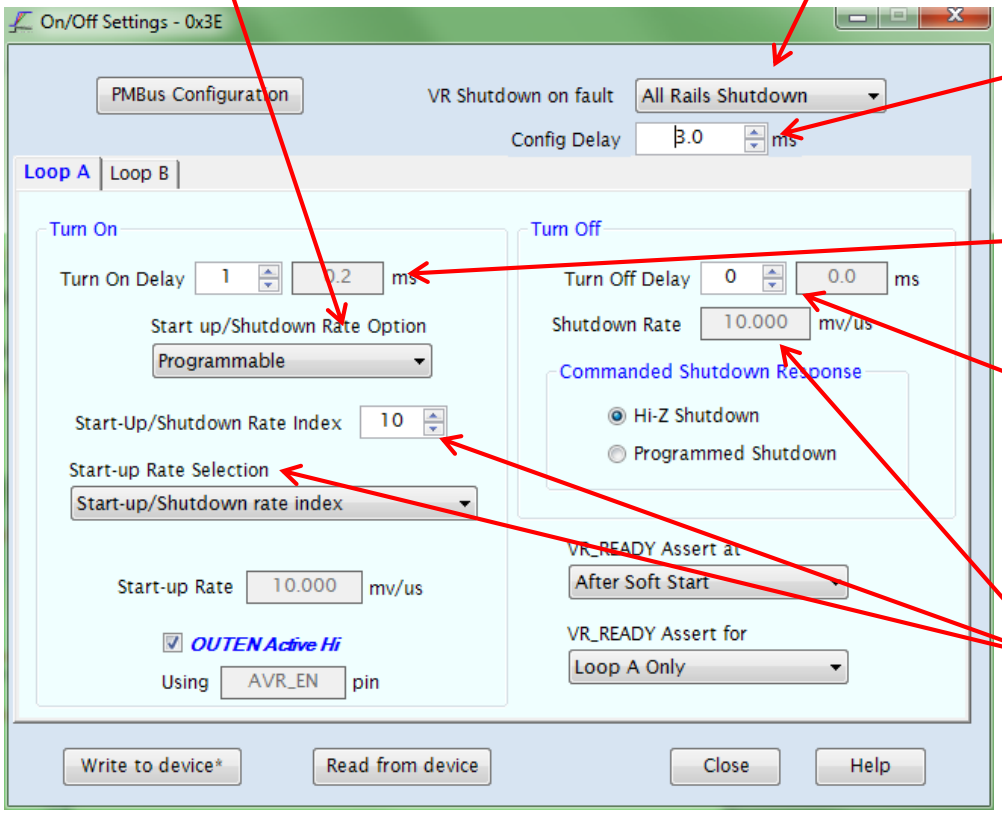
Agenda

On/Off Settings

Start-up Rate Option
–Controls the rate (mV/µs) of which the controller will ramp up VOUT to the desired **Vboot** voltage or the rate for shutdown if in Programmed Shutdown mode. Start-Up and Shutdown rate can differ from each other if so selected by **Start-up/shutdown rate selection**

VR Shutdown on Fault
–*All rails shutdown*: all rails will shutdown due to shutdown fault
–*Fault rails only*: only faulted rail(s) will shutdown due to shutdown fault

This also influence PMBus status reporting.



Config Delay
–This delay is introduced after the rising 3.3Volt supply passes UVLO to ensure the voltage completely settles
–After this delay, the VR will initialize the analog measurements which are sensitive to the integrity of 3.3Volt supply.

Typical set to 3.0

Turn On Delay
Time from Enable signal until Vout start to ramp up.

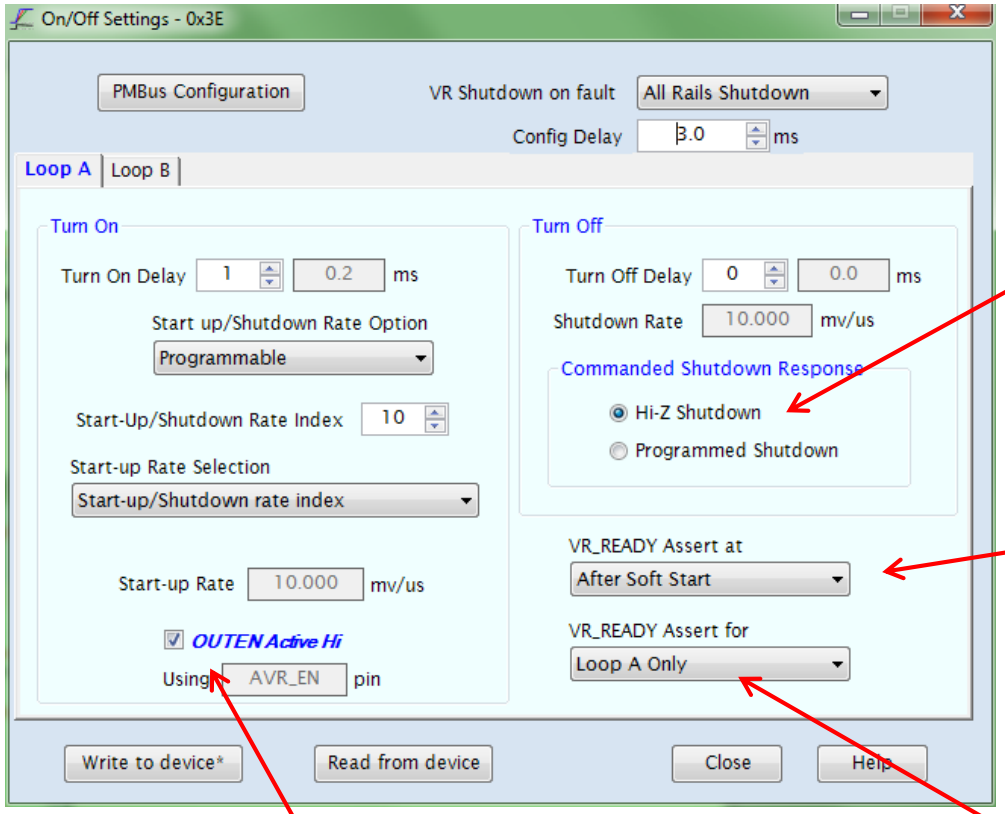
Turn Off Delay
Time from Enable signal goes away until Vout start fall.

Start-up/shutdown rate selection

Start up ramp can be selected to be equal to or slower than the ramp for Turn off. This is useful when powering up a large capacitor bank as the slew rate can be set lower to avoid too high peak currents

The selected slew rate in mV/us for up/down is displayed for information

On/Off Settings



Commanded Shutdown Response
–*Hi-Z Shutdown*: Forces both the HS and LS FETs to tri-state when the VR is turned off
–*Programmed Shutdown*: VOUT ramps down with the rate specified in the **Shutdown Rate**

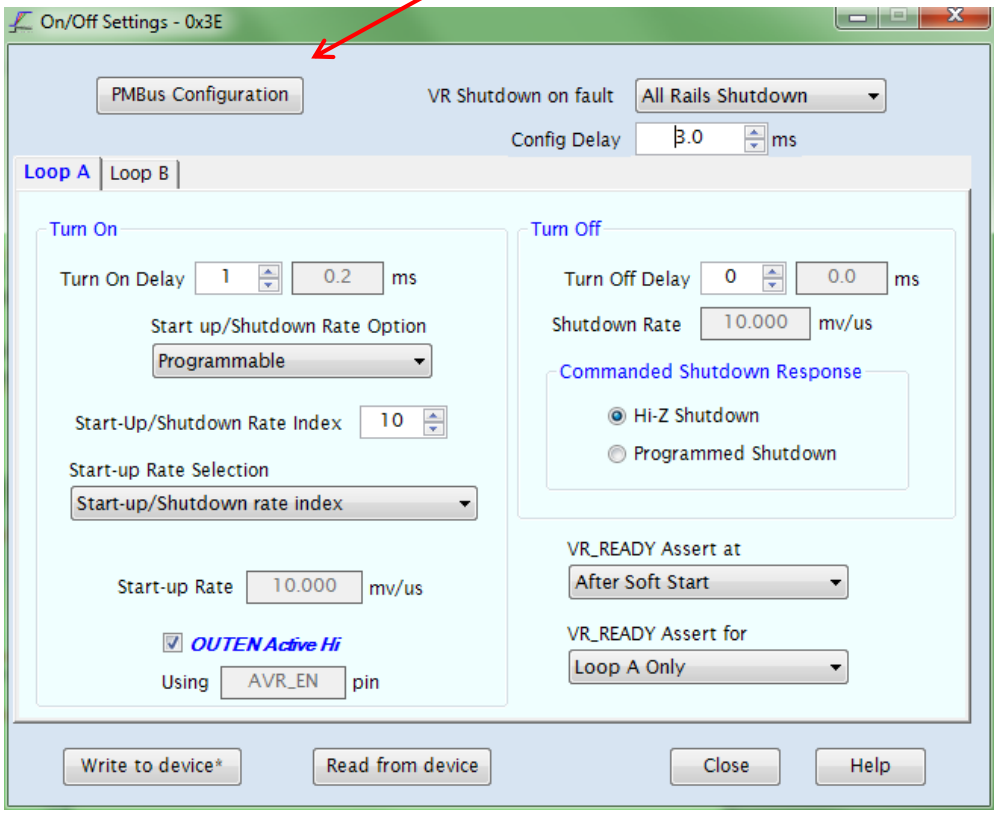
VR_READY Assert at
–*After Soft Start* – VR_READY is asserted after the soft start ramp to VBoot is complete. This is the appropriate setting for **VR13 application**.
–*Beginning of Soft Start* - VR_READY is asserted after VR_EN is asserted when the controller is ready to accept SVID commands. This is the appropriate setting for **IMVP8 applications**

OUTEN Active Hi
–*Checked*: Output is enabled when VR_EN is High
–*Unchecked*: Output is enabled when VR_EN is Low
The pin used for enable is shown for information

VR_READY Asserts for
–*Loop A only* – VR_READY pin assertion for Loop A only. This is the appropriate setting where loop independent VR_READY signals are needed.
–*All Active Loops* – VR_READY pin assertion for all active loops. This is the appropriate setting where there is only one VR_READY signal for multiple loops.

On/Off Settings

PMBus Configuration
When using PMBus there are additional on off settings possible.
Click this button to get to the PMBus page



Agenda

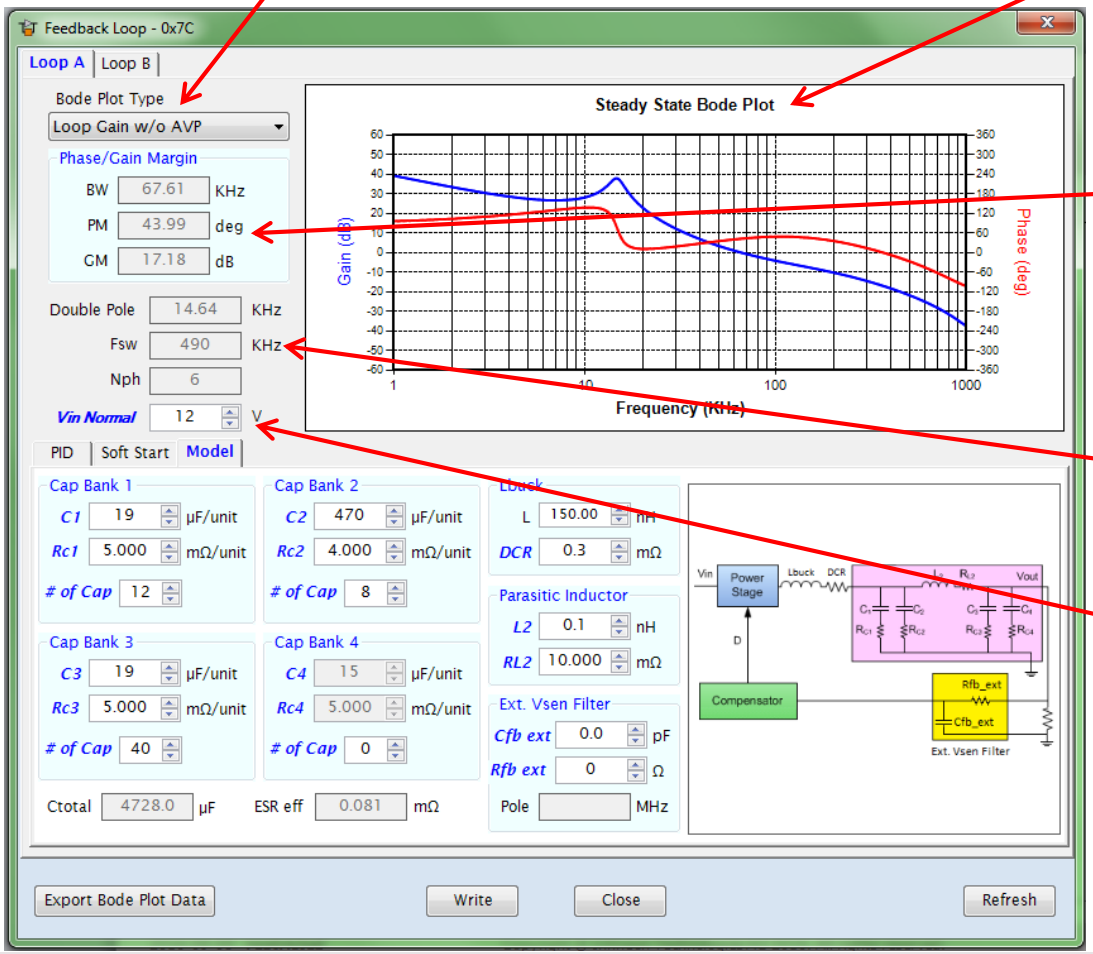
Feedback loop

Bode Plot Type:

Pull down menu where different types of Bode plots can be selected

Bode plot

Shown for the condition that is selected under the **Bode Plot Type** button



Phase /Gain Margin is calculated based on the parameters entered in **Model** tab

BW Bandwidth. Where gain passes 0dB

PM Phase Margin

GM Gain Margin

For Information these parameters are shown

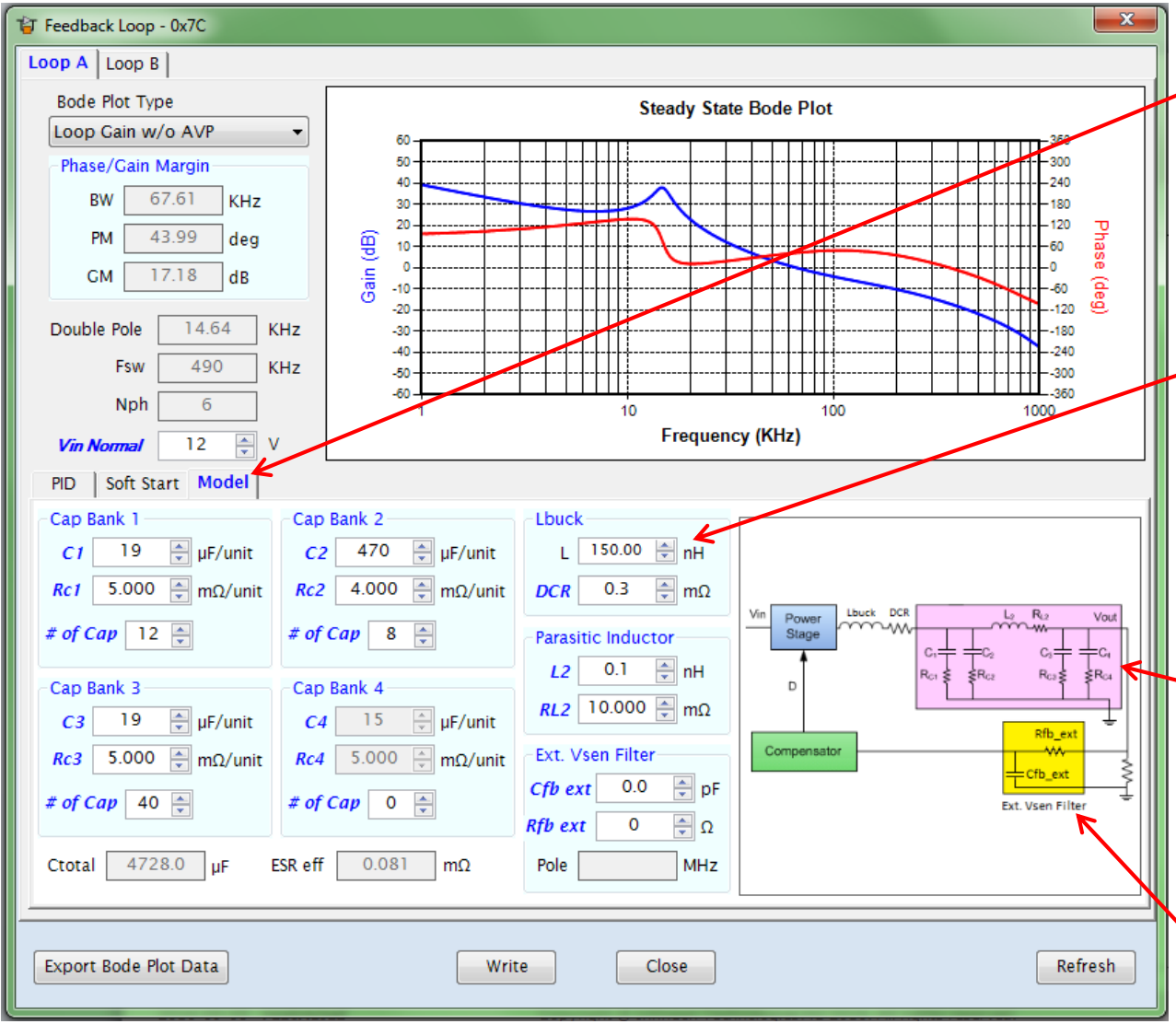
Double Pole: The pole due to output L and C

Fsw: Switching frequency

Nph: Number of phases

Input voltage: Used for calculations

Feedback loop Model



Recommend to start with the **Model** tab as Bode plot depends on Model being set up with what values used.

Any derating of Ceramic capacitors due to voltage must be considered before entering Capacitor values.

Lbuck:

Here the Inductor value is entered. This Inductance value is saved in a register inside the controller and important to set correct for calculations to be right.

Other L and C related values on this page is used by GUI only for Bode plot and simulations. They are not saved in controller

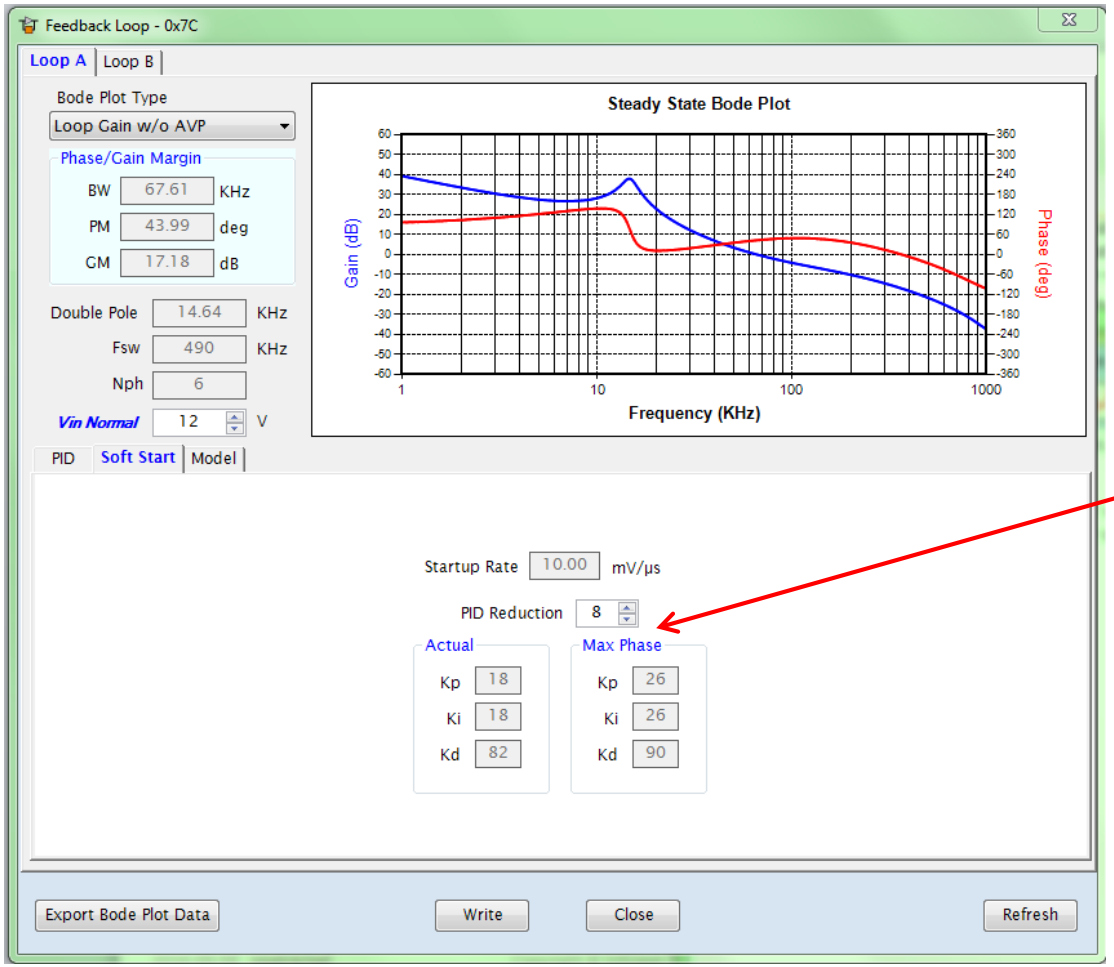
Model simulates a CPU in a socket. Cap bank 1 and 2 are MLCC and bulk capacitors after inductors. Bank 3 and 4 are MLCC capacitors inside the socket.

Parasitic inductor L2 and R_{L2} simulate the impedance of the copper traces into the socket

Ext Vsen Filter:

Simulates any resistance and capacitance in the feedback path. i.e. a 10ohm resistor that is used to inject signals for Bode measurements

Feedback loop Soft Start



Slew rate is for information and can be selected in another place.

During softstart the PID values can be reduced to slower settings.

They do not need to be as fast responding during soft start as during normal operation.

i.e. Not the same big transients to handle.

The lower settings allow a smoother monotonic ramp of Vout

PID compensation can be optimized during soft start.

Startup Rate

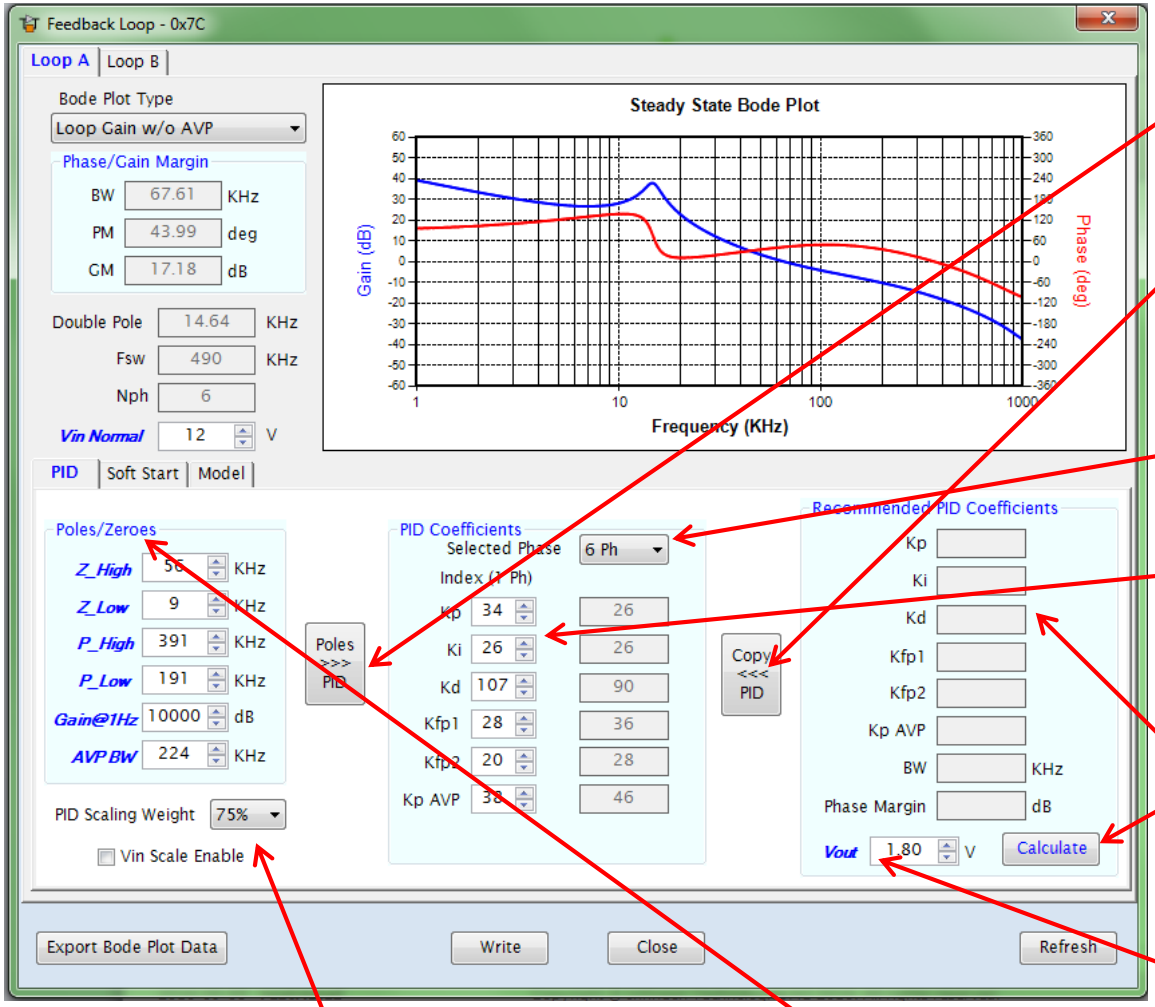
–Effective startup ramp rate

–The startup rate can be changed in the On/Off Settings dialog

PID Coefficients

–During start up: adjust the voltage feedback loop compensation during the initial start up period only

Feedback loop PID



Poles >>> PID button

Poles / Zeros can be converted to **PID Coefficients** by clicking this button

Copy <<< PID button: copies **Recommended PID Coefficients** to the **PID Coefficients**

Selected Phase: For information the PID coefficients for different number of phases can be shown for information.

PID Coefficients: the coefficients can be entered directly or calculated by the GUI using the buttons.

Recommended PID Coefficients

GUI can calculate a set of recommended coefficients

- **Calculate button**: displays the calculated PID coefficients based on the entered values in the **Model** tab, **Vin** and **Vout**

Vout: Output voltage Used for internal calculations of PID in the GUI

PID Scaling Weight
Vin Scale Enable See following slides for explanation. Typical setting 75%

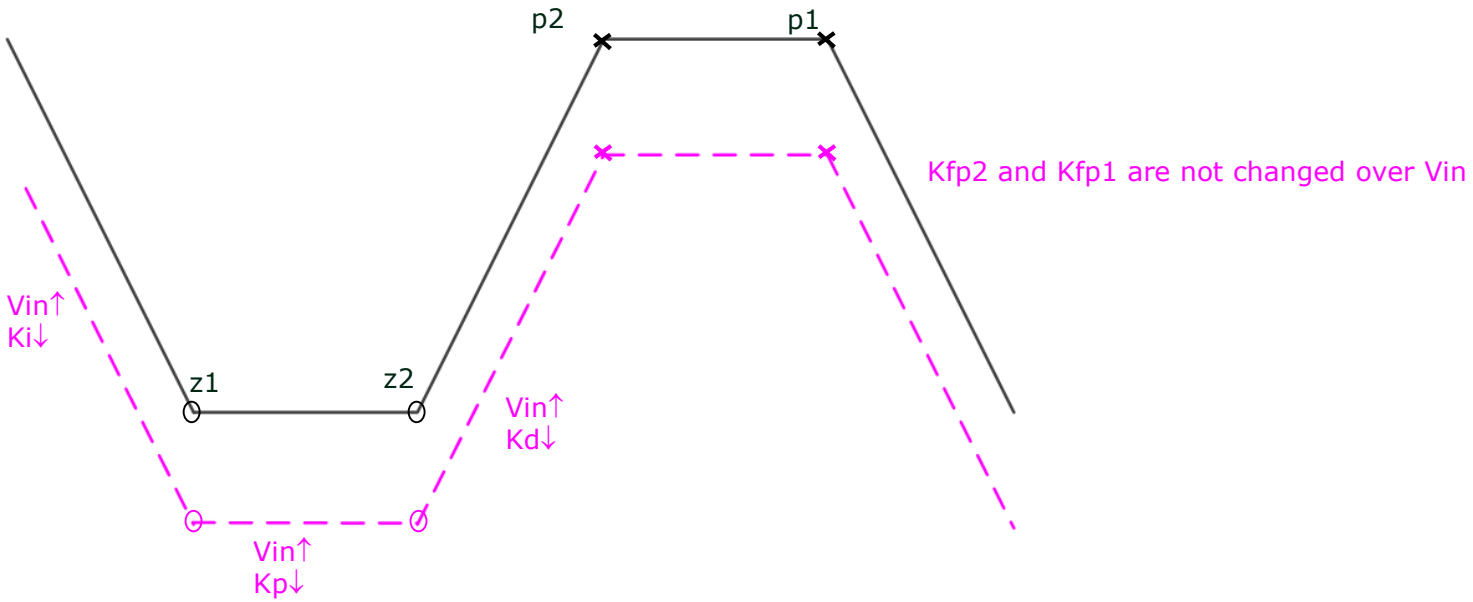
Poles / Zeros

Enter the parameters for the desired Poles and Zeros. GUI can convert this to PID coefficients

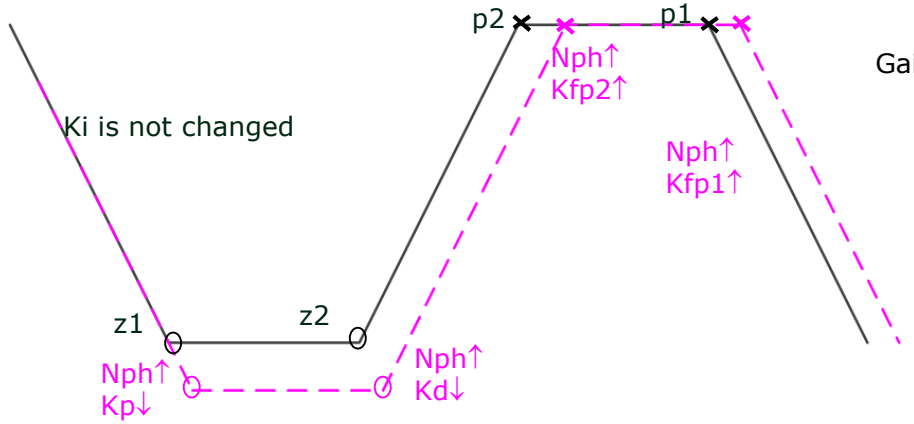
Vin scaled PID

- Kp, Ki, Kd can be programmed to be scaled over Vin to
  - Maintain the same zeros and poles location
  - Keep the same gain

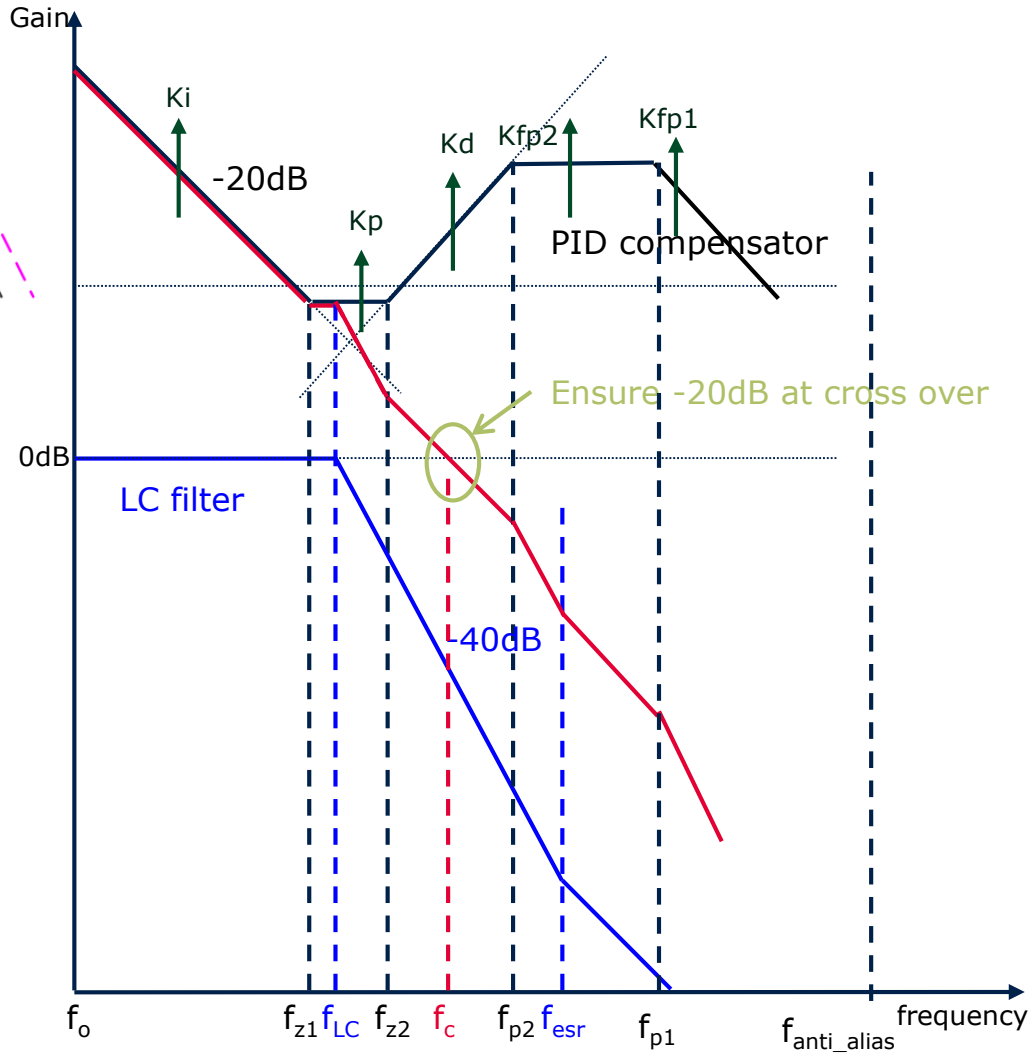
  Note: Kfp2, Kfp1 and Kp(avp) are unchanged over Vin



PID scaling over Nph change (1 of 2)



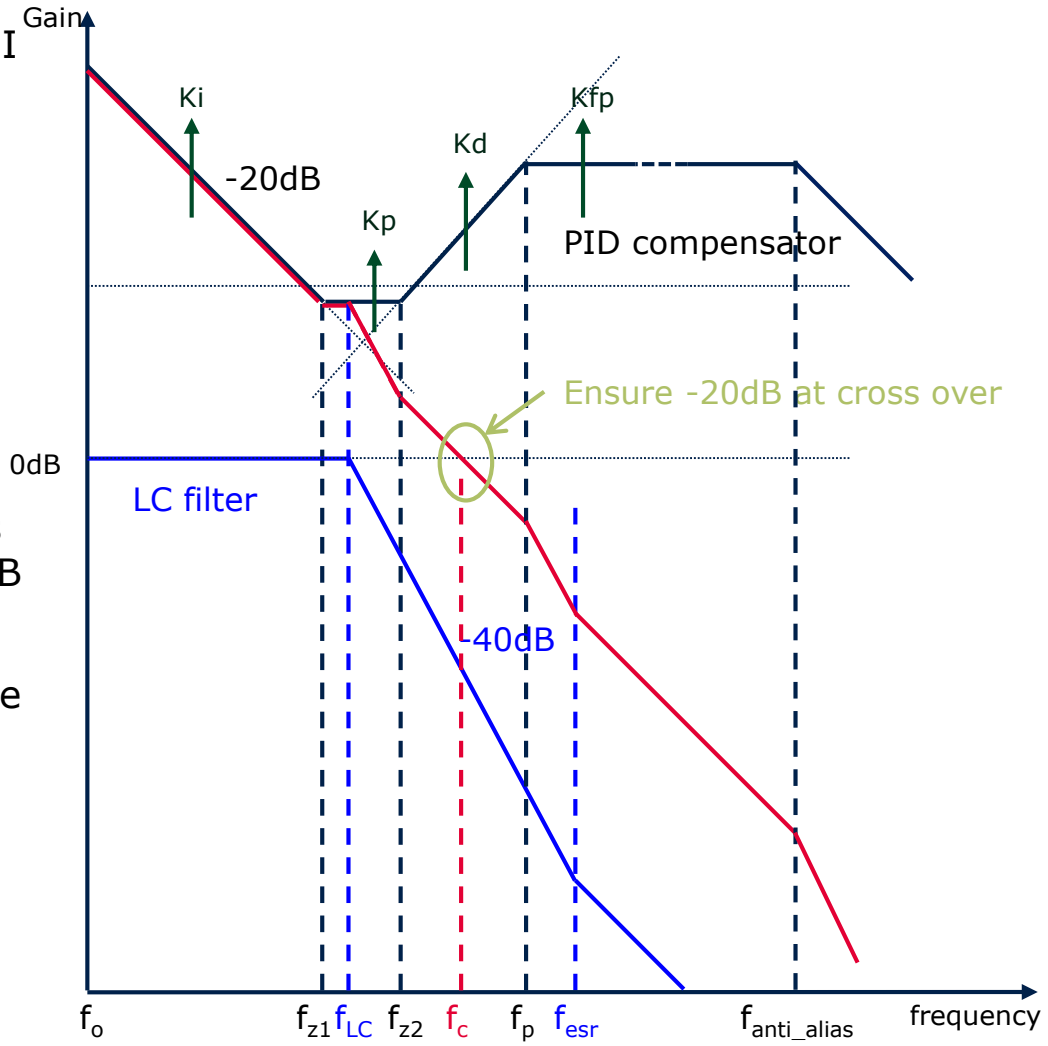
- Kp, Kd, Kfp2, Kfp1 and Kpavp will be scaled automatically as the Nph is being added or dropped. Note: Ki is not changed
- As Nph is increasing
  - Kp, Kd is decreasing
  - Kfp2, Kfp1, Kpavp is increasing
- Change of Kd is proportional to Nph and Kp, Kfp2, Kfp1 and Kpavp are proportional to square root of Nph
- z1, z2, p2, p1 are moved to the higher frequency when Nph is increasing because double pole location is moved to higher frequency



Feedback Loop PID: Compensator – Steady State (Voltage Loop)

PID coefficients

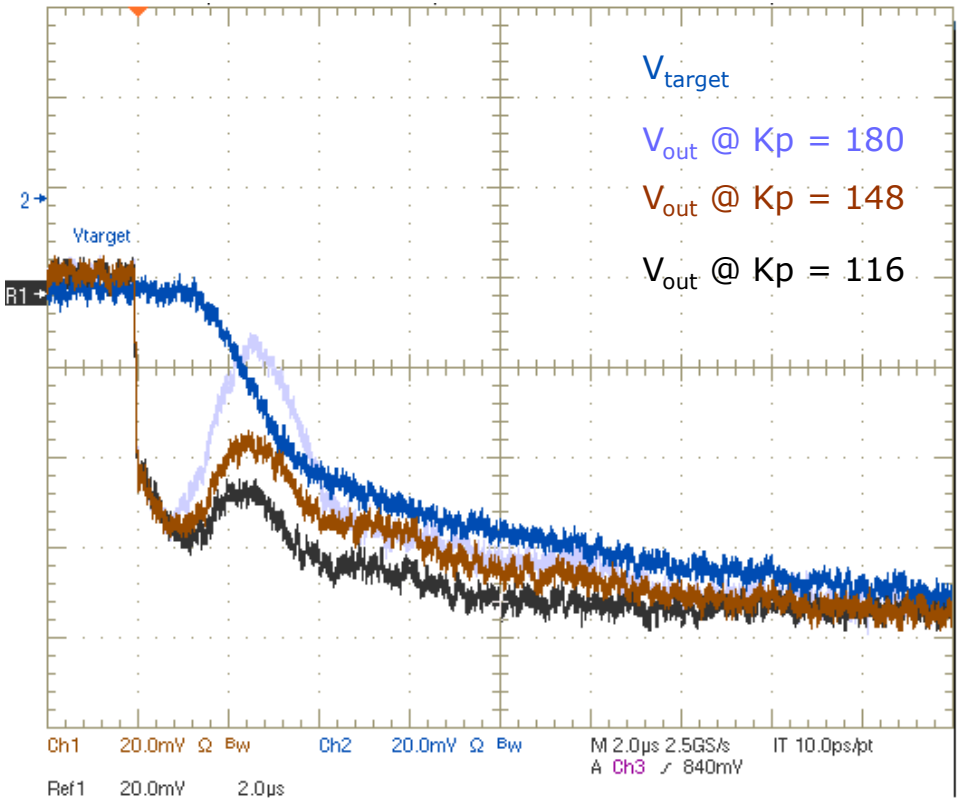
- PID compensator: similar to Type III compensator
  - f_{z1}: 1st zero of PID compensator (Ki and Kp intersection)
  - f_{z2}: 2nd zero of PID compensator (Kp and Kd intersection)
  - f_o: pole at origin (Ki)
  - f_p: high frequency pole (Kd and Kfp intersection)
  - f_{anti_alias}: high frequency anti-alias pole @ around 10MHz for LoopA/B
  - LC filter:
    - f_{LC}: output LC filter double pole
    - f_{esr}: ESR zero of C_{out}

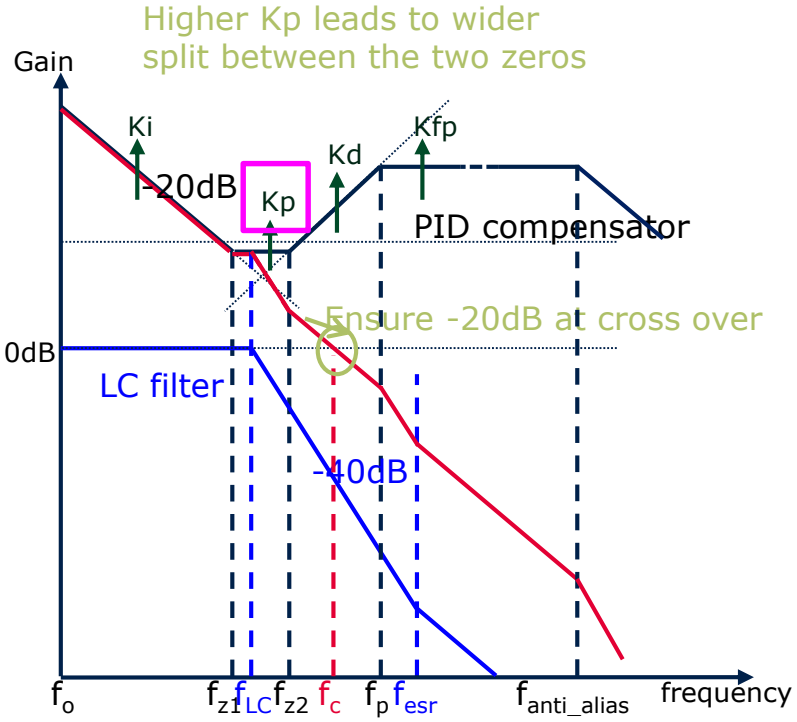


Feedback Loop PID: Recommendations for Designing a Stable Voltage Feedback Loop

- The first zero should be placed on the left side of the LC filter's double poles, and the second zero placed on the right side of the double poles
- The cross-over frequency (fc) or bandwidth (BW) should not exceed 1/4 of the switching frequency
- The Gain should cross the 0dB threshold with a slope of -20dB /dec
- **Kp**/**Ki**/**Kd**/**Kfp** values are larger for lower phase-count than that for higher phase-count
- PID coefficients are non-linear. Coefficient index delta of 32 is equivalent to 6dB change in gain
- **Kp(AVP)** should be smaller for VR's where a large DC load-line setting is required

Feedback Loop PID: Steady State Voltage Loop Compensation Kp impact on transient

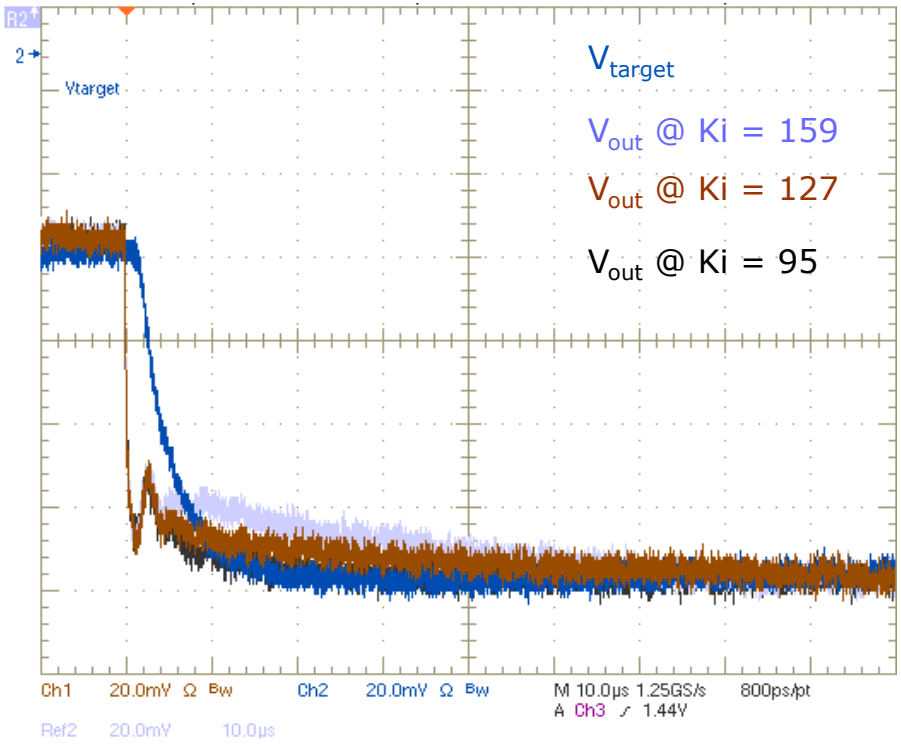


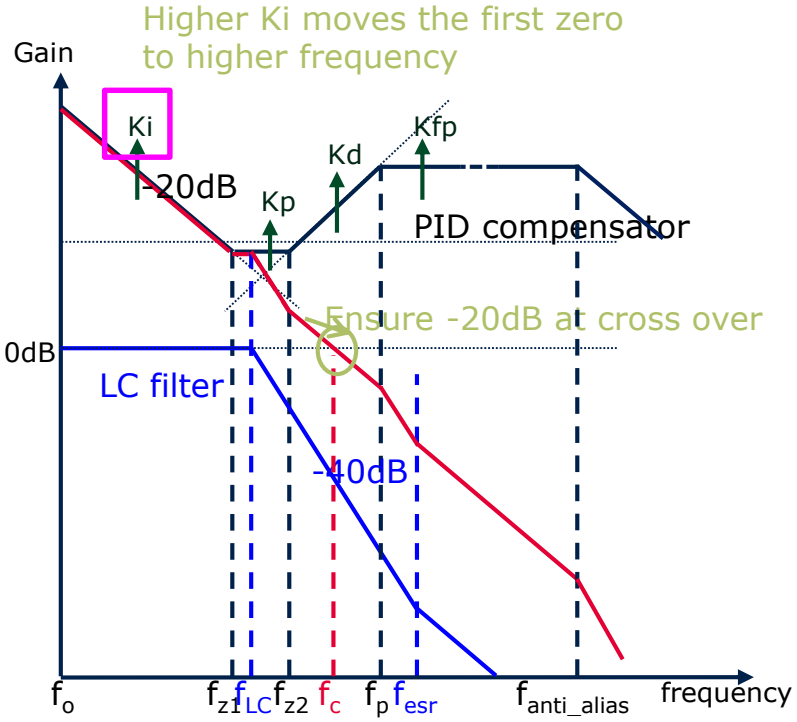


- P term is proportional to Verr. The higher the **Kp** the higher the BW, but the higher the ring back
- From the time domain transient response:
  - **Kp** mainly affects the first ring back amplitude
  - **Kp** has some impact on first undershoot beyond 100ns of load stepping

Note: **Kp** affects the transient response within the first 5us

Feedback Loop PID: Steady State Voltage Loop Compensation Ki impact on transient

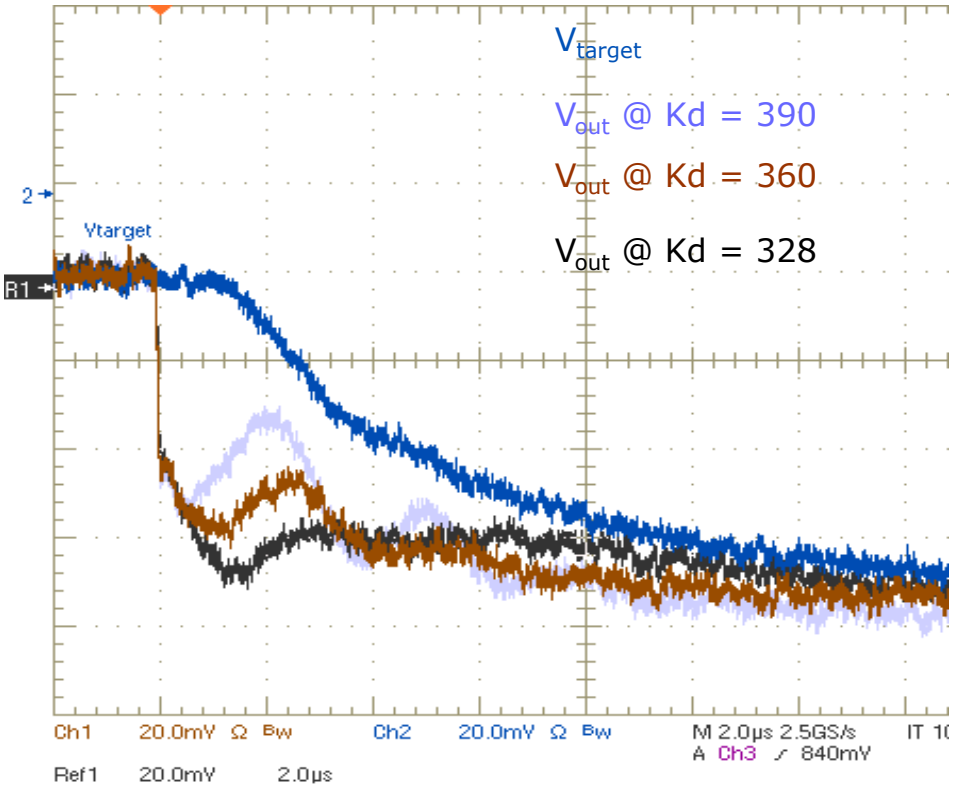


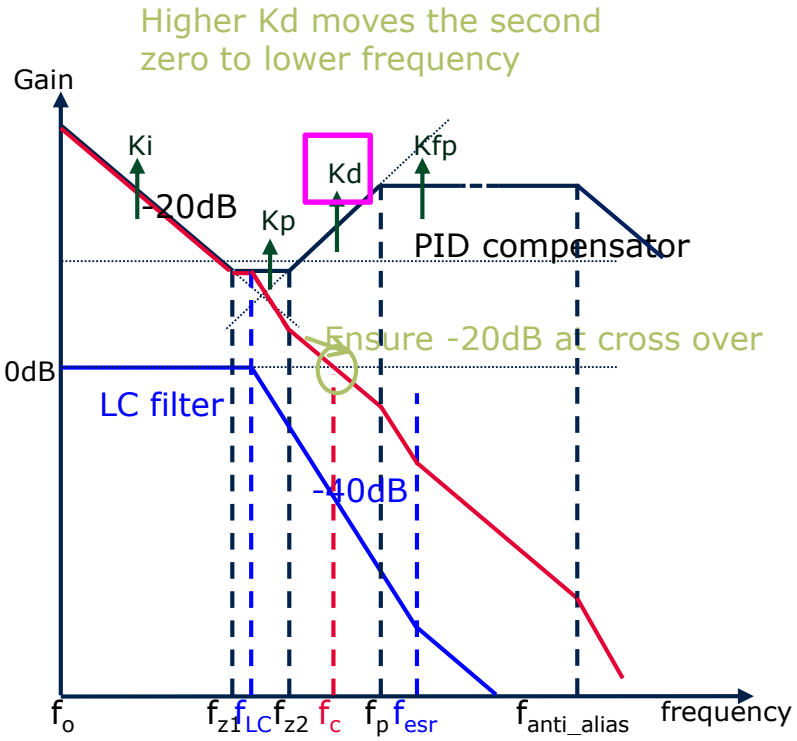


- I is the integral term used to drive the DC value of Verr to zero
- From the time domain transient response, **Ki** mainly affects:
  - The settling trend of V_{OUT} after the initial transient response
  - If **Ki** is too high, V_{OUT} overshoots V_{target} in the highlighted region
  - If **Ki** is too low, V_{OUT} may lag V_{target} in the highlighted region can cause extra undershoot

Note: **Ki** affects the transient response after the initial 10us to 40us

Feedback Loop PID: Steady State Voltage Loop Compensation Kd impact on transient

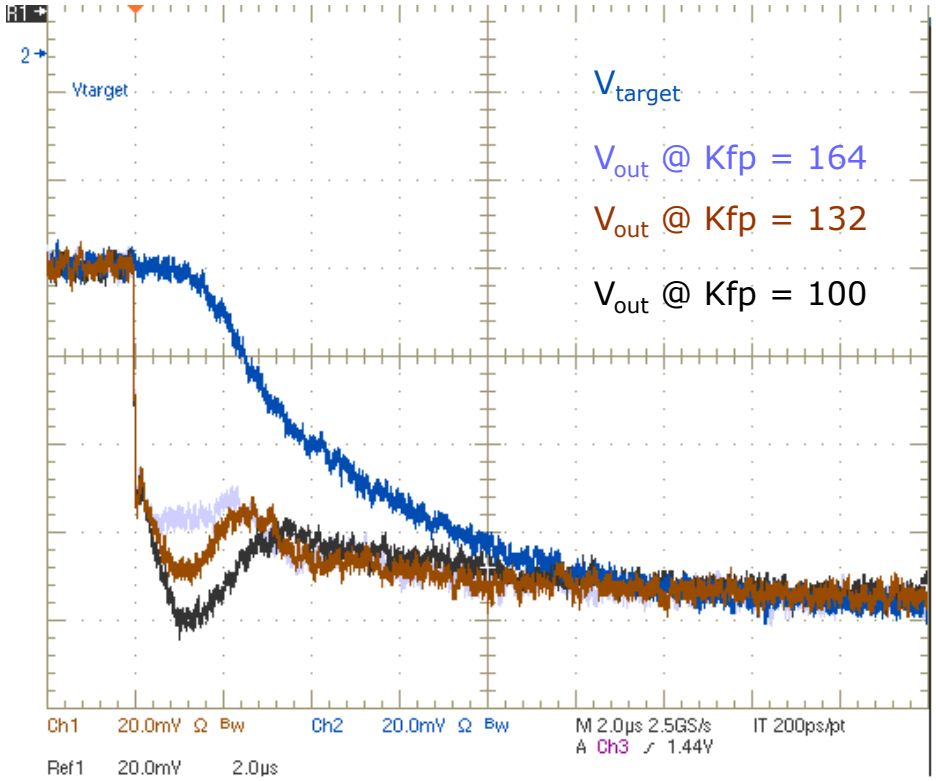


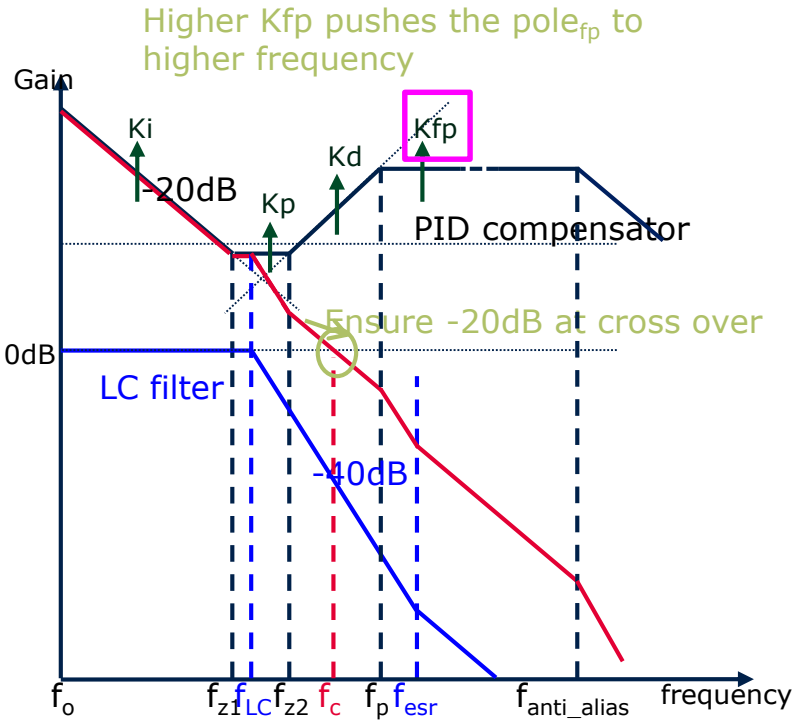


- D is the derivative term. The higher the Kd, the higher the BW but with less phase margin
- From the time domain transient response, **Kd** mainly affects:
  - The first undershoot beyond the 100ns of load stepping. The higher the **Kd**, the less the undershoot
  - But too high of **Kd** will cause V_{OUT} ringing due to insufficient phase margin

Note: **Kd** affects the transient response within the first 5us

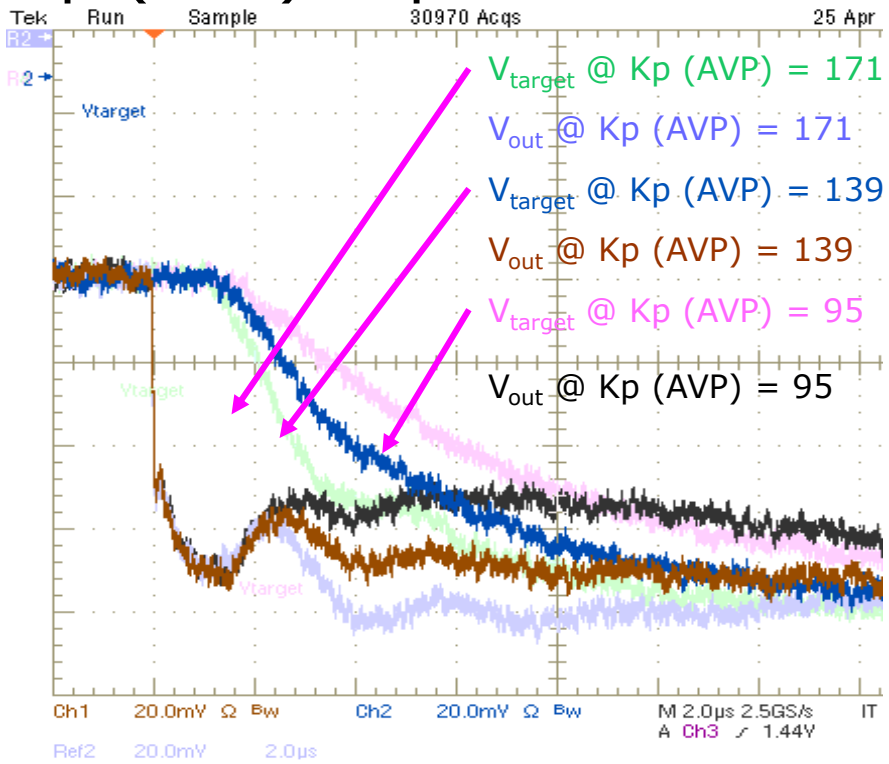
Feedback Loop PID: Steady State Voltage Loop Compensation Kfp impact on transient





- **Kfp** provides a high frequency pole to roll off the gain introduced by the P and D terms. If **Kfp** is too high, the D term gain at high frequency will not be attenuated and hence results in less phase margin
- From the time domain transient response, **Kfp** mainly affects:
  - The first undershoot beyond the 100ns of load stepping. The higher the **Kfp**, the less the undershoot
  - But if **Kfp** is too high it will lead to V_{OUT} ringing due to insufficient phase margin

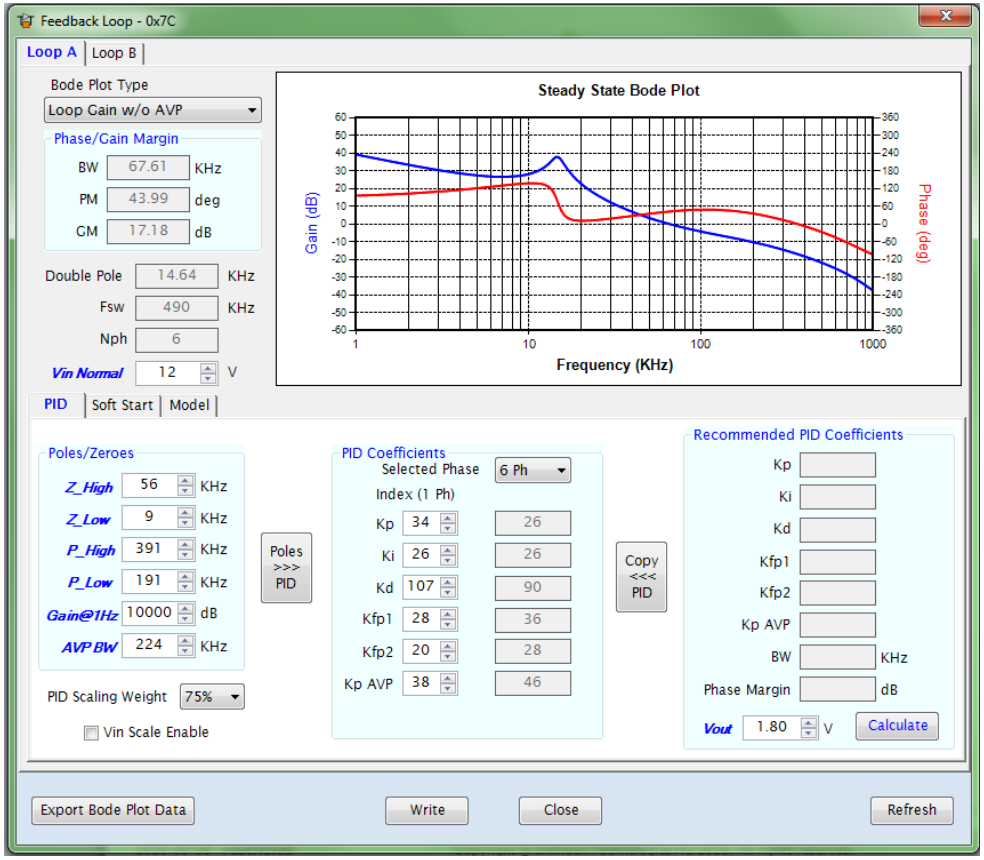
Feedback Loop PID: Steady State Voltage Loop Compensation Kp (AVP) impact on transient

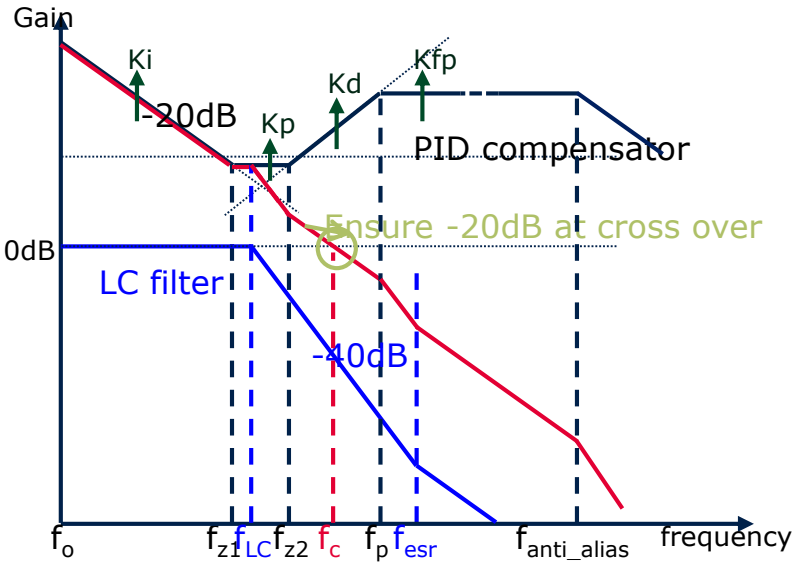


- **Kp(AVP)** is the low pass filter of the AVP loop.
- From the time domain transient response, **Kp(AVP)** mainly affects:
  - how fast the target voltage can track the changing inductor current during transient conditions
  - If **Kp(AVP)** is too low, V_{OUT} will take longer to settle to the final DC target
  - The higher the **Kp(AVP)** , the higher the AVP loop BW, and it may overlap with the voltage loop to induce extra undershoot or ringing at V_{OUT}

Note: **Kp(AVP)** affects the transient response in 5us to 20us

Feedback Loop PID: Compensator – Steady State (Voltage Loop)



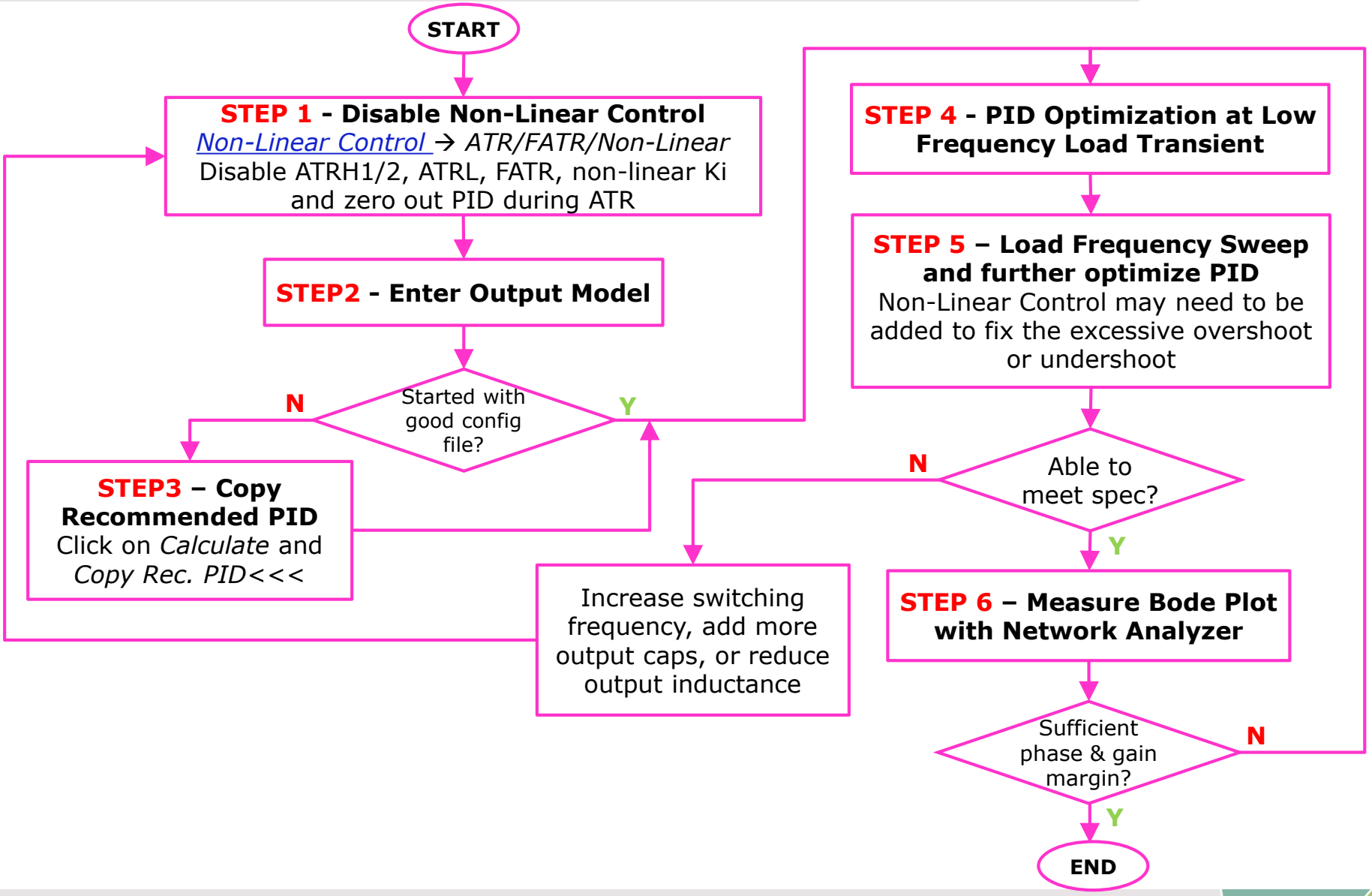


Poles/Zeroes

- **Z1**: first zero at f_{Z1}
- **Z2**: Second zero at f_{Z2}
- **P_Low**: pole at fp
- **P_High**: pole at f_{anti_alias}
- **Gain @ 1Hz**: DC gain
- **AVP BW**: AVP bandwidth
- **Poles>>>PID button**: calculates and populates the desired PID coefficients based on Poles and Zeros information entered

Agenda

Voltage Loop Compensation Procedure



Agenda

Nonlinear Control...

The following parameters can be programmed in the **Nonlinear Control** dialog:

- Active Transient Response (ATR) parameters to reduce undershoot or overshoot excursions during transient load events
- Frequency Active Transient Response (FATR) parameters to improve transient response over output load frequency, especially for transient loads at beat frequency
- Dynamic VID (DVID) parameters to optimize the VR's response to the SetVID_Fast/Slow/Decay commands
- Non-Linear parameters to gain more undershoot or overshoot margin at high load repetition frequency
- Feed forward parameters to gain faster response during the specific cases listed below or variable case as below

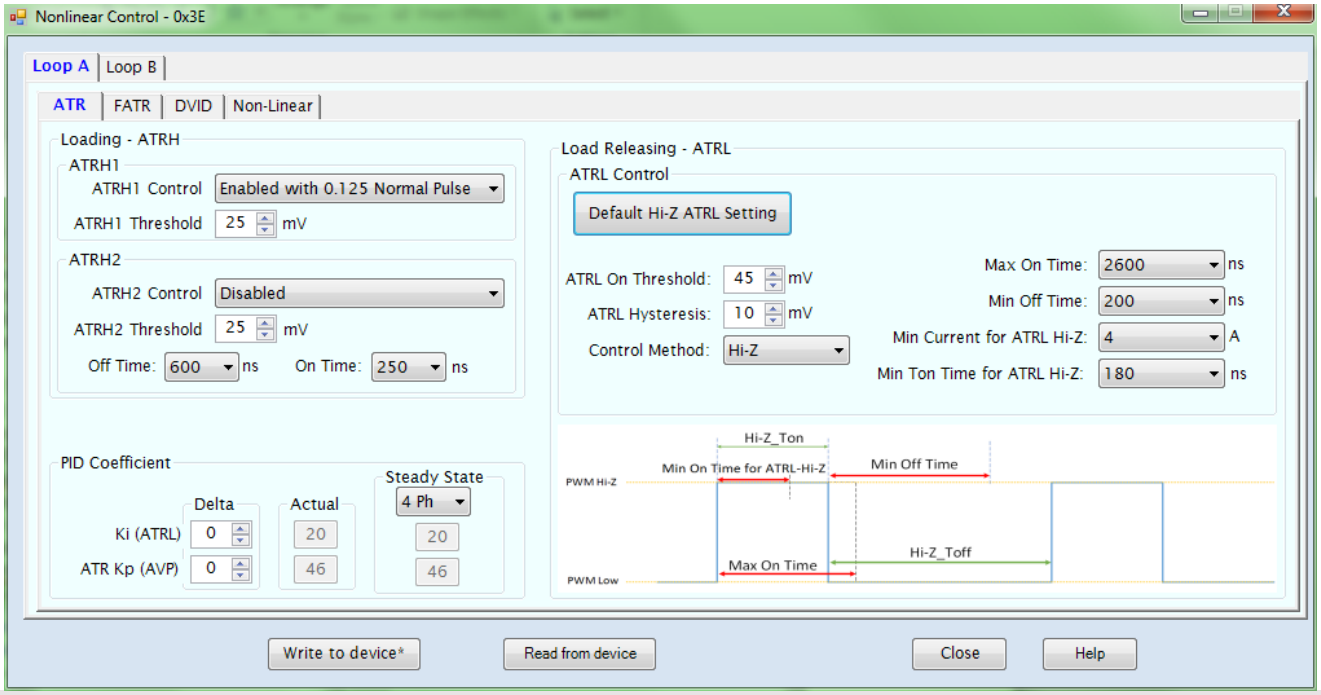
Only enable the ATR functions if adjusting PID alone can not meet the undershoot and overshoot requirements

–ATR control mechanisms are driven by comparators and programmable thresholds

–The response is non-linear and may add jitter at the output

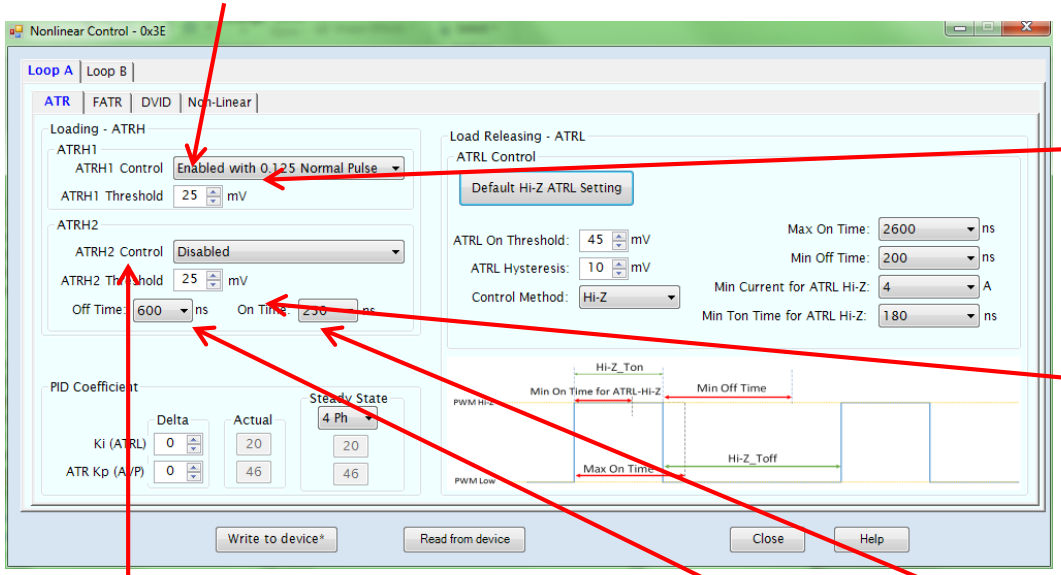
– The thresholds should be at least 5mV (typically 10mV) wider than the measured steady state ripple voltage

– If ATR has to be enable, the PID should be made less aggressive ☐ start by adjusting(lower) Kd and Kfp terms



Nonlinear Control... ATR

ATRH1 Control
–Use to program the strength of the ATRH1 control
–A wider pulse width corresponds to a stronger ATRH1 control
–Disable: No ATRH1 control
–Enabled with 0.50/0.375/0.25/0.125 Normal Pulse: ATRH1 control is enabled. The normal pulse width is decided by the feedback loop control and ATRH1 will be fired in 0.50/0.375/0.25/0.125 normal pulse width
–Recommended starting point is 0.25 of normal pulse if ATRH1 is needed. Stronger ATRH control reduces the undershoot of VOUT but will increase ring-back.



ATRH1 Threshold
–ATRH1 control threshold
–The smaller the threshold, the stronger the ATRH1 response because of the increased likelihood that ATRH1 will be triggered
–It is recommended that the threshold not be too close to the steady-state ripple size, otherwise ATRH pulses can be falsely fired during normal regulation. Select a threshold at least 10mV higher than measured VOUT switching ripple.

ATRH2 Threshold–ATRH2 control threshold
–Similar to ATRH1 Threshold
– Recommended to set > ATRH1 Threshold

On Time
–On time (PWM high duration) of the ATRH2 pulse when ATRH2 Control is set to Enabled with Pulse Control
–If ATRH2 On time is too narrow, it could be swallowed by the driver and then provide little or no help in reducing undershoot
-If ATRH2 On time is too large, it could saturate output inductor. It can also make the PWM width too wide and be limited by the maximum duty cycle setting.
-Select ATRH2 pulse in the range of 100ns to 200ns and select a much longer Off time (>800ns) for robust ATRH2 behavior

ATRH2 Control . Only use if ATRH1 is not enough.

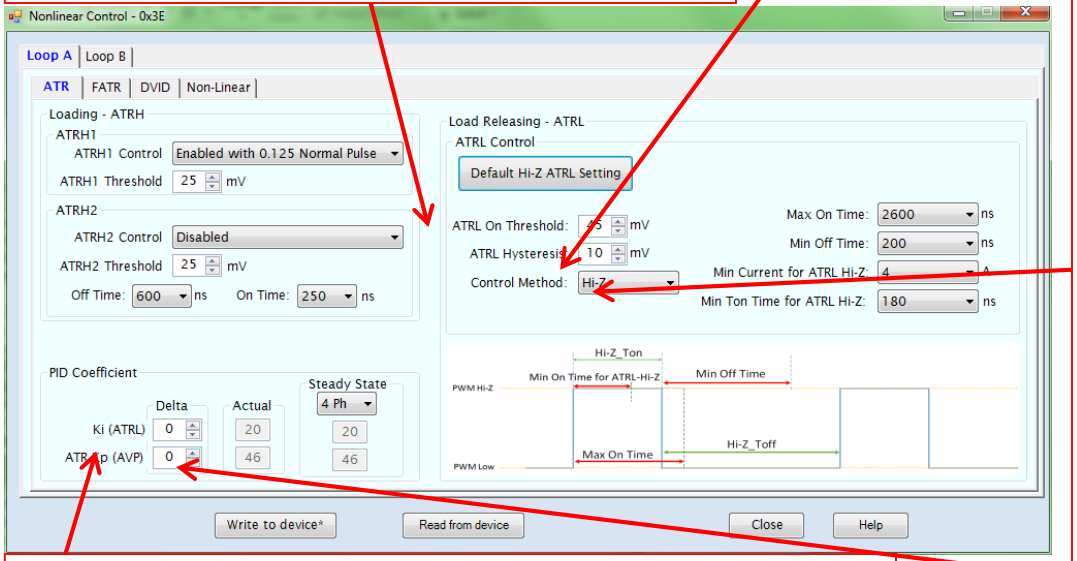
–Disabled: no ATRH2 control,
–Enabled with Pulse Control: ATRH2 pulse width is programmed by the Off Time and On Time

Off Time
–Off time (PWM low duration) of the ATRH2 pulse when ATRH2 Control is set to Enabled with Pulse Control

Nonlinear Control... ATR

ATRL On Threshold
–ATRL will be engaged if the VOUT overshoot exceeds the target VOUT plus this threshold
–Recommended not to set smaller than the switching ripple amplitude, otherwise it will be falsely fired in the steady state

ATRL On Hysteresis
–Prevents ATRL window chattering and hence stressing FET drivers
–Recommended value is 10mV



Control Method
–Disabled: Disable ATRL
–Hi-Z: Low side FET is off, uses Body diode
- Low side on: FET turns on when ATRL window is active
–Recommended to be in Hi-Z if ATRL needs to be enabled

•When both high side FET and low side FET are off, the positive current will go through the low side body diode
•Compared to the path through low side FET, the low side body diode will cause a larger voltage drop across the low side FET and be able to reduce the positive inductor current sooner, thereby more effectively reduce the overshoot

Ki (ATRL)
–Delta: This will reduce Ki when the ATRL window is active regardless of ATRL function is enabled/disabled. When the ATRL window is active, less error Voltage signal will be accumulated by the integrator which allows the average VOUT to be shifted up during high frequency transients that relieves some stress on meeting the undershoot specifications.
–Actual: Calculated value based on the Delta and Steady State
–Steady State: Steady state Ki value for different number of phases

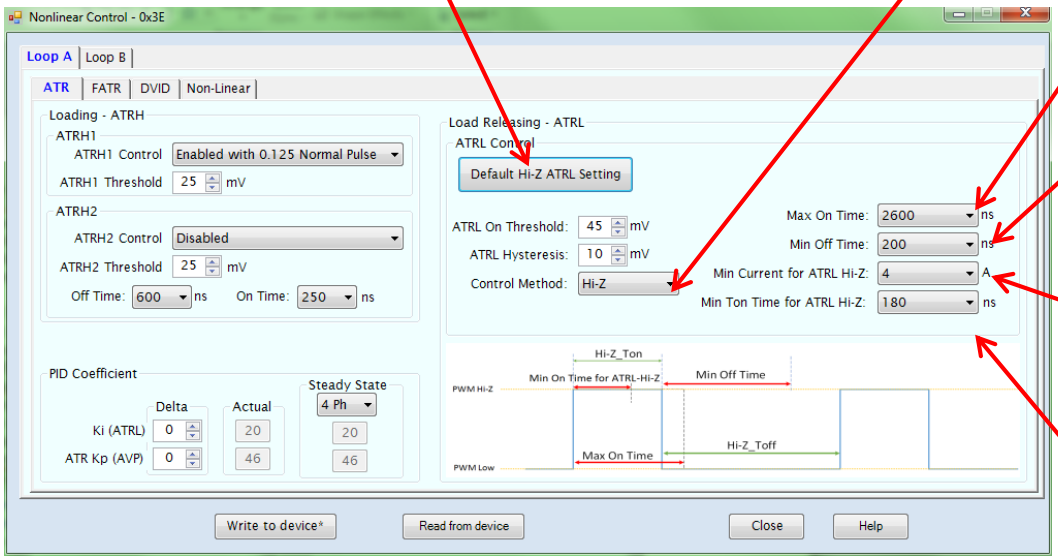
ATR Kp (AVP)*
–Delta: Kp(avp) index when ATR is detected
–Actual: Calculated value based on the Delta and Steady State
–Steady State: Steady state Kp value for different number of phases

Nonlinear Control... ATR

Default Hi-Z ATRL setting
Set all the ATRL parameters to a default setting with Hi_Z response

Control Method
–Disabled: Disable ATRL
–Hi-Z:Low side FET is off, uses Body diode
-Low side on: FET turns on when ATRL is active

–Recommended to be in Hi-Z if ATRL needs to be enabled. See description on following slides



Max Off Time
–Maximum PWM Hi-Z duration in ATRL Hi-Z control mode when the ATRL window is active

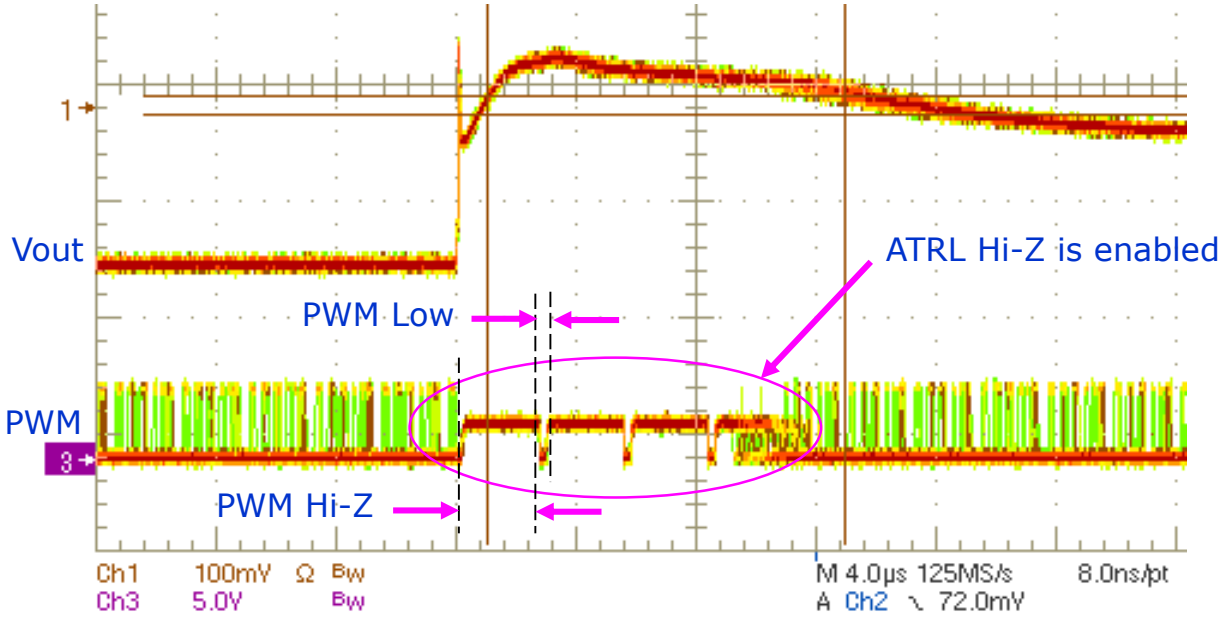
Min Off Time
–Minimum PWM low duration in ATRL Hi-Z control mode when the ATRL window is active

Min Current for ATRL Hi-Z
–Minimum current in ATRL Hi-Z control mode when the ATRL window is active. If the current (per phase) is lower the setting here, the ATRL control mode will become "Low Side ON" See next page for more details

Min Ton Time for ATRL Hi-Z
–Minimum PWM Hi-Z duration in ATRL Hi-Z control mode when the ATRL window is active

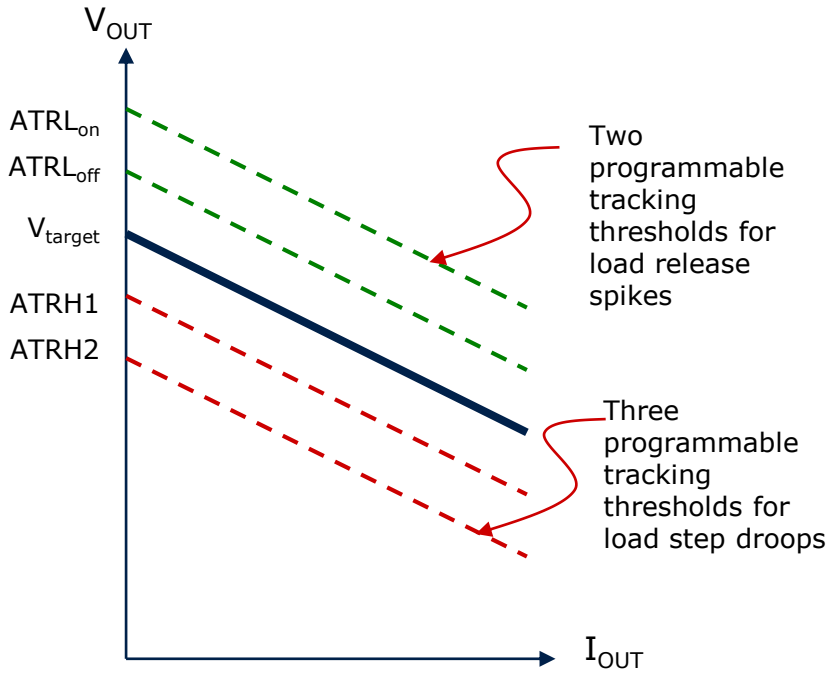
Nonlinear Control... ATR

- **Min Current for ATRL Hi-Z**
- –When the phase current is lower than the setting specified here, the ATRL behavior will be changed from Hi-Z to LSFET on
- –Minimum positive inductor required to sustain Hi-Z state during ATRL
- –When the inductor current falls below this threshold, the low side FET will turn on to continuously discharge the output cap



Nonlinear Control: ATR Overview

- Active Transient Response (ATR) is used to reduce undershoot or overshoot excursions during transient load events
  - ATR**H**: Actively inserts additional pulses (PWM **H**igh pulses) on each phase to minimize undershoot during load step conditions
  - ATR**L**: Actively turns on the low side FET(s) (PWM **L**ow pulses) or forces PWM into tri-state so that the inductor current can go through the low side body diode during load release conditions
- ATR**H** threshold: ATRH will be fired when the droop caused by the load step is above the programmed threshold
  - ATRH1/2 programmable thresholds
- ATR**L** threshold: ATRL will be fired when either of the 2 programmable tracking thresholds are entered during load release spikes
  - ATRLon
  - ATRLoff = ATRLon Hysteresis



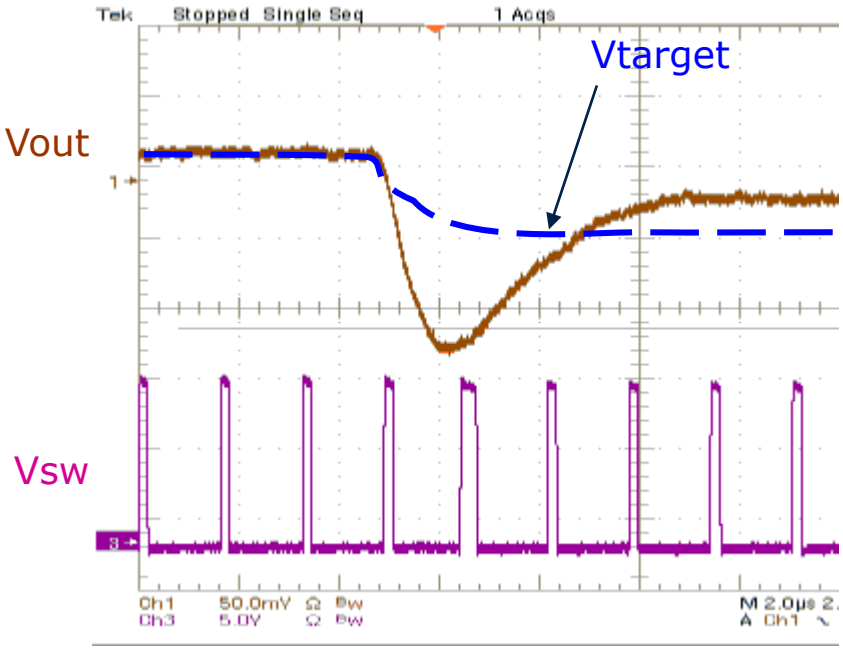
Nonlinear Control: ATRH

- ATRH – undershoot detector
  - Use during positive load steps to enable the additional PWM pulses on top of the regular scheduled PWM pulses controlled by the PID
    - This adds pulses to one or more phases to reduce the V_{OUT} undershoot
  - When V_{OUT} is below the ATRH threshold, the corresponding ATRH window will be activated
  - The firing of ATRH pulses between phases are “scheduled” to prevent inductor saturation
    - The pulse width of the ATRH pulses is controlled by a combination of the PID and the programmable on/off time durations

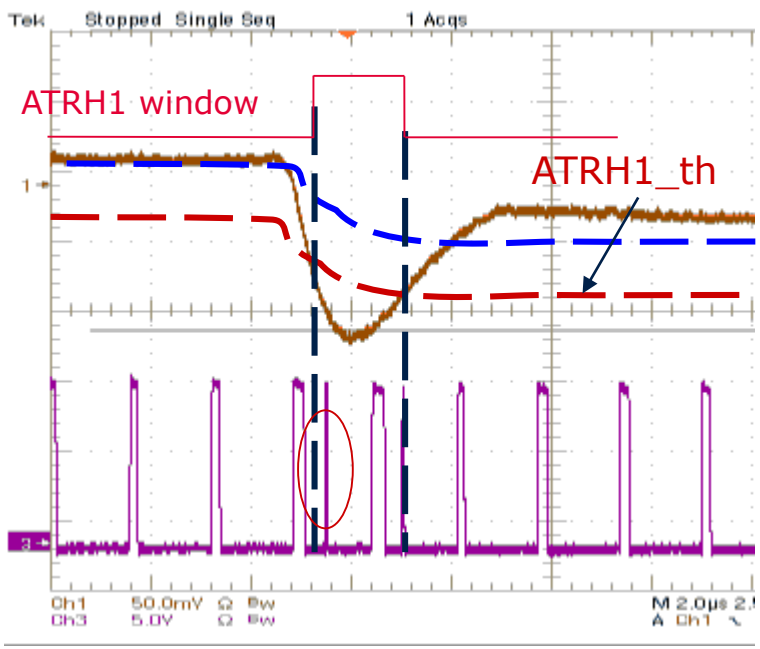
Nonlinear Control: ATRH

- When the load undergoes a positive step (increased load current), V_{OUT} droops
- When V_{OUT} < ATRH_th, the controller will fire extra PWM pulses to reduce undershoot
  - The ATRH_th is equal to target voltage minus ATRH threshold

w/o ATRH



with ATRH



Nonlinear Control: ATRL

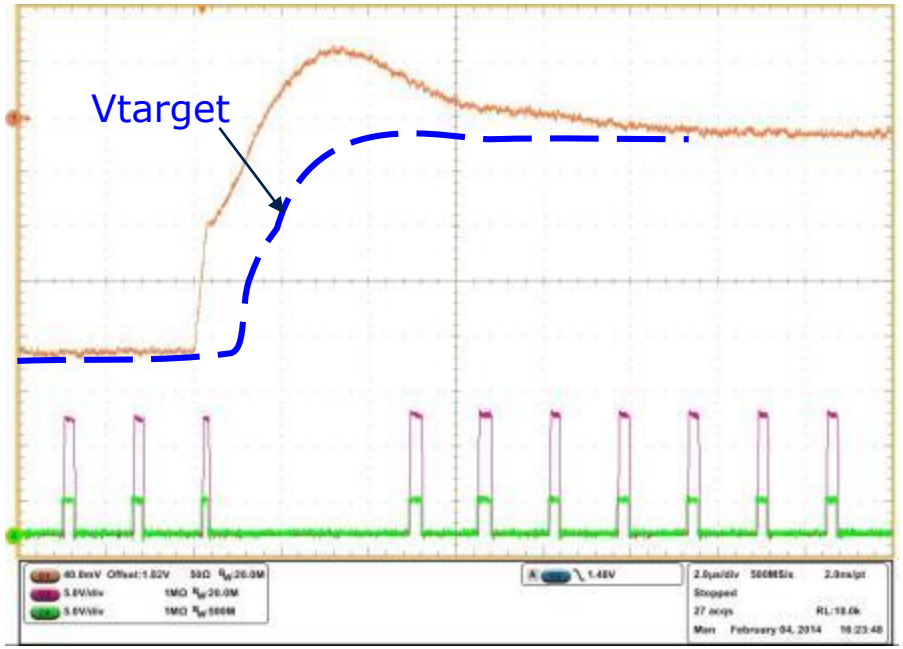
- ATRL – overshoot detector
  - Use during negative load step (load current release) to quickly bring the PWM outputs to a Hi-Z or Low state (depending on what the programmed action is)
    - This turns off the power stage in Hi-Z mode letting current flow through the Body diode to dissipate the energy.
    - Or when in Low Side On mode turns on the low side FET

    to reduce the V_{OUT} overshoot
  - When V_{OUT} is above the ATRLon threshold, the ATRL window will be activated and deactivates once V_{OUT} drops below ATRLoff threshold.
  - If ATRL is disabled normal switching will continue and the PWM pulses will be shorter during the load release compared to when ATRL is on and either PWM pulses are supressed (LowSide FET on) or High Impedance (Hi-Z) to force current through the FET body diode.

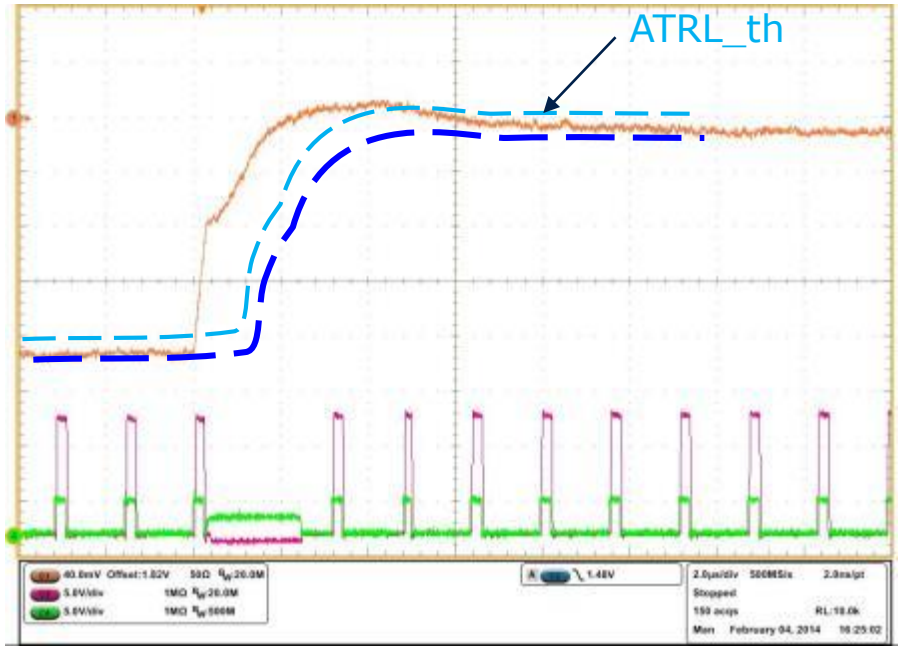
Nonlinear Control: ATRL

- When the load is released, V_{OUT} overshoots due to excess energy in the inductor being transferred to the output capacitors
- When V_{OUT} > ATRL_th, activating a PWM Hi-Z or Low Side On mode will attempt to dissipate some excess energy to reduce overshoot
  - ATRL_th is target voltage plus ATRL on threshold

w/o ATRL

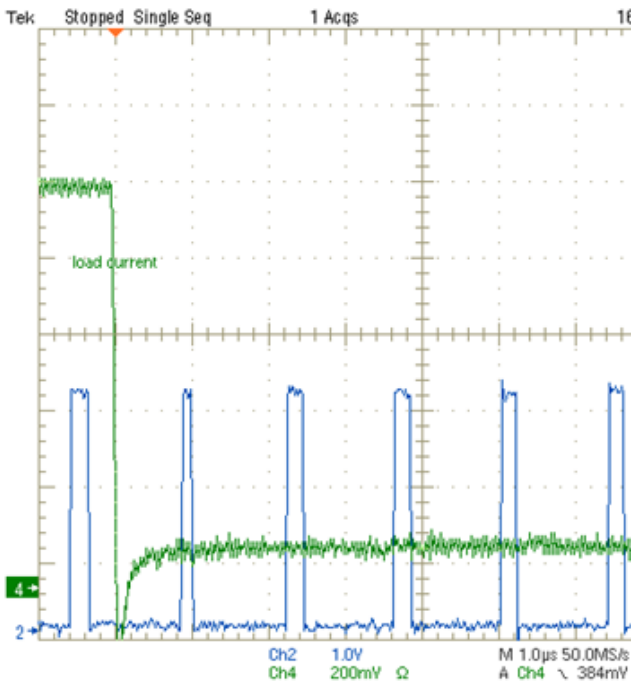


with ATRL

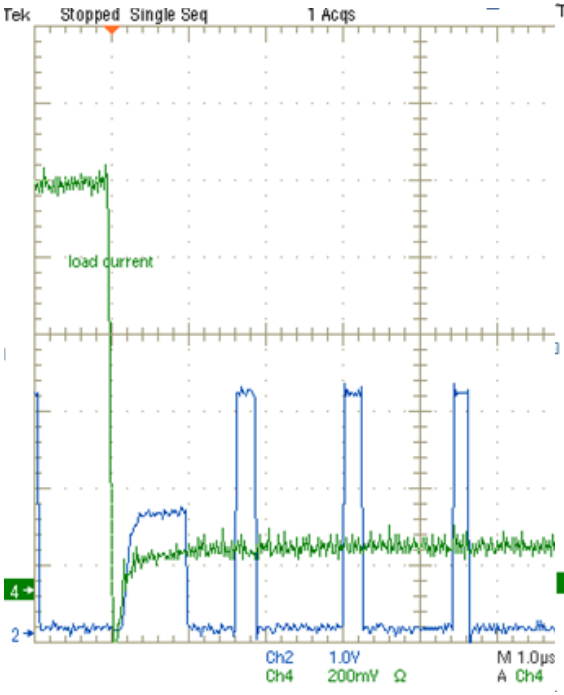


Nonlinear Control: ATRL

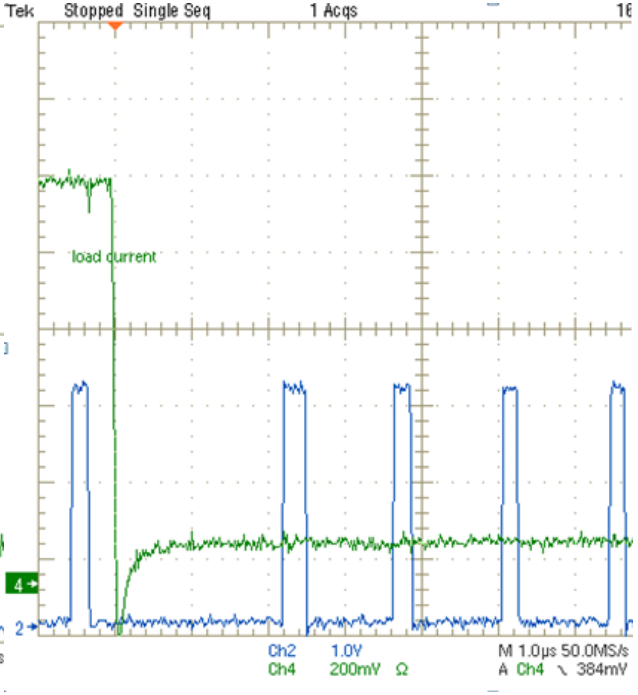
- The three settings for ARTL will treat the PWM signal differently
- Disabled



Hi-Z



Low Side on

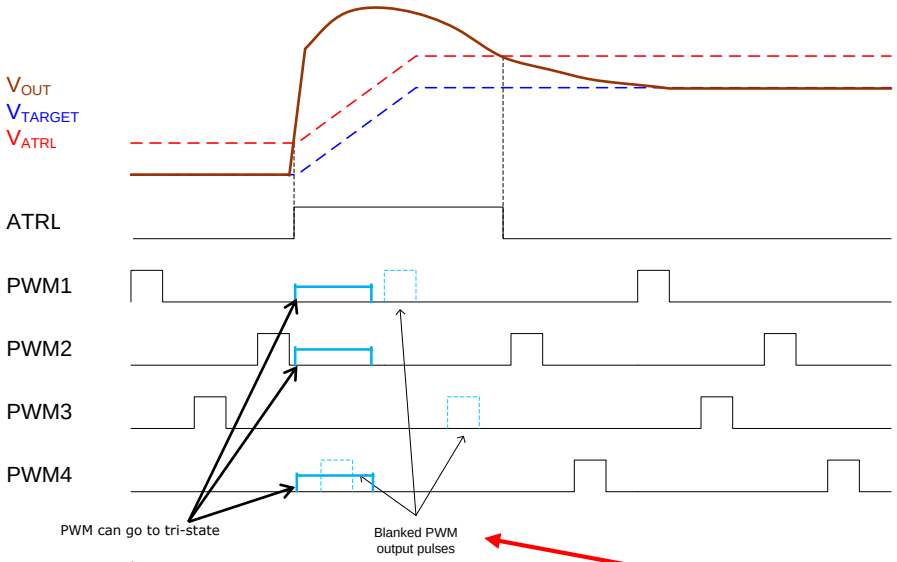


Disabled=ATRL is not active at all. PWM pulses continue

Hi-Z= Let the circulating current go through the body diode of the bottom FET

Low Side On= FET is on and let inductor current circulate through bottom FET and pulses are skipped.

Nonlinear Control: ATRL



Hi-Z

All PWM phases tri-state at the same time to all phases until Vout falls below ATRL threshold voltage

Low Side on

PWM pulses are blanked the whole time Vout is above ATRL threshold voltage

Disabled

PWM pulses are continuing during the load release.

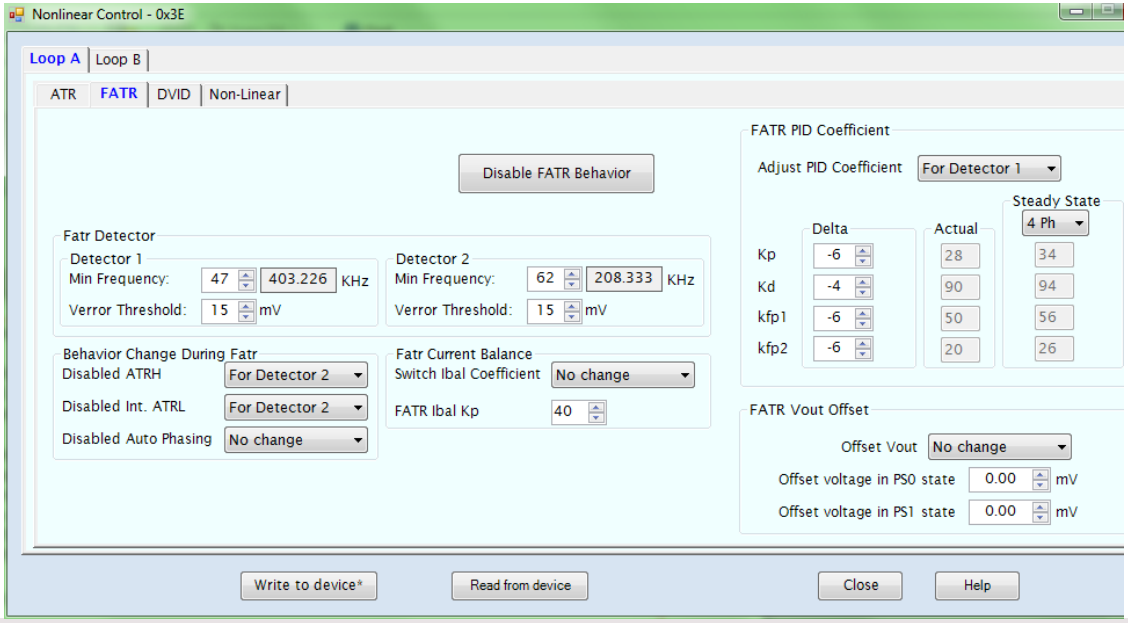
PWM pulses may be blanked for high Vout overshoot depending on how fast PID regulation reacts

Nonlinear Control: ATR Recommendations

- Only enable the ATR functions if adjusting PID alone can not meet the undershoot and overshoot requirements
  - ATR control mechanisms are driven by comparators and programmable thresholds
  - The response is non-linear and may add jitter at the output
- The thresholds should be at least 5mV (typically 10mV) wider than the measured steady state ripple voltage
- If ATR has to be enable, the PID should be made less aggressive → start by adjusting Kd and Kfp terms

Nonlinear Control...FATR

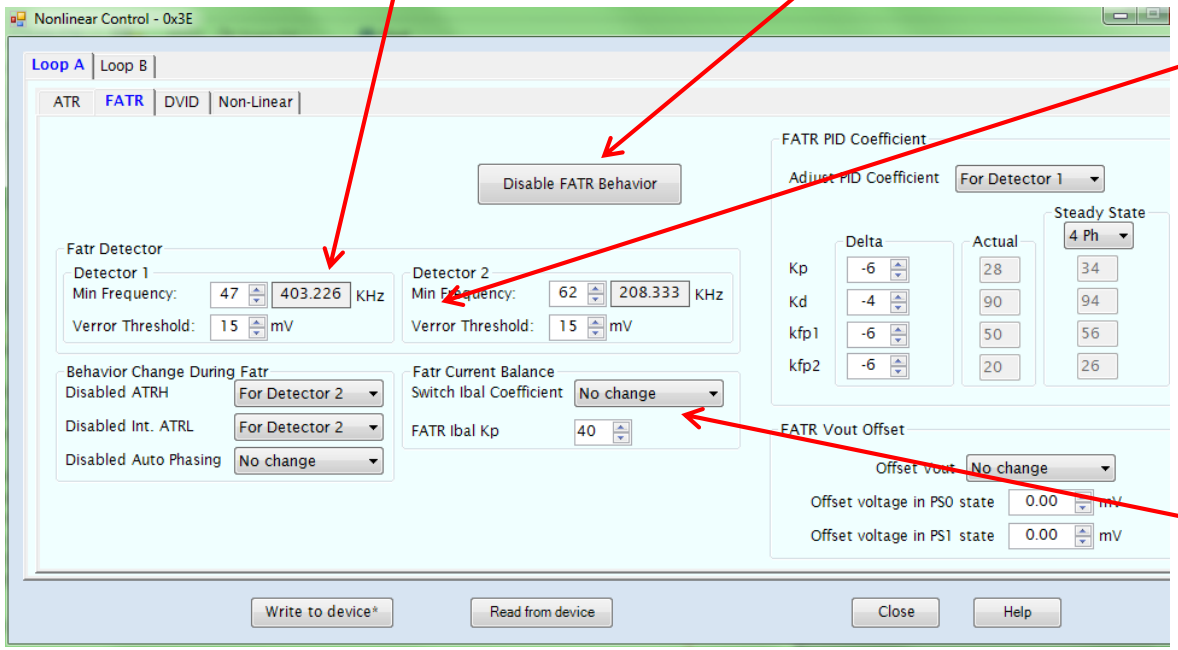
›FATR can improve transient response over output load frequency, especially for transient loads at beat frequency.
›FATR is made up of 3 independent load frequency detectors and adjustment controls that activate when the target load frequencies are detected.
›Only enable FATR if adjusting PID and ATR together still cannot meet the undershoot and overshoot requirements.
›Recommended FATR settings are the default settings when FATR is required.
›Recommended FATR settings for manual optimization of the FATR settings
–Step 1: Determine the oscillation frequency
–Step 2: Determine the cause of the oscillation
- •If it is due to ATR, disable ATR at a frequency that is slightly below the frequency determined in step 1
- •If it is due to an aggressive PID, lower the bandwidth at a frequency that is slightly below the frequency determined in step 1
- •If it is due to current balance, increase the current balance Kp coefficient at frequencies above one-fifth of the switching frequency



Nonlinear Control...FATR

Disable FATR Behavior / Restore FATR Behavior
Button will toggle the text each time it is clicked
–Selection boxes below will display "No Change" in terms of FATR behavior when disabled

Min. Freq. (Detector 1and 2)
–Minimum load transient frequency for Detector 1 and 2
–A frequency above the specified frequency and an amplitude above Verror Threshold will execute FATR settings.



Verror Threshold (Detector 1 and 2)
–Defines the window which the controller counts the number of crossings above and below the Verror threshold over time to determine the load repetition frequency
–Verror threshold should be greater than the output ripple voltage to avoid false detection.

FATR Current Balance

–The recommended setting is to adjust the current balance parameter Kp (**FATR Ibal. Kp**) to ≥40 at and above one-fifth of the switching frequency to mitigate circulating current

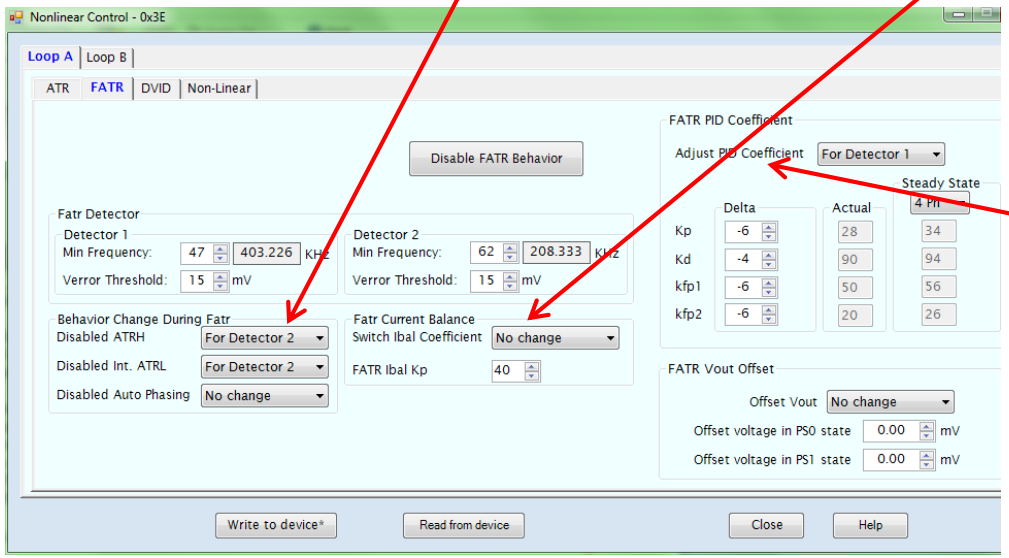
Nonlinear Control...FATR

Behavior Change During FATR: select the desired behavior for various Non-Linear features when the load frequency is above the FATR setting

–*No Change*: no behavior change
–*For Detector 1or 2*: behavior change based on the detector value selected

FATR Current Balance

–The recommended setting is to adjust the current balance parameter Kp (**FATR Ibal. Kp**) to ≥40 at and above one-fifth of the switching frequency to mitigate circulating current



FATR PID Coefficient

–Reducing the PID coefficients during load transient will help stabilize the system

–**Adjust PID Coefficient**
- adjust PID coefficient based on the detector selected

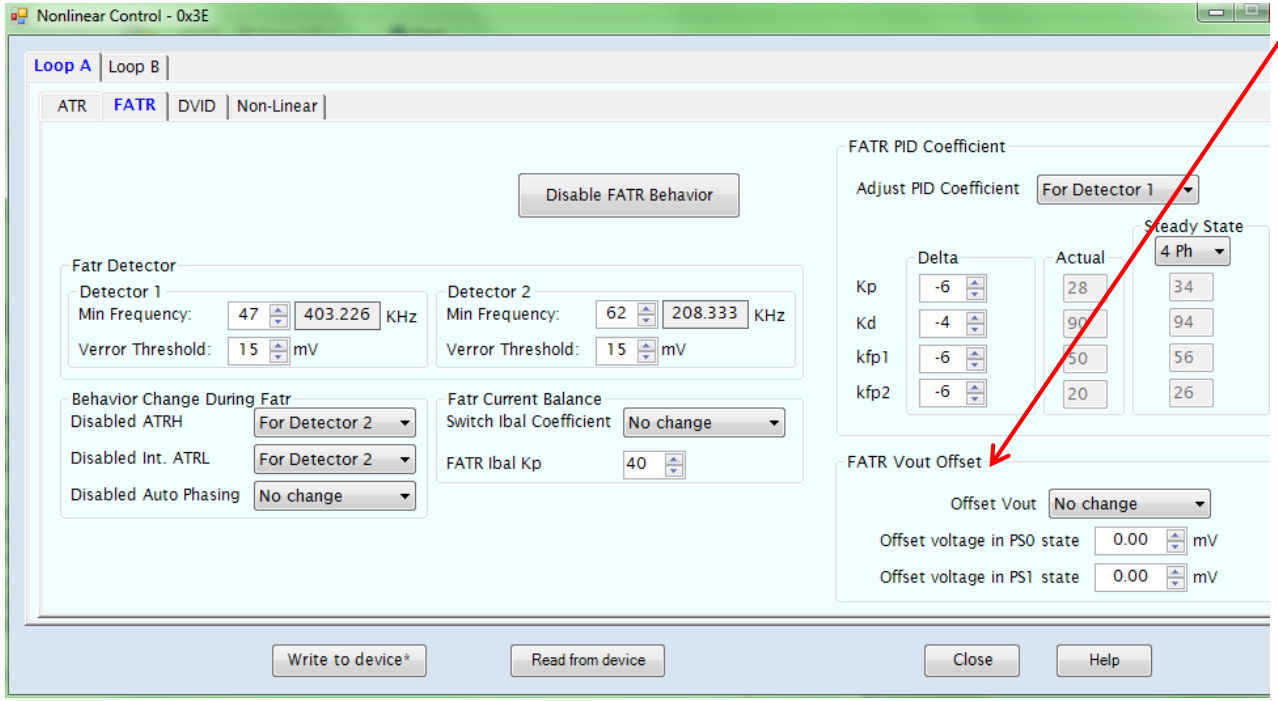
–**Kp/Kd/Kfp**

- **Delta**: allows user to set PID coefficient changes
- **Actual**: Calculated value based on the Delta and Steady State
- **Steady State**: Steady state values for the 1Ph, 2Ph, or MaxPh

Nonlinear Control...FATR

FATR Vout offset

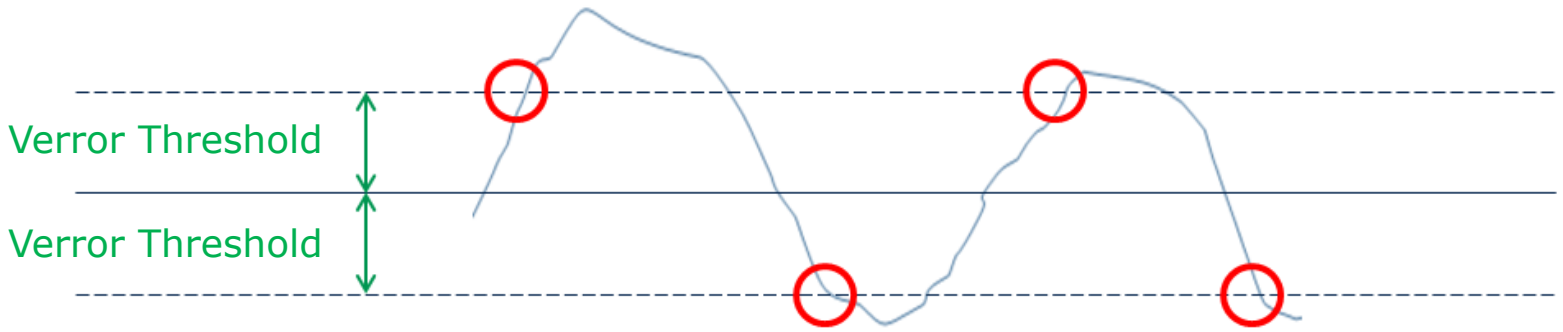
Allows offset compensation that in some conditions can occur when FATR is active



Nonlinear Control: FATR

Verror Threshold (Detector 1/2)

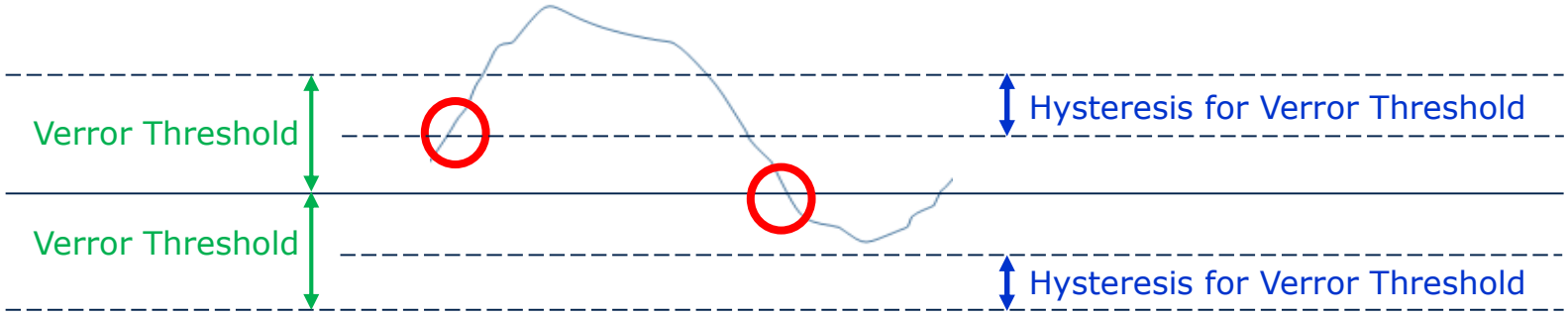
- Defines the window which the controller counts the number of crossings above and below the Verror threshold over time to determine the load repetition frequency
- Verror threshold should be greater than the output ripple voltage to avoid false detection



Nonlinear Control: FATR

Hysteresis for Verror Threshold

- Once the load repetition frequency has been detected, the hysteresis threshold reduces the threshold necessary to stay at the detected frequency



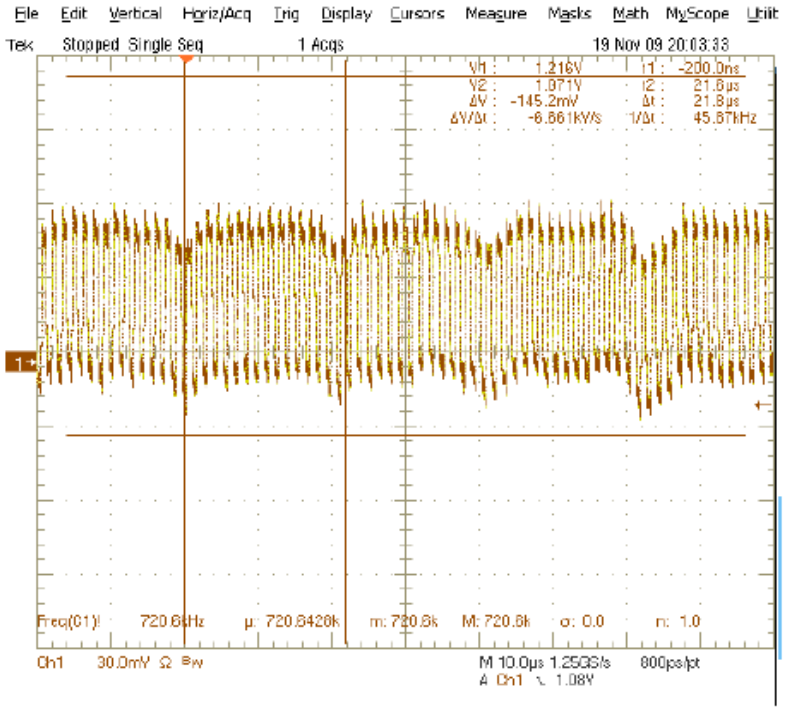
Behavior Change During FATR: select the desired behavior for various Non-Linear features when the load frequency is above the FATR setting

- *No Change*: no behavior change
- *For Detector 1/2/3*: behavior change based on the detector value selected
- ATRH Disabled Rate
  - Rate that applies to both entering and exiting the behavior
  - Recommended settings is Slew

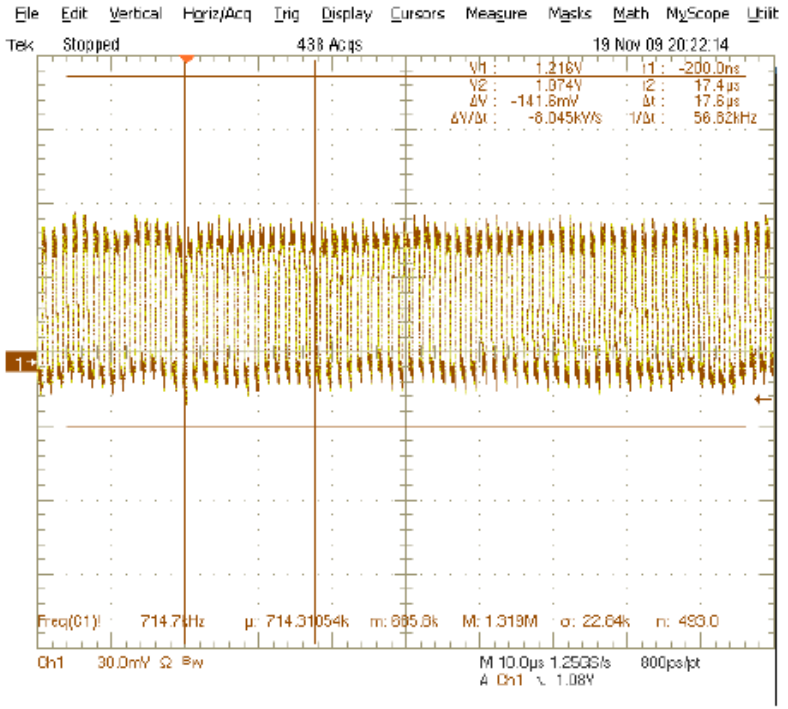
Nonlinear Control: FATR Design Example

- Observation: V_{OUT} oscillation at load frequencies above 700kHz
- Optimization: Reduce PID in FATR PID Coefficient for load frequencies > 700kHz

*FATR **dis**abled*



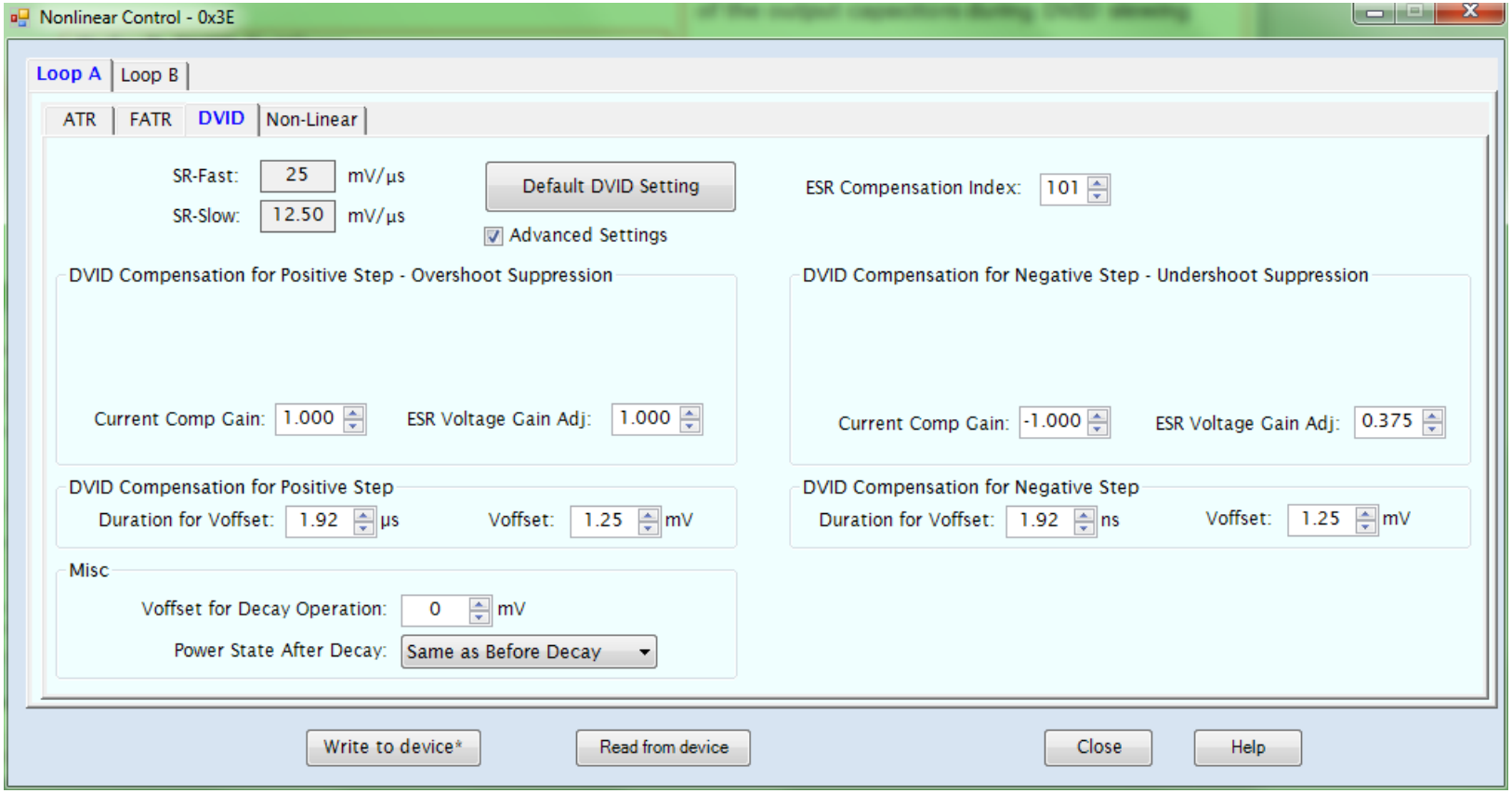
*FATR **en**abled*



VOUT Waveform Comparison

Nonlinear Control...DVID

Dynamic VID (DVID) parameters to optimize the VR's response to the SetVID_Fast/Slow/Decay commands



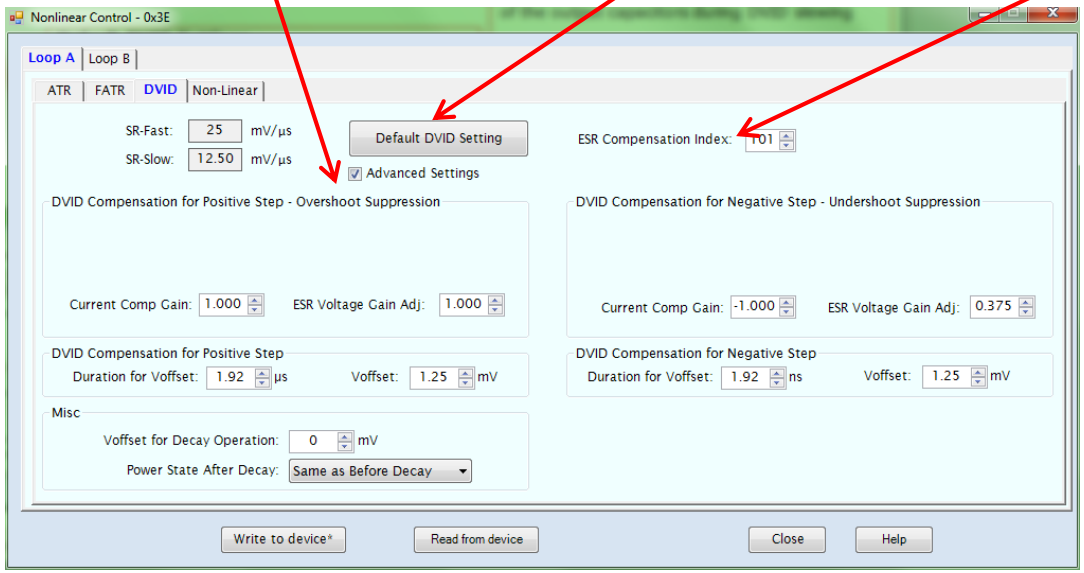
Nonlinear Control...DVID

Show Advanced Settings
–Enables DVID advance settings when selected

Default DVID Settings

–Calculates and sets the ESR Compensation Index based on the user-specified parameters in the Feedback Loop/Output Model dialog

–Sets all other parameters (including advanced setting parameters) to their default values



ESR Compensation Index

–Calculates the voltage offset caused by the ESR of the output capacitors during DVID slewing

–Is inversely proportional to the Cout *ESR time constant (***Cannot equal 0!***)

–Decrease and re-adjust the DVID Compensation slider bars (when Advance setting box is not marked)

•If fast response is needed or ring back follows the overshoot

•Lowering this value forces the target voltage to ramp up/down faster that makes the response more aggressive and bigger overshoot if the sliders stay in the same position

–Increase and re-adjust the DVID Compensation slider bars when Advance setting box is not marked

•If there is a need to weaken the compensation

Note: The normal range for **ESR Compensation Index** is ~40 to ~130. Values below 40 often result in a very aggressive response and the ones bigger than 130 end up very small improvements.

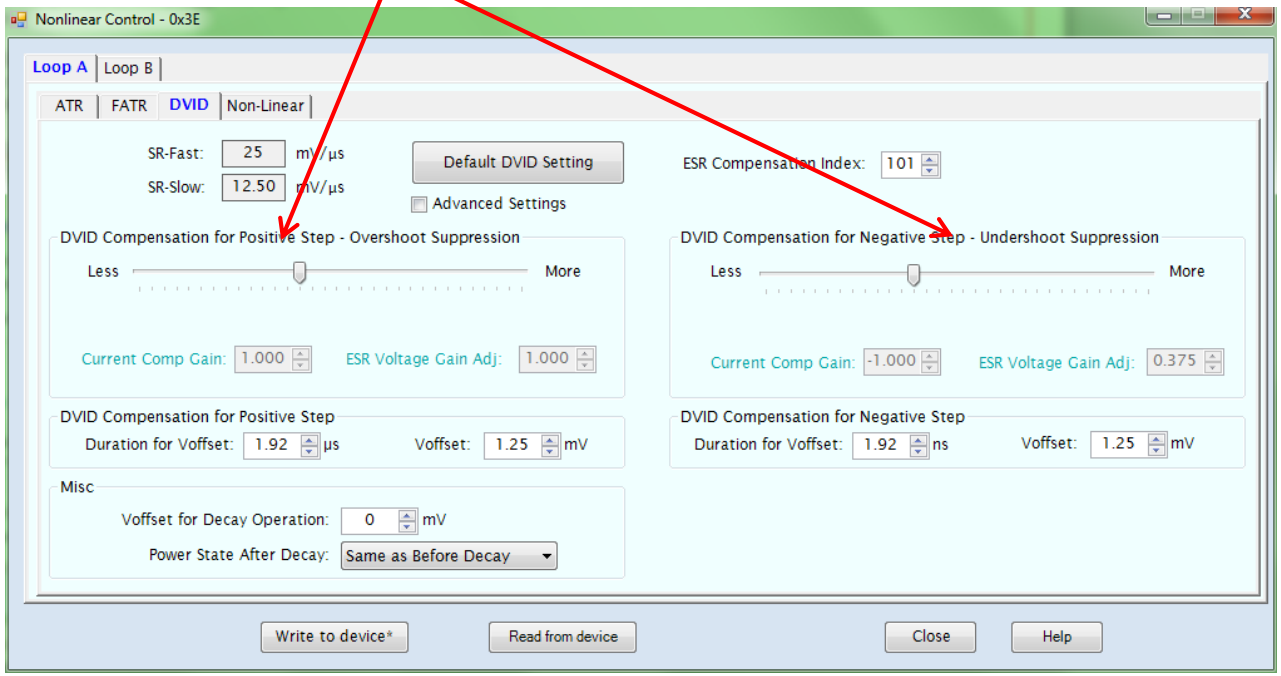
Nonlinear Control...DVID

DVID Compensation slider bars
–Use to adjust Current Comp. Gain and ESR Voltage Gain Adjust in positive or negative step

–Positive Step – Overshoot Suppression
•If the DVID response is slow, move the slider to the right to make it faster at the expense of a higher overshoot
•If the DVID response is very aggressive, move the slider to the left to make it slower and have more overshoot suppression

–Negative Step – Undershoot Suppression
•If a slower response and with less undershoot is desired, move the slider to the left (smaller index)
•Move the slider to the right or left to obtain the desired response

–Slider bars are disabled and not visible when Advance Settings box is marked



Nonlinear Control...DVID

Current Comp. Gain
–Use to compensate the voltage offset caused by the load-line effect on the output capacitor charging or discharging current during DVID slewing
–Directly proportional to load-line and inversely proportional to ESR

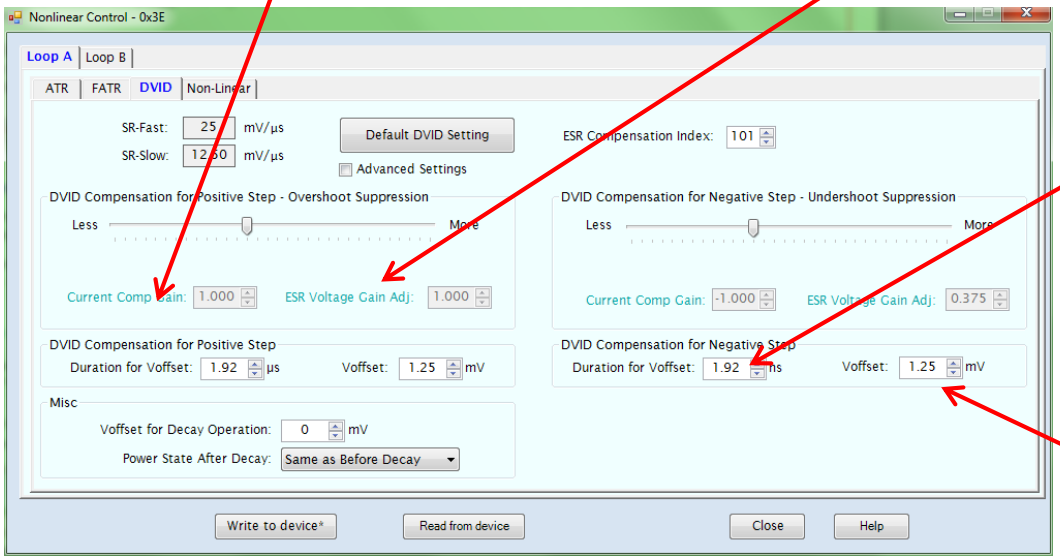
–Positive Step – Overshoot Suppression
•Usually ≥ 1 because faster response is desired

– Negative Step – Overshoot Suppression
•Usually ≤ 0 because response should be slowed down to prevent any undershoot, therefore it is suggested to be not fully compensated

ESR Voltage Gain Adj
–Used to compensate voltage offset caused by the output capacitors' ESR during DVID slewing

–Positive Step – Overshoot Suppression
•Usually set to 1

–Negative Step – Undershoot Suppression
•Usually set less than Positive Step – Overshoot Suppression value

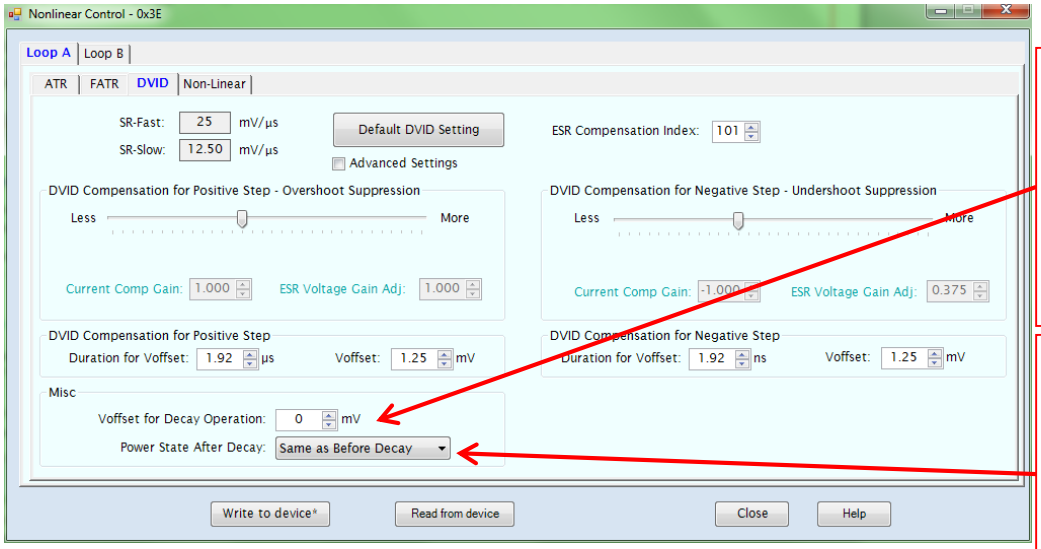


Duration for Voffset

–Time where the Voffset will be applied after the ramp completion
–Independent settings for Positive and Negative Step

Voffset
–Offset amplitude added after the ramp completion
–Independent settings for Positive and Negative Step

Nonlinear Control...DVID



Voffset for Decay Operation

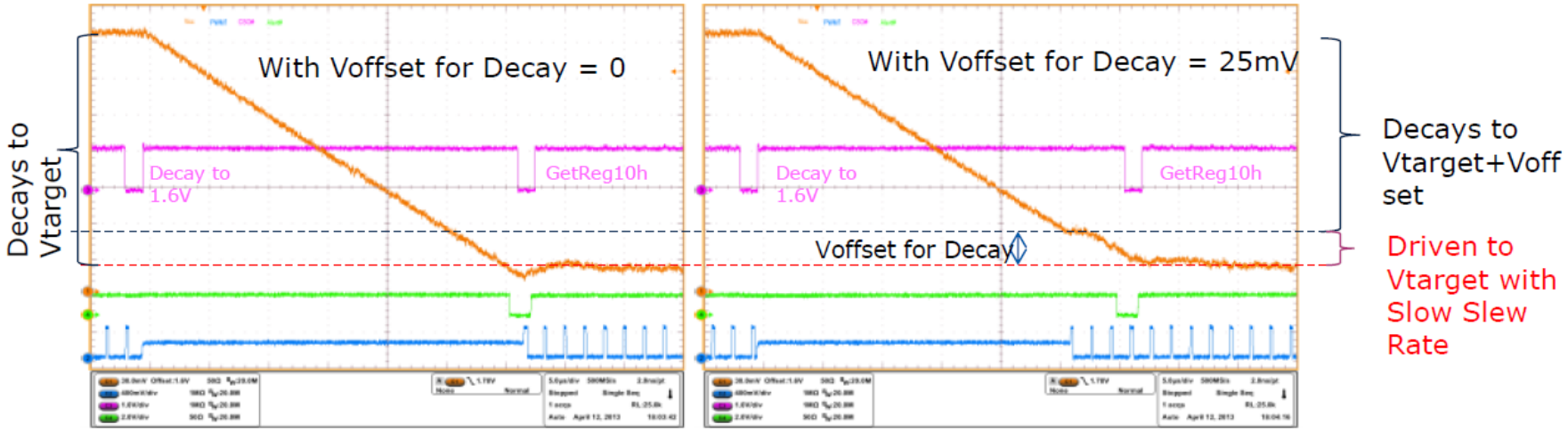
–After the VR reaches the Vtarget + Voffset through decay, the VR will actively drive Vout and continue to ramp to the Vtarget with the specified number of phases for PS2, at slow slew rate

–Recommended value is 25mV

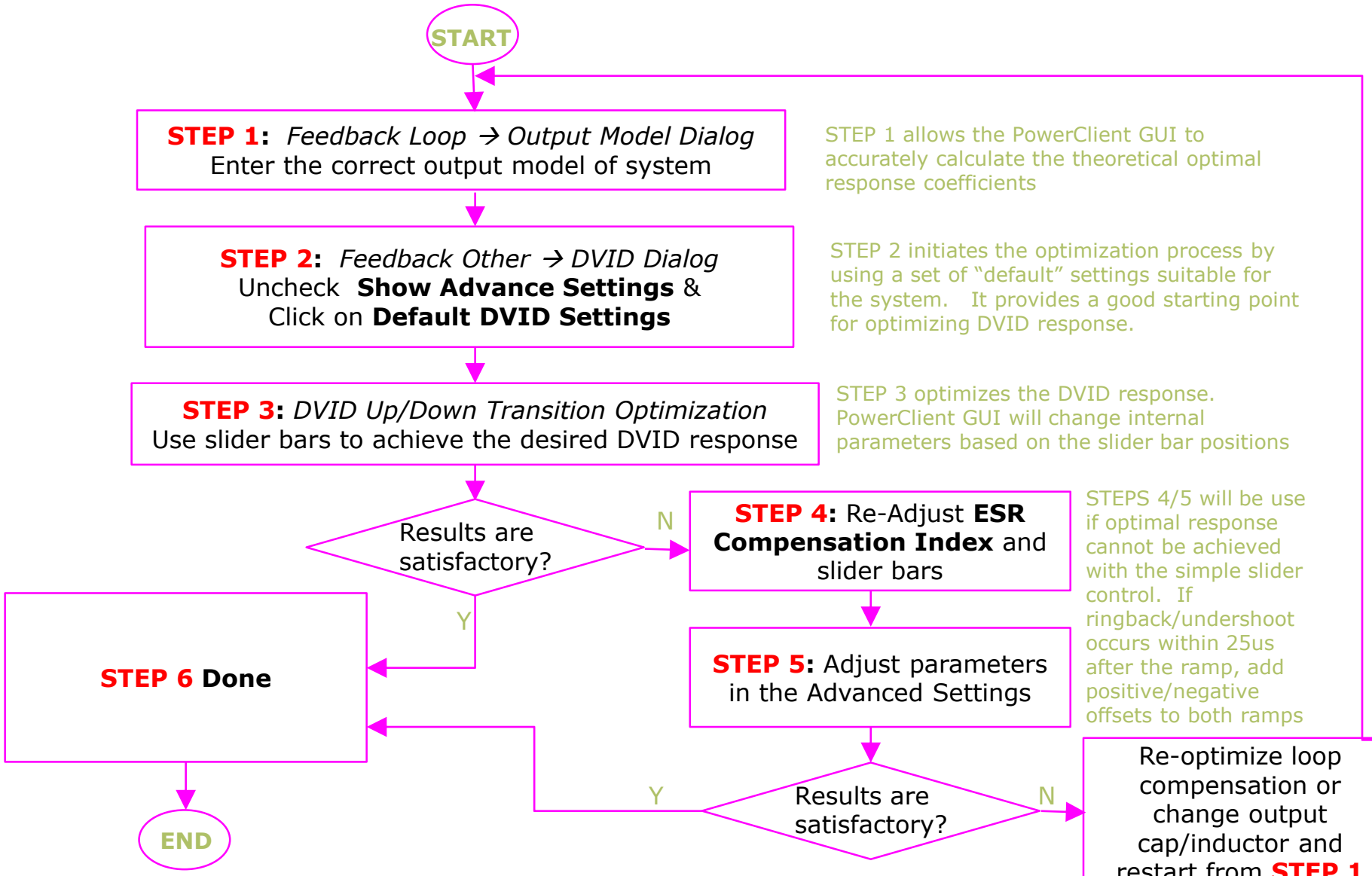
PowerState After Decay

–Same as Before Decay – VR will keep the same PowerState after the decay as it had before decay. Normally for VR13 applications.

–PS2 – VR enters PS2 state after decay. Normally for IMVP8 applications.



Nonlinear Control...
DVID Optimization Procedure

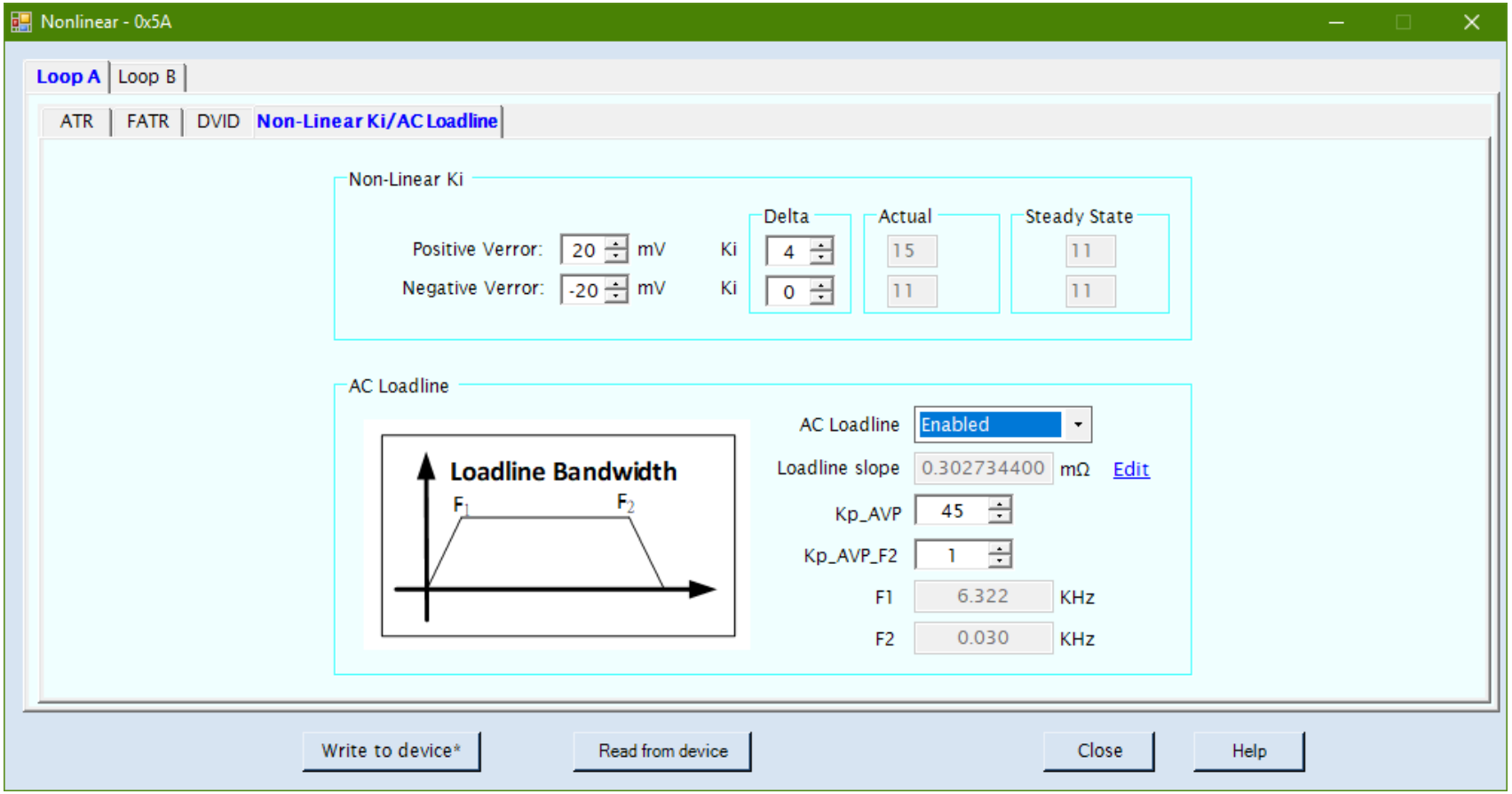


Nonlinear Control...
DVID Optimization Procedure

- If desired response cannot be achieved in **Step 5**
- –Re-adjust PID coefficients in the Feedback Loop/Compensation tab dialog. The current response is not well optimized.
- •An unstable system will cause undesired rings or oscillations
- •A very slow system cannot meet DVID timing requirements
- –Reduce output inductance or capacitance: Current introduced by very large output capacitance (C*dv/dt) is very difficult to compensate for.
- •Extra current (energy stored in L) during a DVID up event will transfer to the output cap resulting in overshoot waveform
- •Large overshoot will accumulate more error in the PID which the loop has to remove, resulting in slight undershoot

Nonlinear Control... Non-linear

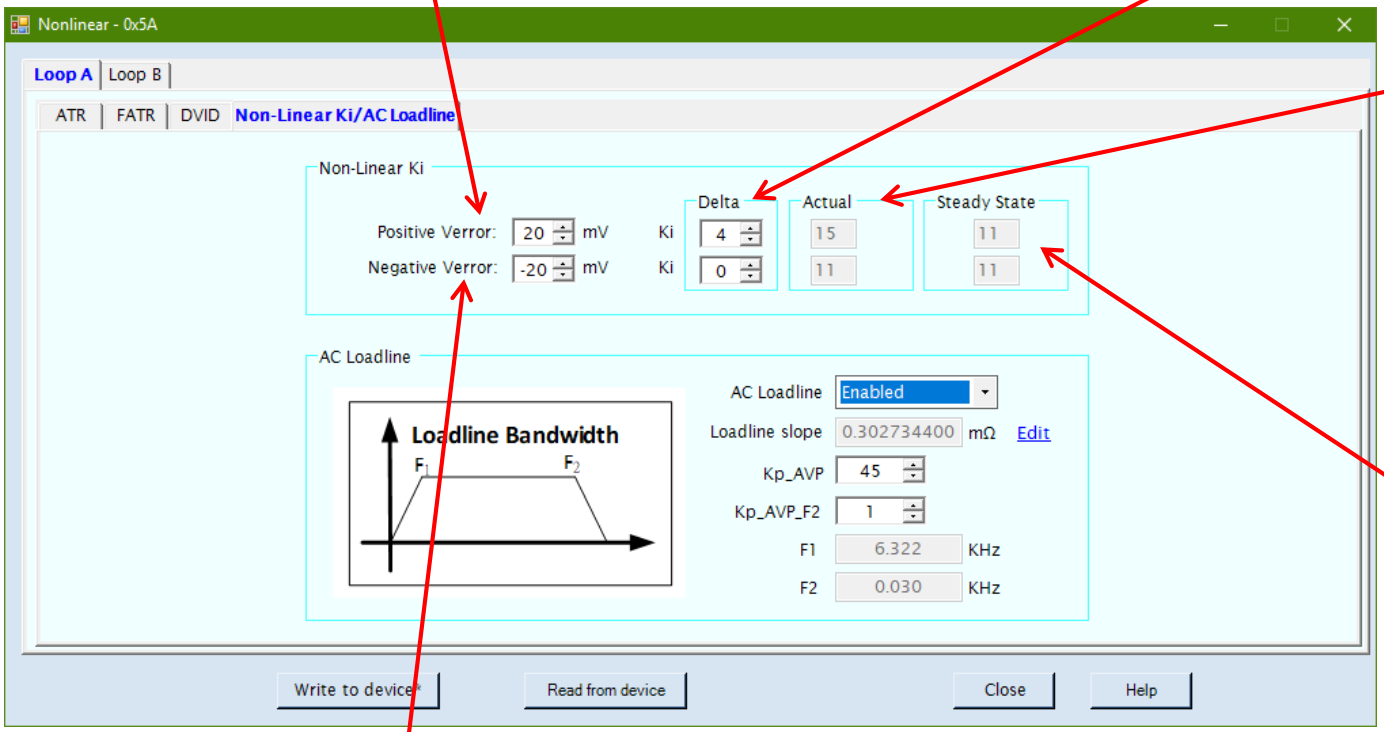
Non-Linear parameters to gain more undershoot or overshoot margin at high load repetition frequency. More explanation on next pages.



Nonlinear Control... Non-linear

Positive Verror:
–Verror threshold to activate Ki change specified in Delta Ki

Delta Ki :
–Ki change applied to the original Ki when Positive or Negative Verror is met



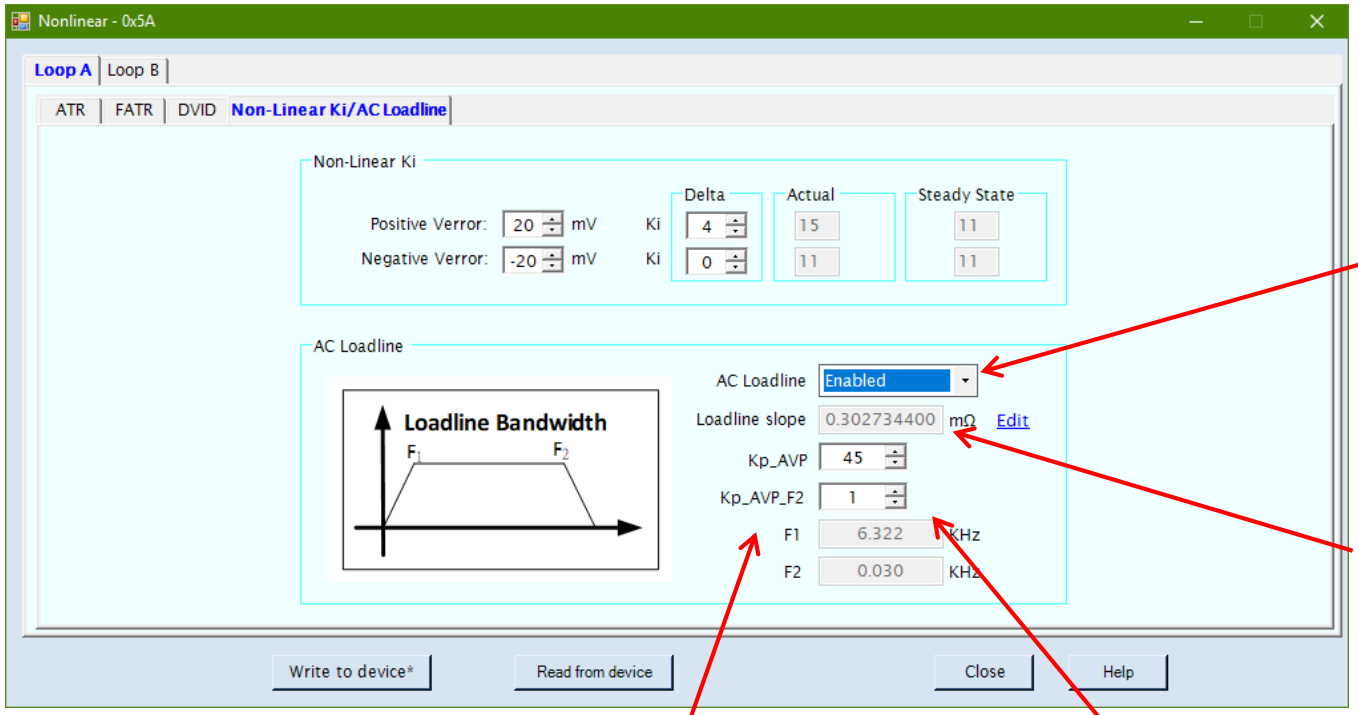
Actual:
–Calculates and displays the actual Ki when the changes in **Delta** are applied

Steady State:
–Displays the original steady state Ki

Negative Verror:
–Verror threshold to activate Ki change specified in Delta Ki

Note: Verror threshold should be larger than output ripple amplitude to avoid false trigger

Nonlinear Control... AC loadline



AC loadline:
Enable or Disable the AC loadline function.
AC loadline add a slope to a loadline between 2 frequencies. While still having the regular performance at steady load for applications that normally do not use loadline.
AC loadline may improve higher frequency load transients to have less over/undershoot.

Loadline slope:
Slope of the AC loadline between selected frequencies.
Notice that when AC loadline is enabled there is no loadline at lower frequencies.

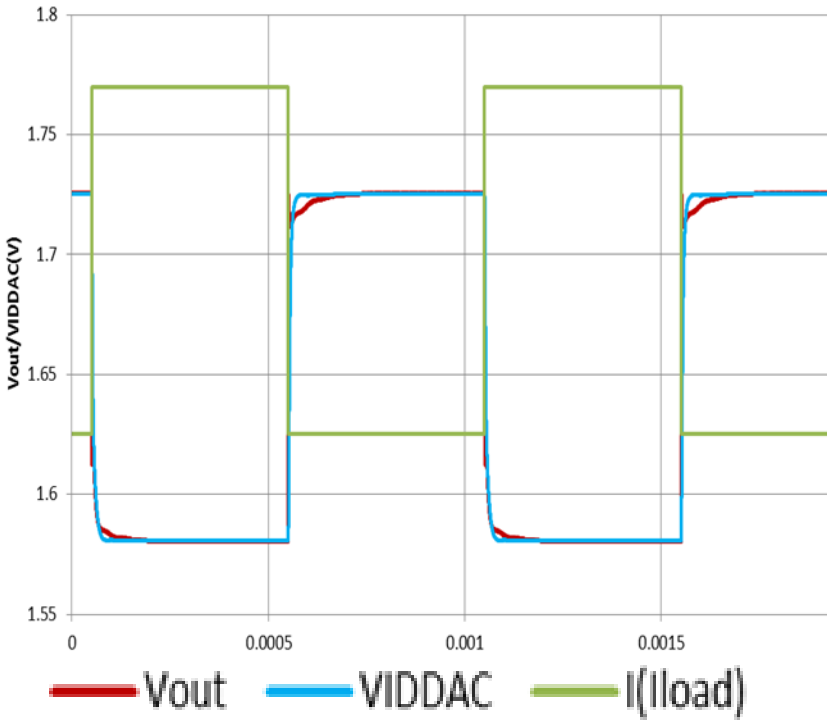
Kp_AVP:
Propotional gain factor at upper frequency of the range where AC loadline works. See calculated frequency F1

Kp_AVP_F2:
Propotional gain factor at lower frequency of the range where AC loadline works. See calculated frequency F2

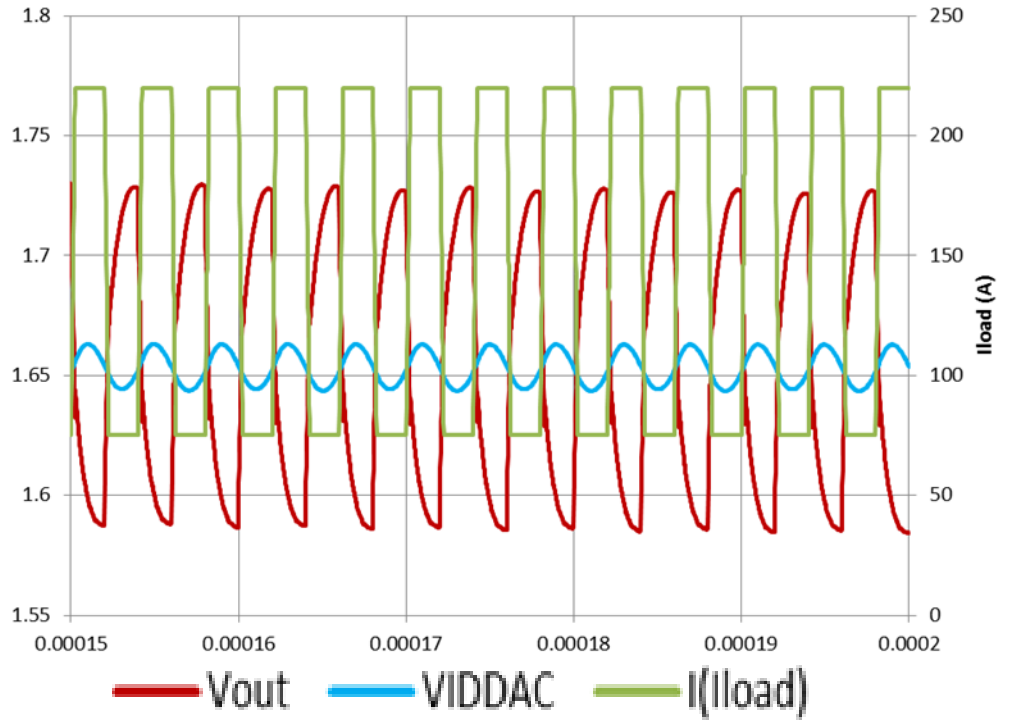
Nonlinear Control:
Non-Linear Background

› At high load repetition frequency, VOUT cannot settle within one load cycle

1kHz Load Transient
(VOUT is settled)



250kHz Load Transient
(VOUT is not settled)

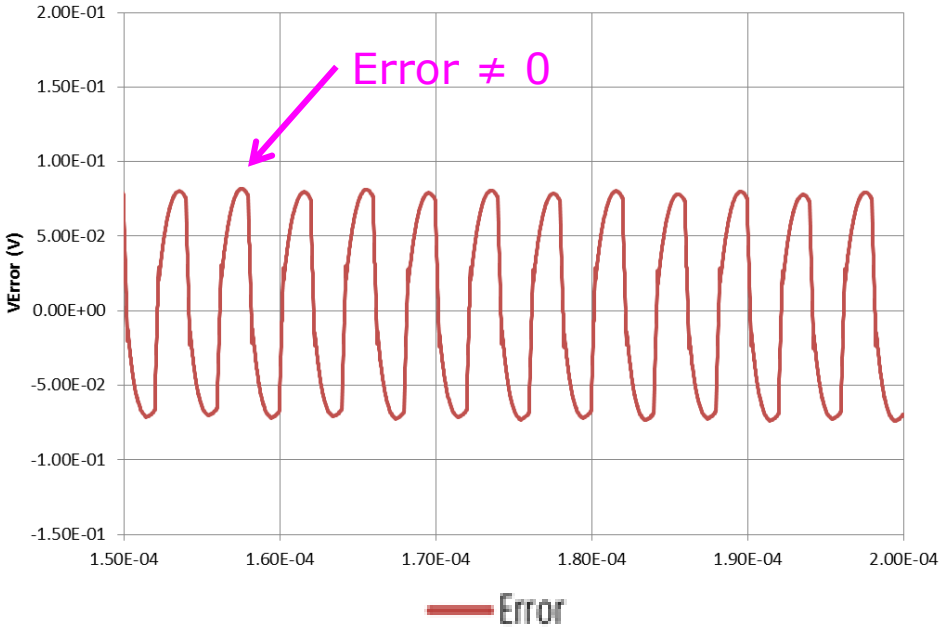


Nonlinear Control: Non-Linear Background

› For high frequency transient response the error can not be reduced to 0 before next cycle of transient load occurs

VError at 1kHz Load Transient

VError at 250kHz Load Transient

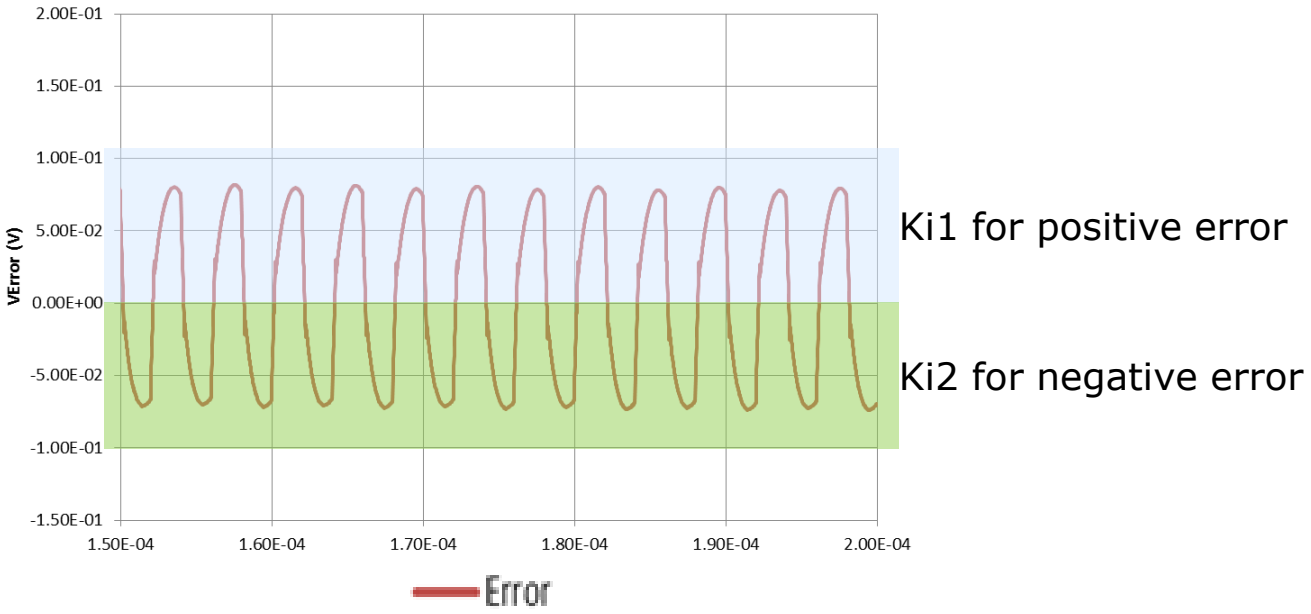


Nonlinear Control:
Non-Linear Background

- Compensator I term is proportional to the integrated error

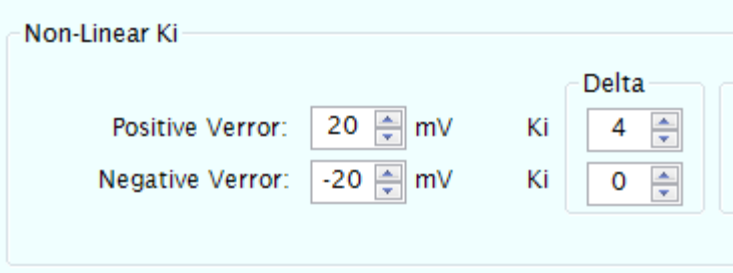
$$I\ term = Ki * \int Error\ dt$$

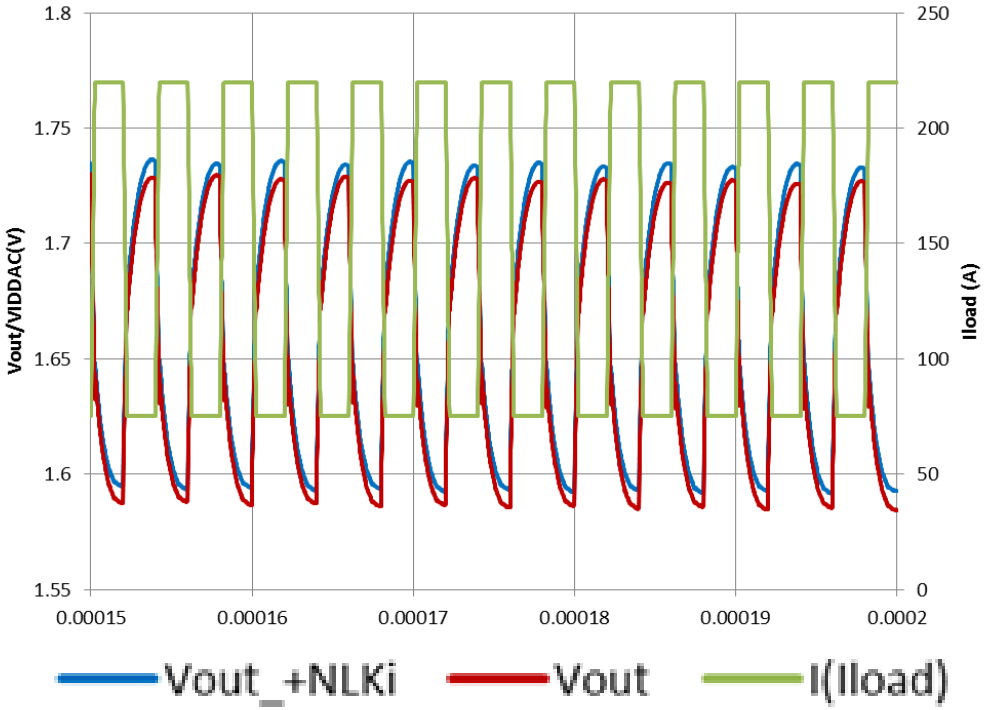
- Ki for positive and negative Verror can be specified separately to influence the I term:
  - If Ki1 > Ki(original) AND Ki2 ≤ Ki(original), VOUT will be shifted up
  - If Ki1 ≤ Ki(original) AND Ki2 > Ki(original), VOUT will be shifted down



Nonlinear Control: Non-Linear example

› If more undershoot margin is needed, we can specify a positive Ki to shift VOUT up





Agenda

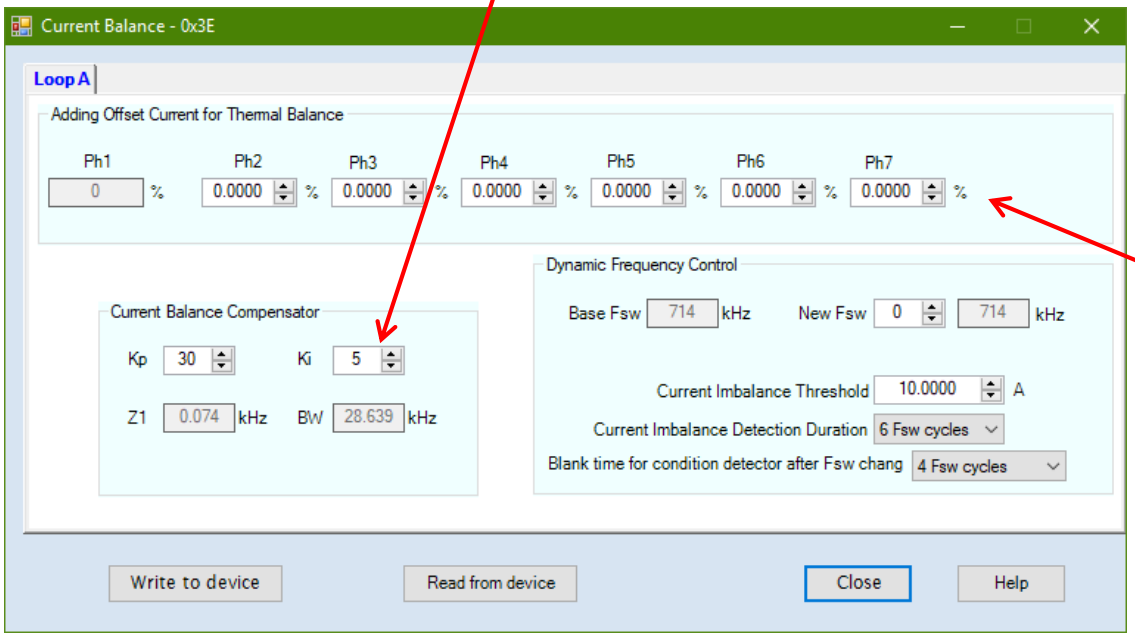
Current balance...

Kp - Current Balance Compensator
Used to tune current balance loop compensator
Ki - Current Balance Compensator
Used to tune current balance loop compensator
Z1 - Current Balance Compensator
Displays the zero location of current balance compensator
BW - Current Balance Compensator
Displays the bandwidth of current balance compensator

How to tune and how to disable

When tuning make sure the Bandwidth BW is less than the BW for Vout loop. Typical 1/3 of the voltage loop.
Typical start values are Kp=30 Ki=5

To turn off current balancing set Kp=0 and Ki=0

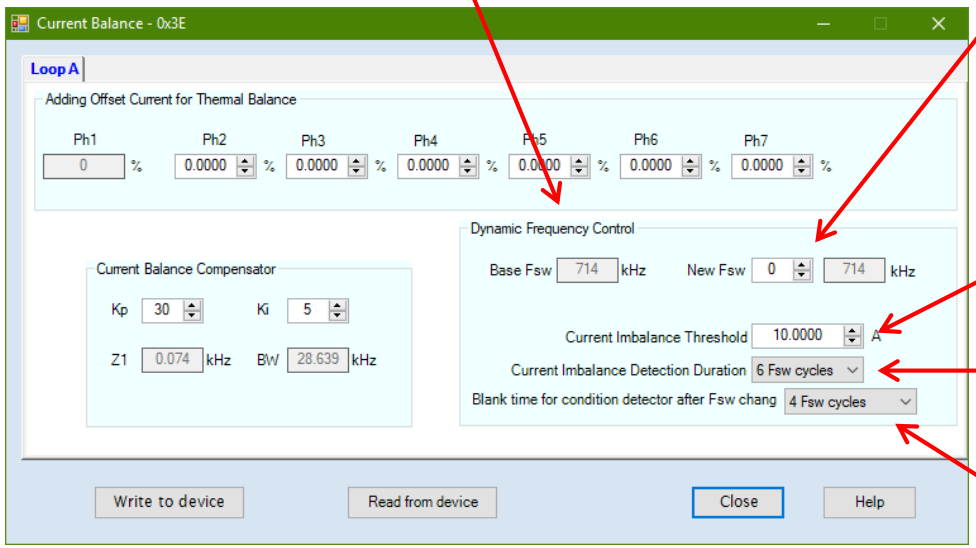


Thermal Balance

Relative to phase1 an offset for current can be added for each phase.
This allow for thermal balancing i.e. Some phases have better airflow and can be allowed to take a higher current

Current balance...

Dynamic Frequency Control
When current imbalance or ATRH exceeds thresholds it is typically when load frequency is close to switching frequency.
It can benefit ripple voltage and/or current balance to then change the switching frequency to another frequency



New Fsw
Set the frequency to shift to when current imbalance or ATRH indicate possible conditions where a shift of frequency is beneficial. Typical 2 or 3 steps from Base Fsw.
No shift occurs when set to 0

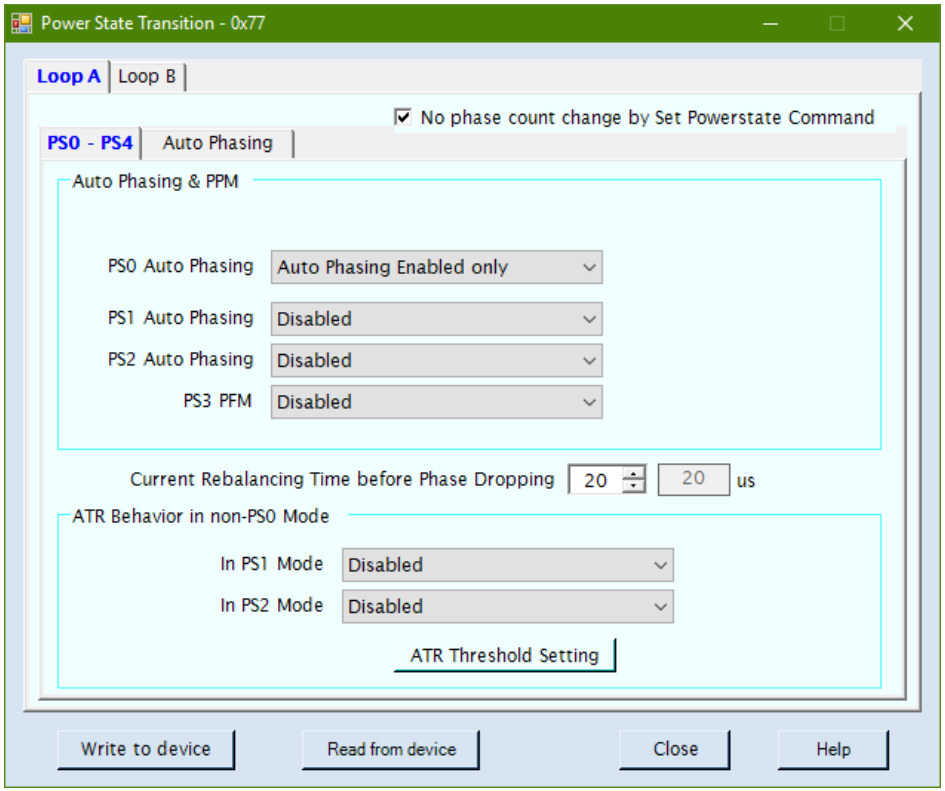
Current imbalance threshold
At which current balance difference to trigger shift of frequency.

Current imbalance duration
How long time for imbalance detected until trigger shift of frequency

Blank time
How long time to wait after a change of frequency until detector can activate a new change in frequency.

Agenda

Power State Transitions...



Auto Power State Definitions

PS0→ more than 1 phase operation
- ○IOUT is greater than the 'phase add' current threshold

PS1→ 1 phase (or 2 phase) operation
- ○IOUT is less than 'phase add' current threshold
- ○IOUT is greater than PS2 threshold

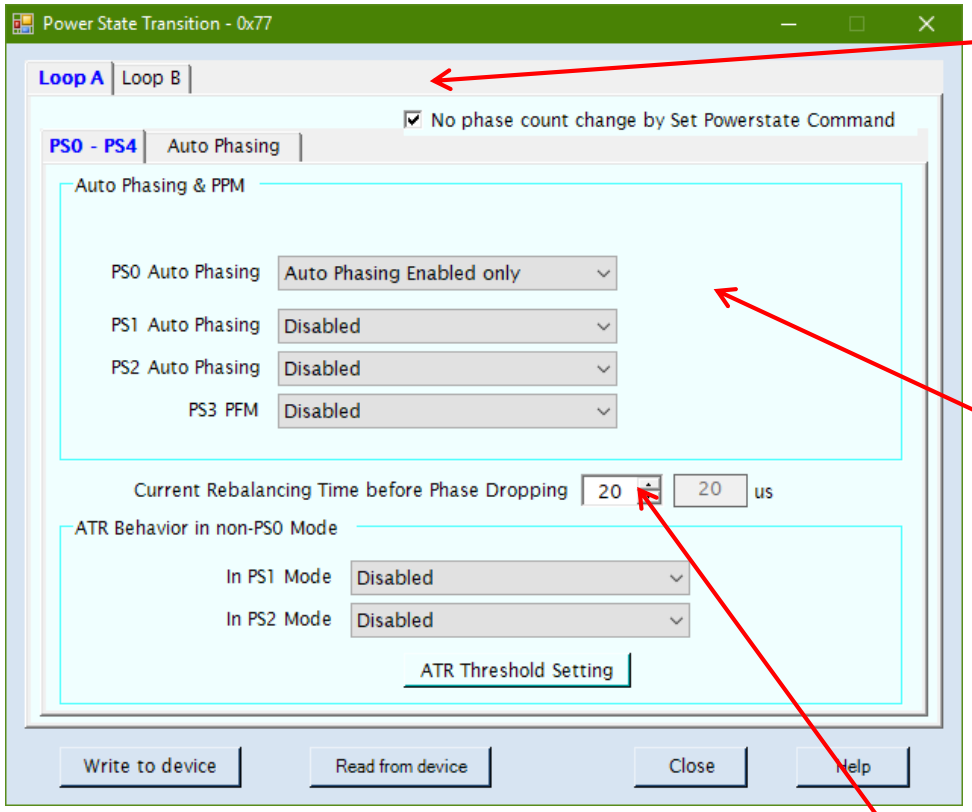
PS2→ Diode Emulation, Constant on-time, variable frequency
- ○IOUT is less than PS2 threshold (typically set between 5A and ½ inductor ripple current)

PS3
- ○Same as PS2

For AMD
PS0=normal operation
PS1=PSI0_L
PS2=PSI1_L

Power State PS0
Is automatically selected when in Overclocking mode or manual selected Vout.

Power State Transitions...



No phase count change by set PowerState Command
When checked, the controller will always operate at PS0 mode. PS commands on the SVID bus are ack'd but will not be reacted to.

PS0/1/2 Auto Phasing
- Specifies the auto phasing function for PS0, PS1, or PS2
  - Disabled: Auto phasing and PFM are disabled
  - Auto phasing is enabled only
  - Auto phasing and PFM enabled

PS3 PFM
- Specifies if PFM is enabled for PS3 operation for extra power savings
  - Disabled –PFM is disabled

◆ When disabling/enabling auto phasing function, PID will get change. This is due to PID scaling function is enabled when auto phasing is enabled.
If PID for Max phase operation is changed, just change back to original value before again selecting auto phasing disabled.

Window look slightly different if controller is in VR14 mode.
Autophasing same for all PS

Current Rebalancing Time before Phase Dropping
–This is used to set the delay before phase dropping (includes by PS command and auto phasing). During this period, the controller is trying to unload the current from the phase to be dropped

Power State Transitions... Auto Phasing

Thresholds for Dropping Phases:
–At which output current should a shift to less number of phases occur.
Example: As Iout current drop below 60A there will be a change from 4 phases to 3 phases.

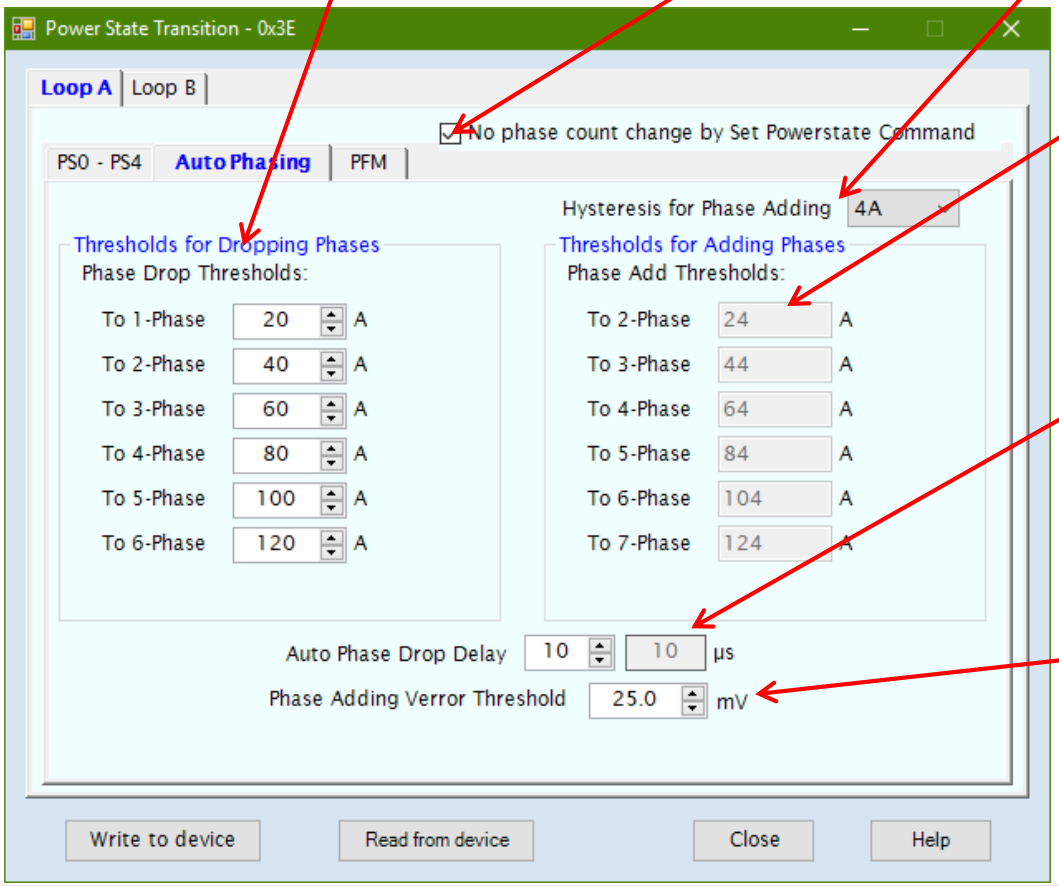
No phase count change by Set Powerstate Command:
–Do not change number of phases even if Powerstate is changed when box ticked

Hysteresis for Phase Adding:
–To avoid too many add/drop of phases a hysteresis can be set. This avoid a continuous change of number of phases if current is just at the set threshold

Thresholds for Adding Phases:
– Calculated from the Hysteresis and the set value for dropping phases. When Iout is higher than the shown current one phase is added

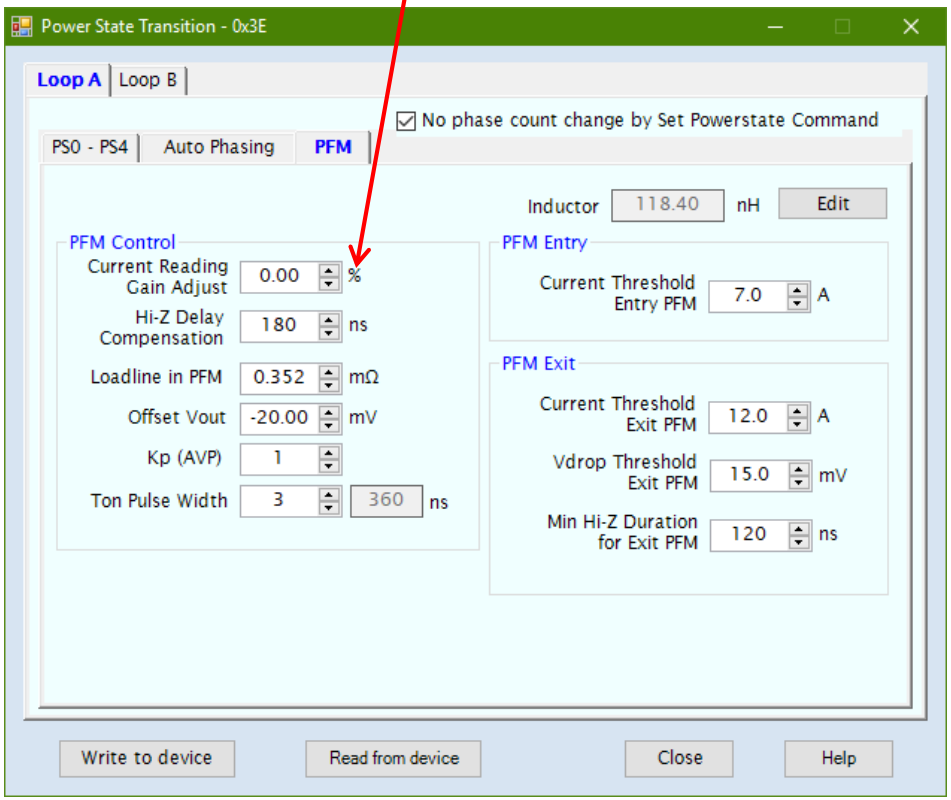
Auto Phase Drop Delay
–For autonomous phase dropping to occur, the output current needs to remain lower than the drop threshold for the entire period of time specified by the Auto Phase Drop Delay parameter.

Phase Adding Verror threshold
–When the error voltage is larger than the specified value, the controller will proceed to add all phases immediately.
i.e. during a large loadstep and Vout drops fast. Then this detection activate all phases for best recovery.



Power State Transitions... PFM

If any of the selections for Autophasing select PFM function then a PFM tab is added in the window. In other cases this tab is not visible.



Current Reading Gain Adjust
Adjustment to the current reading accuracy in PFM mode

Hi-Z Delay Compensate
Reduces the actual off-time of the PWM signal in order to compensate the power stage delay in transitioning from off to Hi-Z

Loadline in PFM
Define how much Vout is adjusted by load current in PFM from 12.5% to 100% of the load-line setting

Offset Vout
Adjust the threshold voltage for the PFM comparator to initiate a new PFM cycle (on/off pulse) when the Vout reaches or drops below this threshold. The threshold should be raised or lowered so that the PFM ripple stays well within the regulation window allowed under PFM.

Kp (AVP)
A delta-term to reduce the bandwidth of the AVP loop during PFM mode

Current Threshold Entry PFM
In 1-Phase PWM mode, the output current must reach this threshold in order to enter PFM mode

Current Threshold Exit in PFM
Exit from PFM under conditions of overcurrent (i.e. 2-3A above the PFM/PWM efficiency cross-over load)

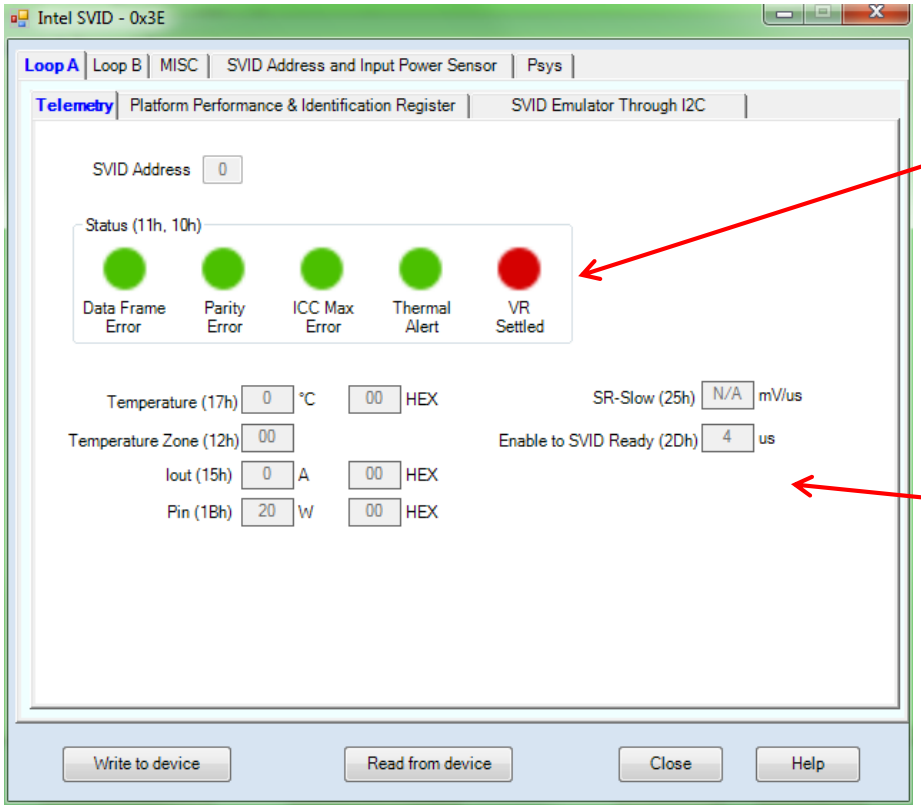
Vdrop Threshold Exit PFM
The threshold at which a transient would trigger an exit from PFM to PWM operation
ATRH1 must be enabled for this function

Min. Hi-Z Duration for Exit PFM
Exit PFM if the Hi-Z time of 6 consecutive PFM cycles is less than this threshold
Configure this threshold such that an exit condition occurs at the PFM/PWM crossover efficiency load-level

Agenda

SVID... Telemetry XDPE122xx family

The Intel SVID window is only available for devices that support SVID



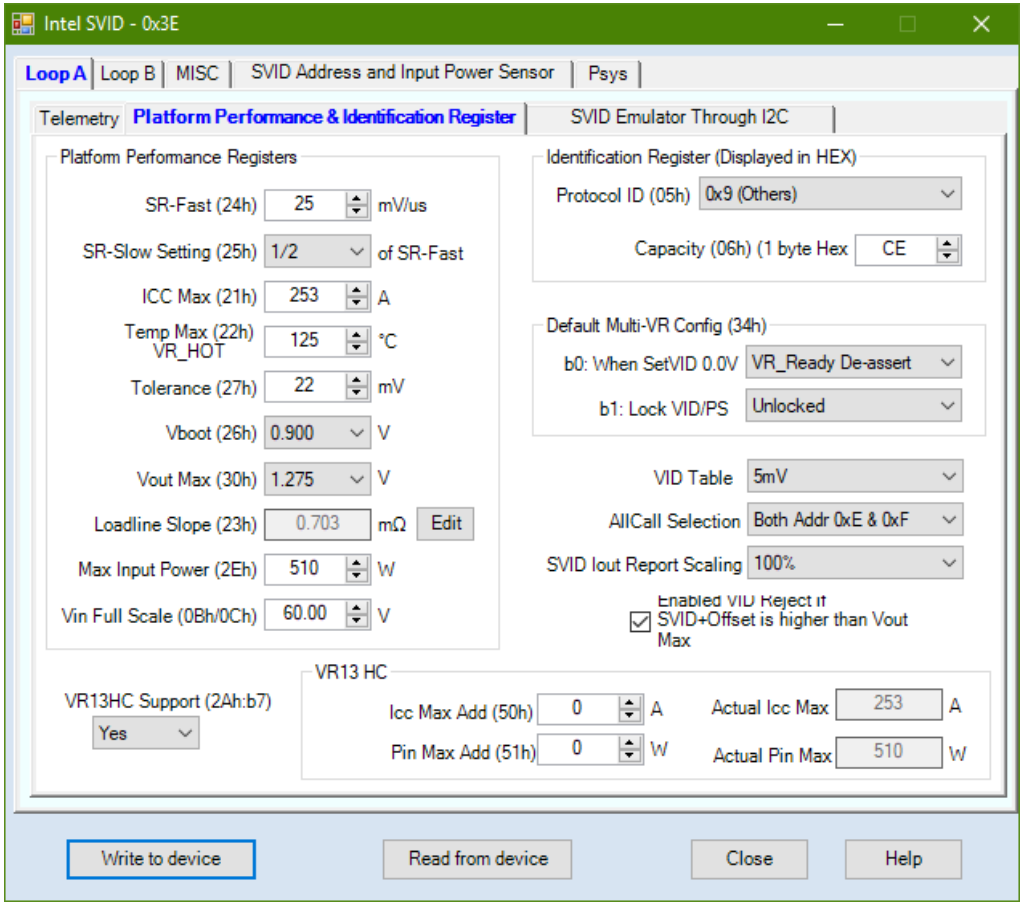
Readout of the status bits in SVID registers.

Readout of parameters in SVID registers.

SVID... Platform Performance XDPE122xx family

Allow settings of all the registers that SVID use.

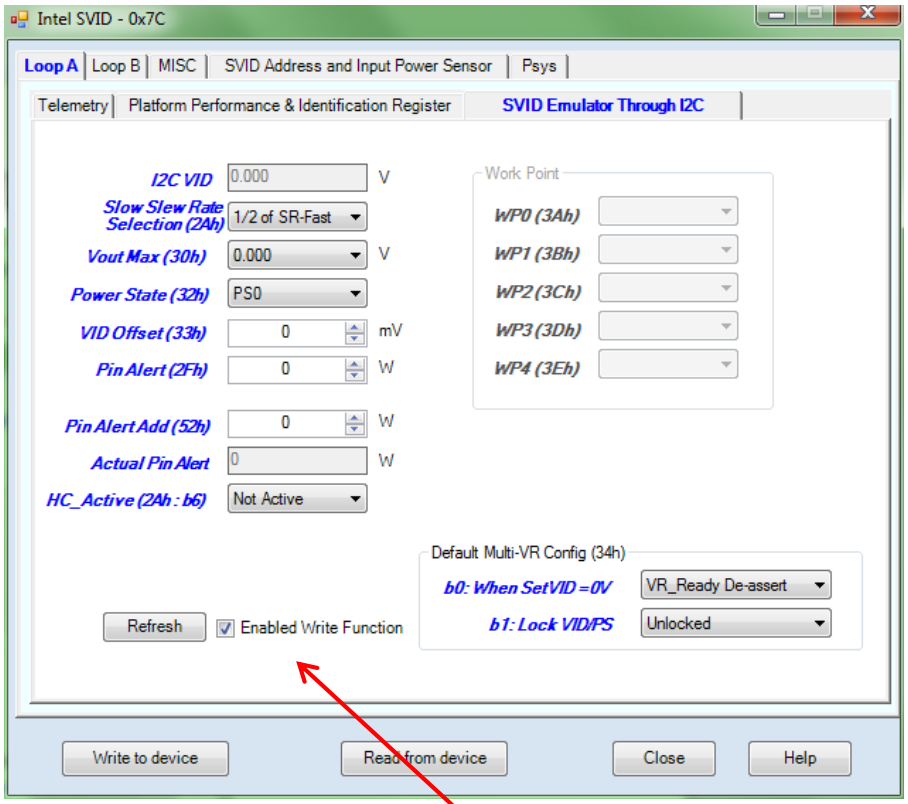
Depending on settings some parameters may not be visible if not used i.e. VR13HC settings only visible when VR13HC is activated.



SVID... Emulator through I2C XDPE122xx family

Allow a number of SVID settings to be emulated and sent via I2C to voltage regulator.

Loop B have less number of settings as it is already set in loop A

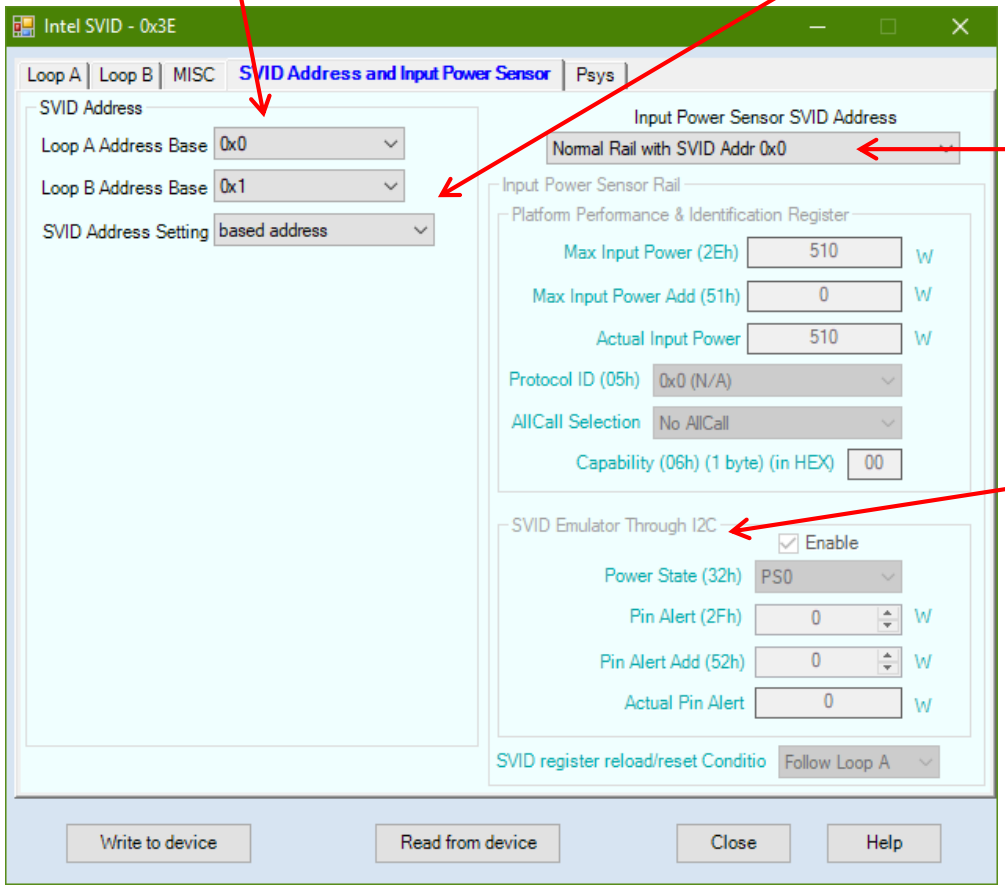


Mark the box to enable this I2C SVID emulator function

SVID... Address and Input Power Sensor XDPE122xx family

Selection of SVID address

SVID address can also be selected using external resistors. Table shows the different combinations of resistor and address



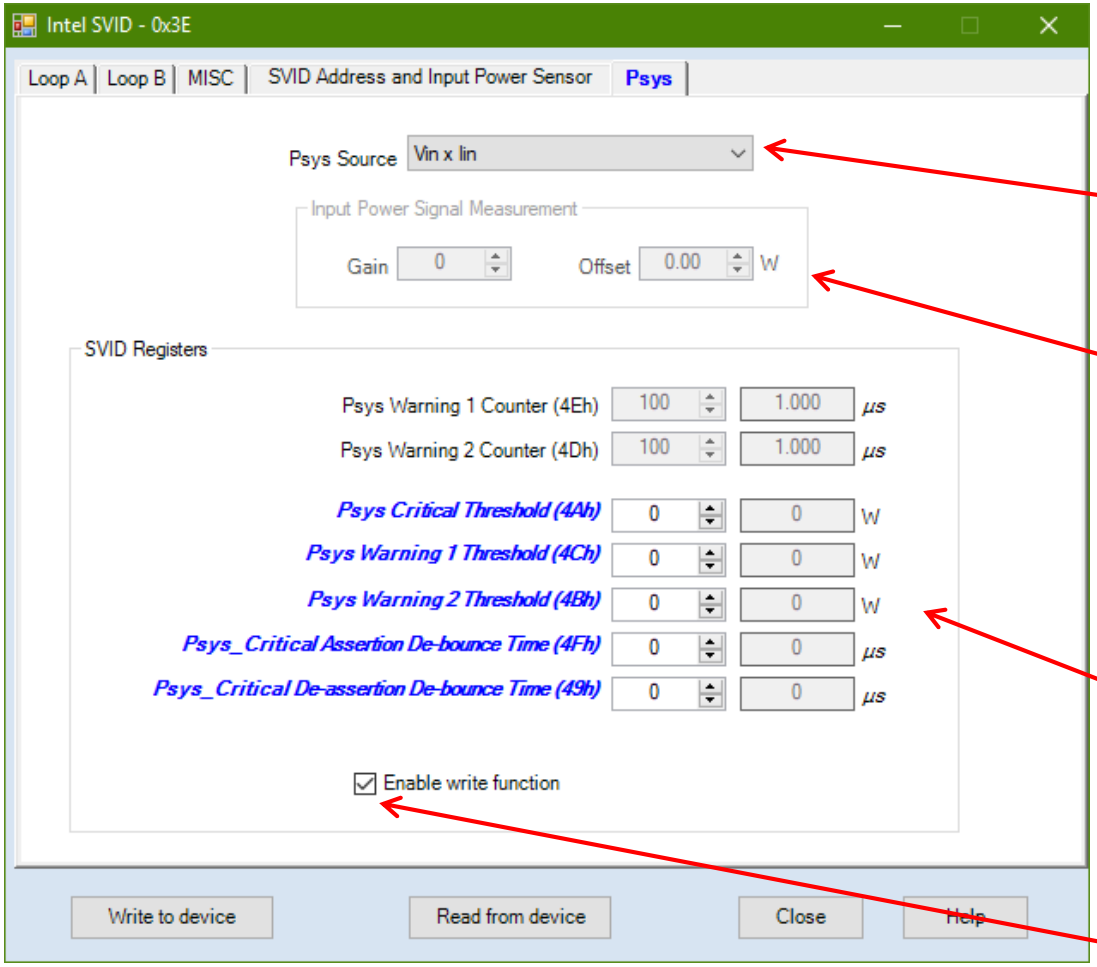
Selection of Input power sensor.

Depending on selections some of the menus may be grayed out as they are not selectable

Allow emulation of SVID via I2C commands

Power state and input power alert **Pin Alert** can be set from GUI when the enable box is marked

SVID... Psys XDPE122xx family



Select which source to use for Psys calculations.

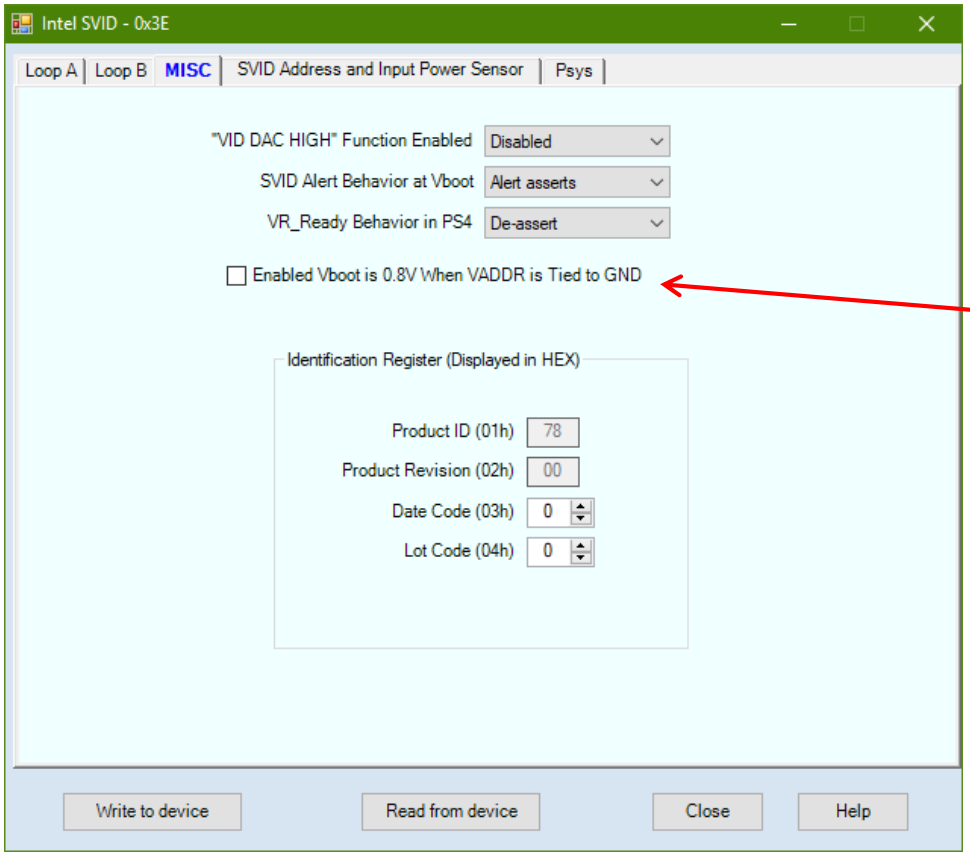
For some Source settings the Gain and offset can be trimmed to make reported input Power match measured values.

Settings for PSYS registers

To be able to write to the registers check this box.

SVID... MISC XDPE122xx family

This window have SVID settings that are not grouped into other functions.

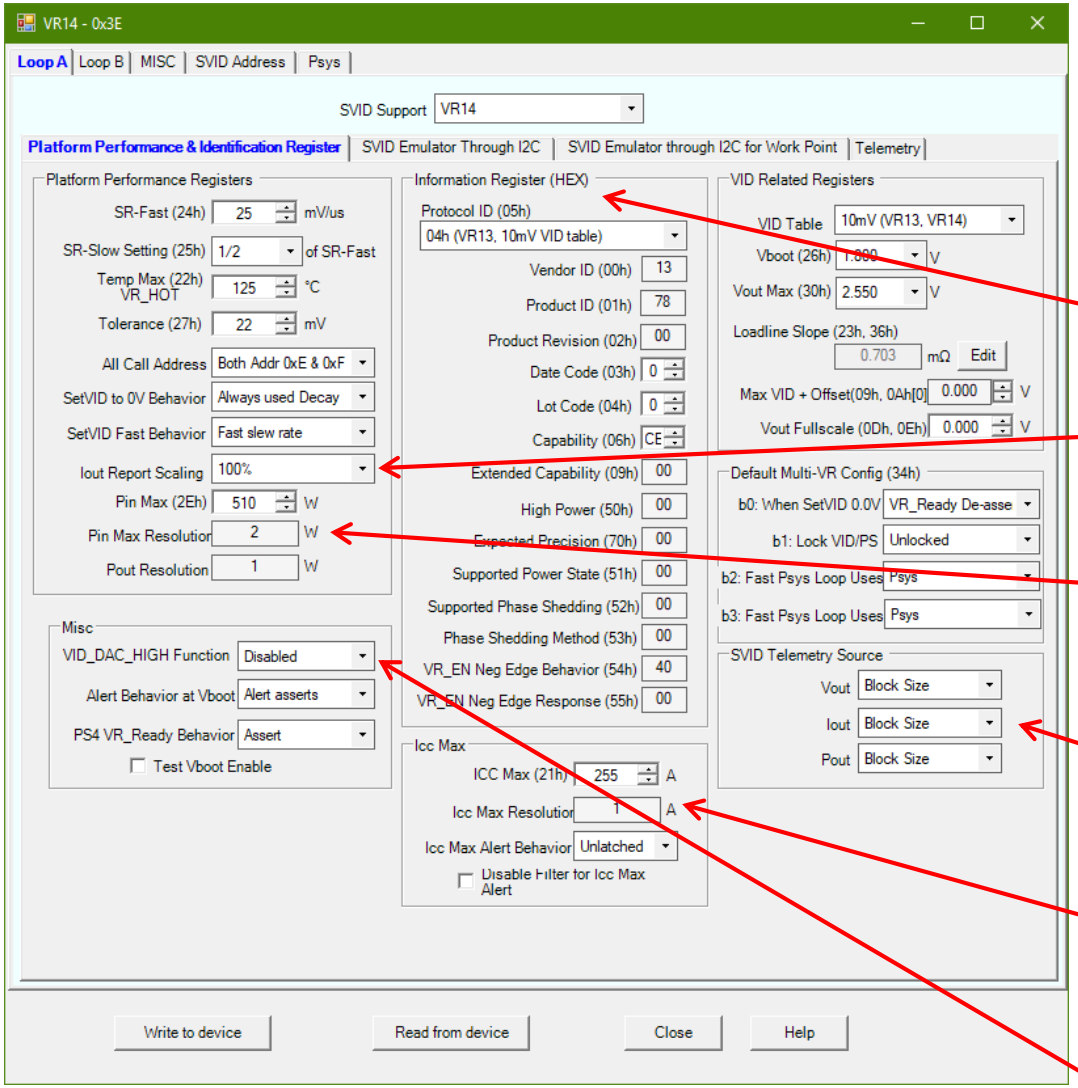


Enable Vboot It is used for testing purpose in production test. In a Vboot=0 application it is not easy to know if the 0Volt means there is an error or not. With function enabled and short vaddr pin to ground, output will go to 0.8V when VREN is asserted.

Using this function, the production can short vaddr pin to GND and measure Vout to determine if the board has any issues before they ship the board.

Agenda

SVID XDPE142xx family (1 of 2)



The Intel SVID window is only available for devices that support SVID. Available settings depend on selected mode VR13, VR13HC, VR14...
For description of the different SVID commands see Intel SVID manual for SVID 1.91

Readout of SVID registers (xxh). Some can be changed others are Read only.

Iout report scaling. Only change the SVID reported current. Other telemetry is still 100%

Pin Max resolution will change automatically in VR14 mode when selecting higher/lower Pin values

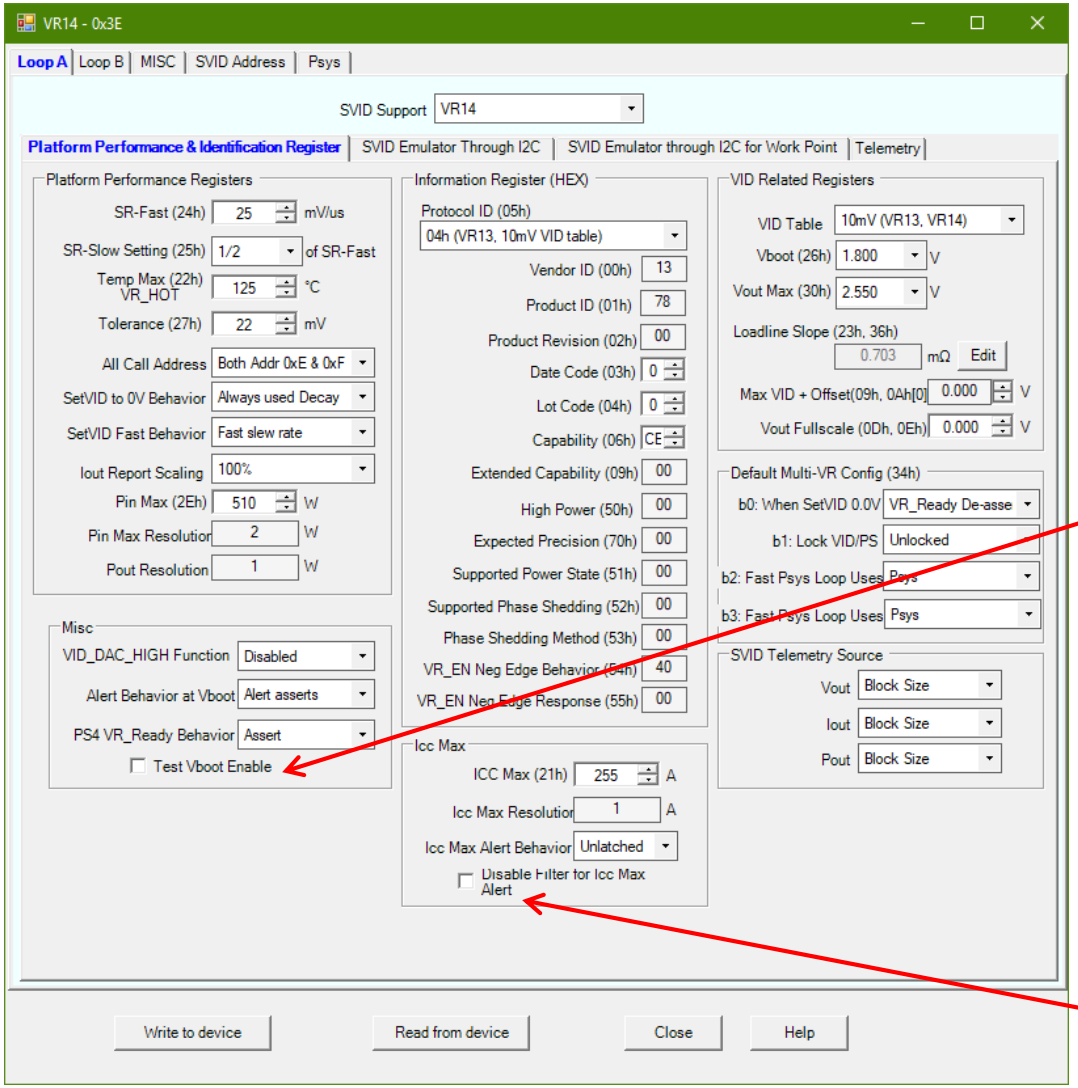
Telemetry source what kind of filter to use.

Slow filter like an analog lowpass filter or a block size that give average of all samples over one full switching period

Current resolution will change automatically in VR14 mode when selecting higher ICCmax than 255A

VID_DAC_HIGH a status indicator in SVID Status1 register if voltage is more than 30mV from the VID target. The status function can be enabled or disabled.

SVID XDPE142xx family (2 of 2)



The Intel SVID window is only available for devices that support SVID.

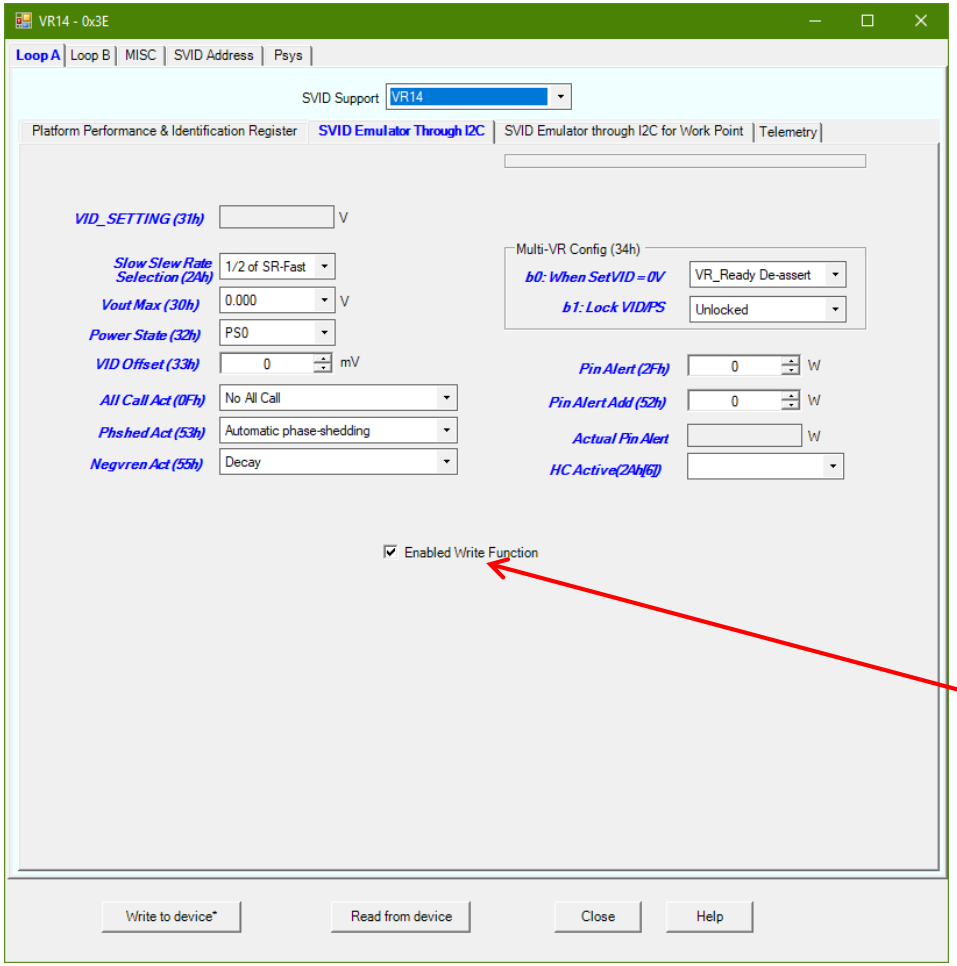
For description of the different SVID commands see Intel SVID manual for SVID 1.91

Test Vboot Enable It is used for testing purpose in production test. In a Vboot=0 application it is not easy to know if the 0Volt means there is an error or not. With function enabled and short xaddr pin to ground, output will go to 0.8V when VREN is asserted.

Using this function, the production can short xaddr pin to GND and measure Vout to determine if the board has any issues before they ship the board.

Disable Filter disables the lowpass filter and uses the instant sampled Icc values for the ICC alert. Makes reaction time fast but can give alerts due to noise in Icc measurments

SVID XDPE142xx family

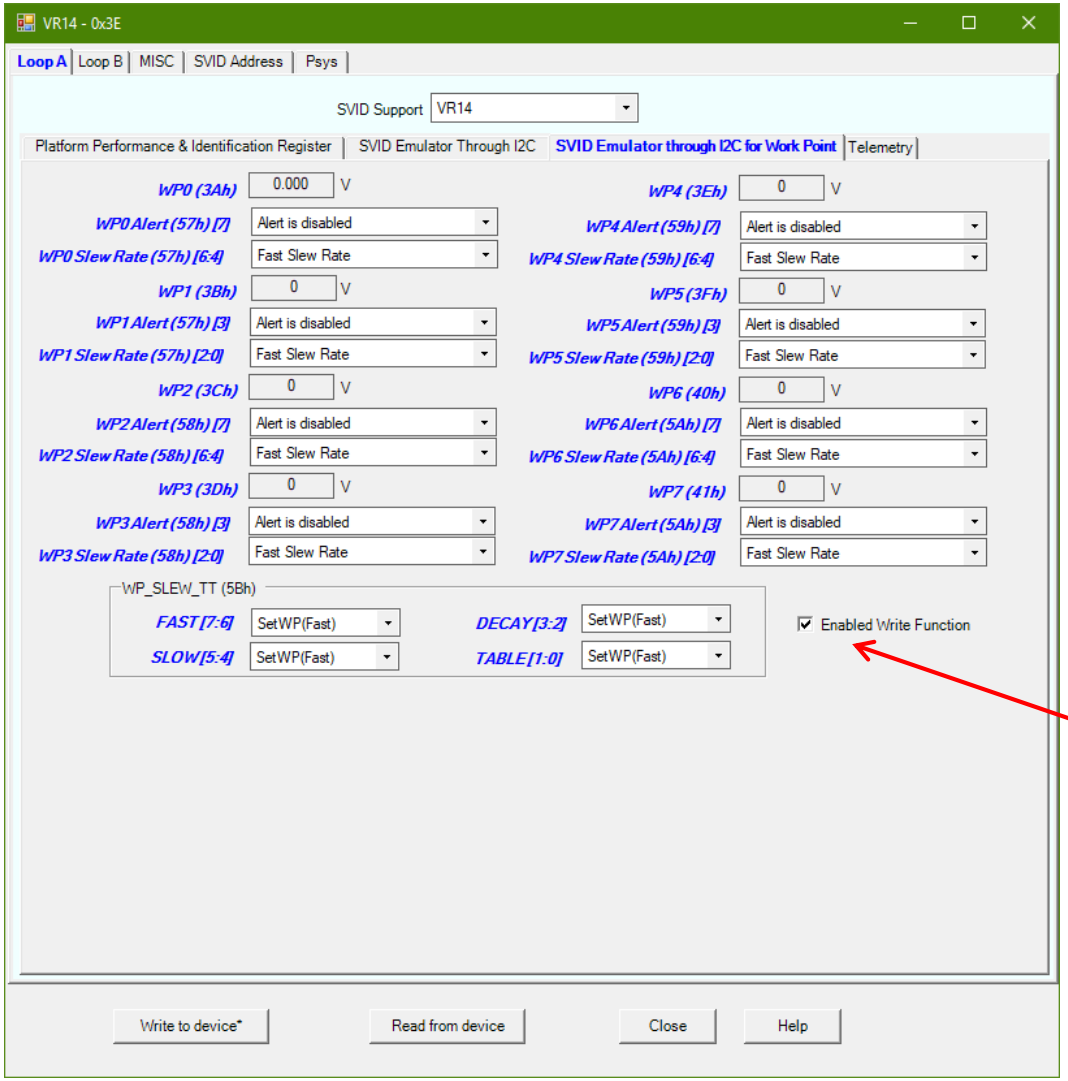


Emulates selected SVID commands using i2c bus to read and write them.

See SVID specification for what the settings do.

To change any value mark the **Enable Write function.**

SVID XDPE142xx family

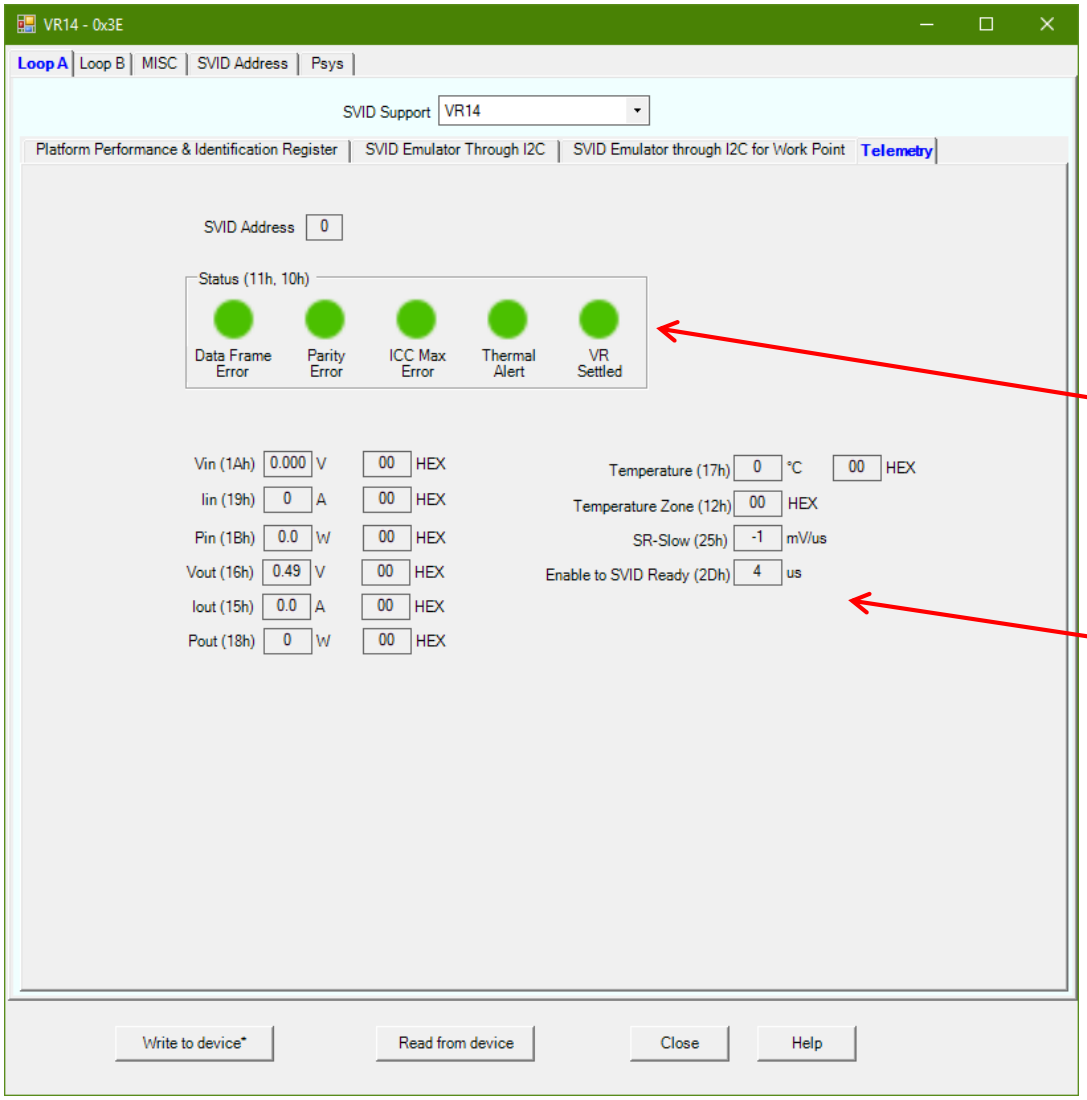


Settings for the different Workpoints.

See SVID specification for what the settings do.

To change any value mark the **Enable Write function.**

SVID XDPE142xx family



Readout for Status and other telemetry readings

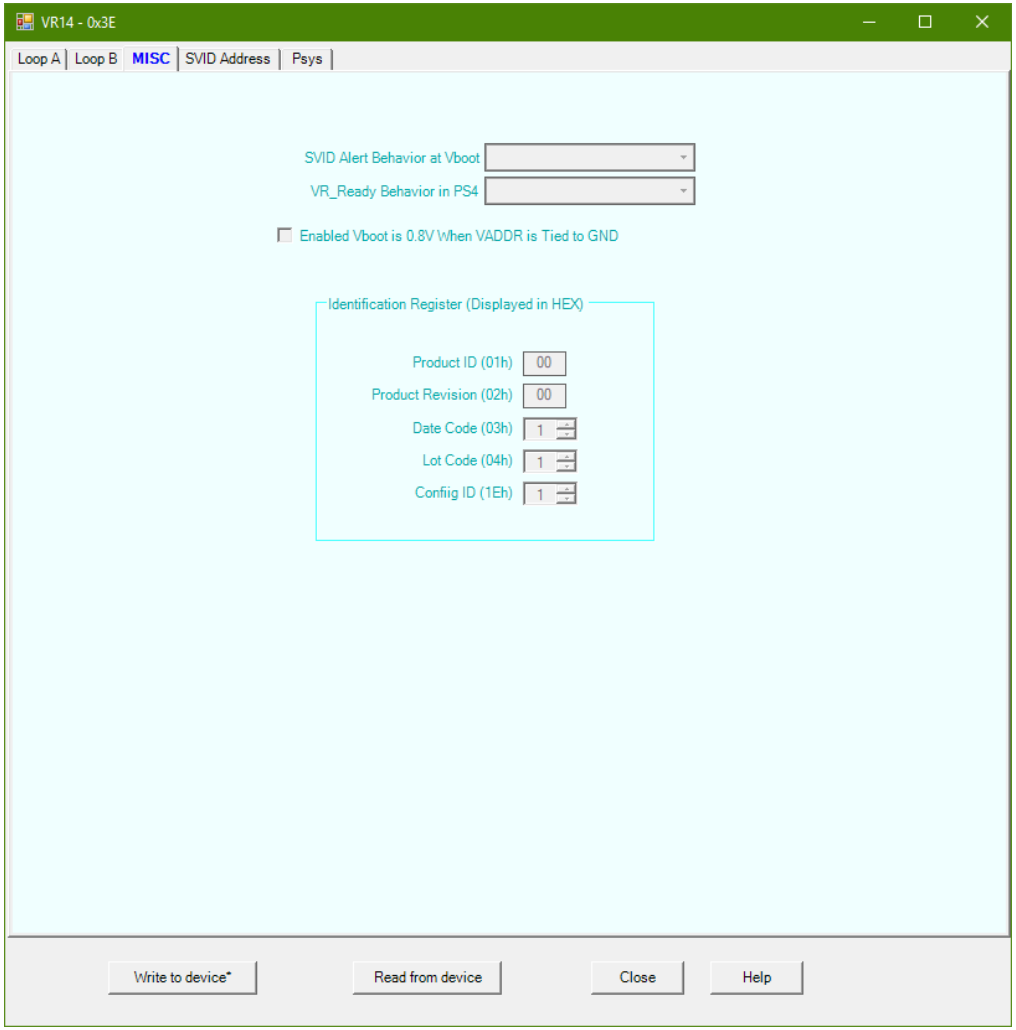
See SVID specification for what the settings do.

Green = there is not fault detected.

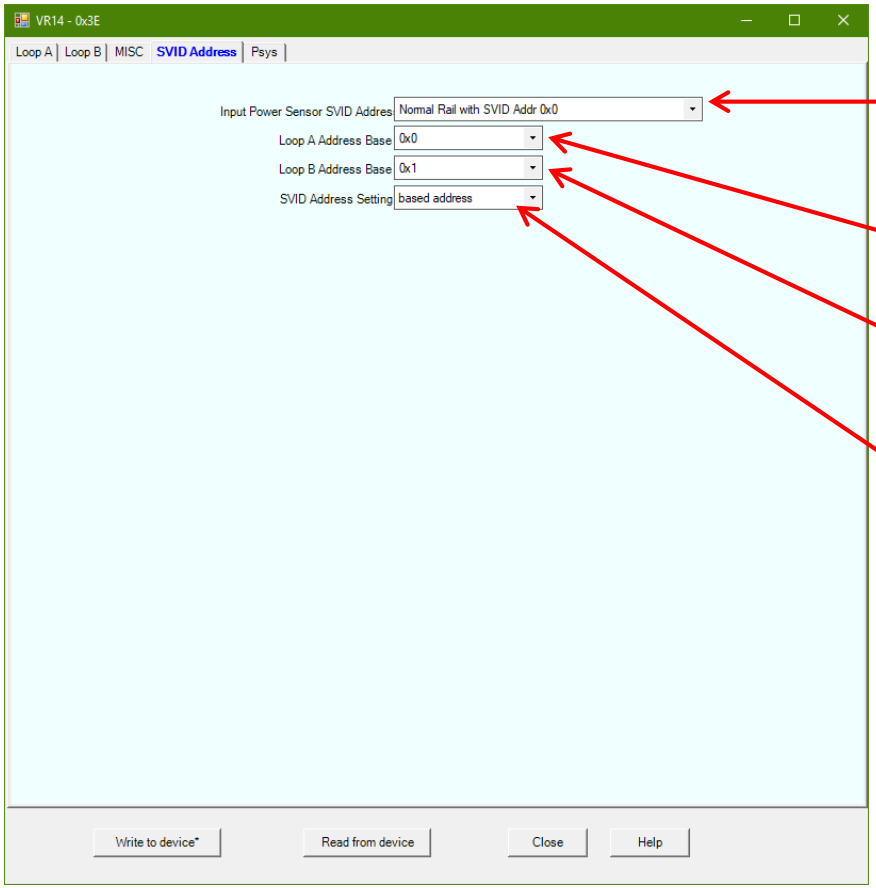
Red = fault detected

Readout of values from registers

SVID XDPE142xx family



SVID XDPE142xx family



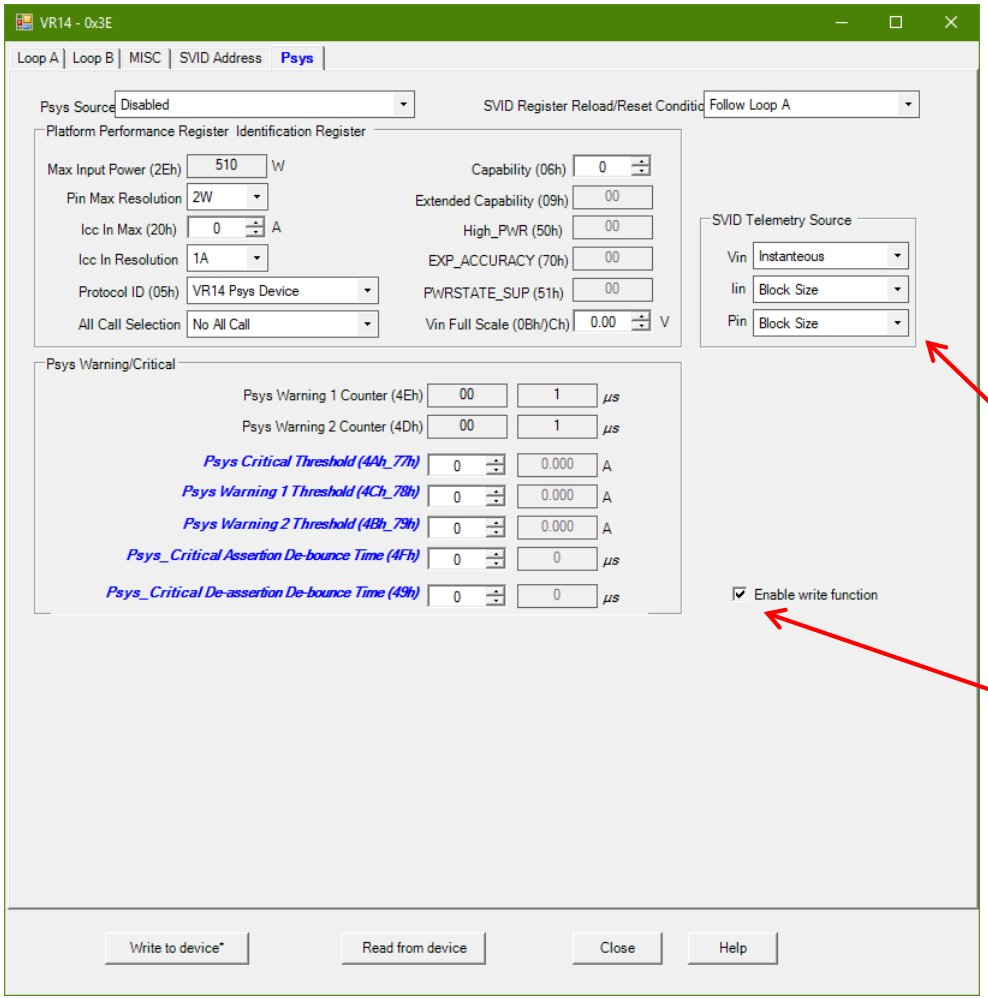
Input Power Sensor SVID address is the address for SVID commands relating to input power.

Loop A address Base is the address for SVID commands for loop A. typical set to 0x0

Loop B address Base is the address for SVID commands for loop A. typical set to 0x1

SVID address Setting select if the address should look at the external resistor that can set an offset to the Base address

SVID XDPE142xx family



Readout for PSYS settings

See SVID specification for what the settings do.

Telemetry source what kind of filter to use.

Vin

Instantenious or Slow filter. Instantenious is immediate latest sample while Slow is like a analog lowpass filter

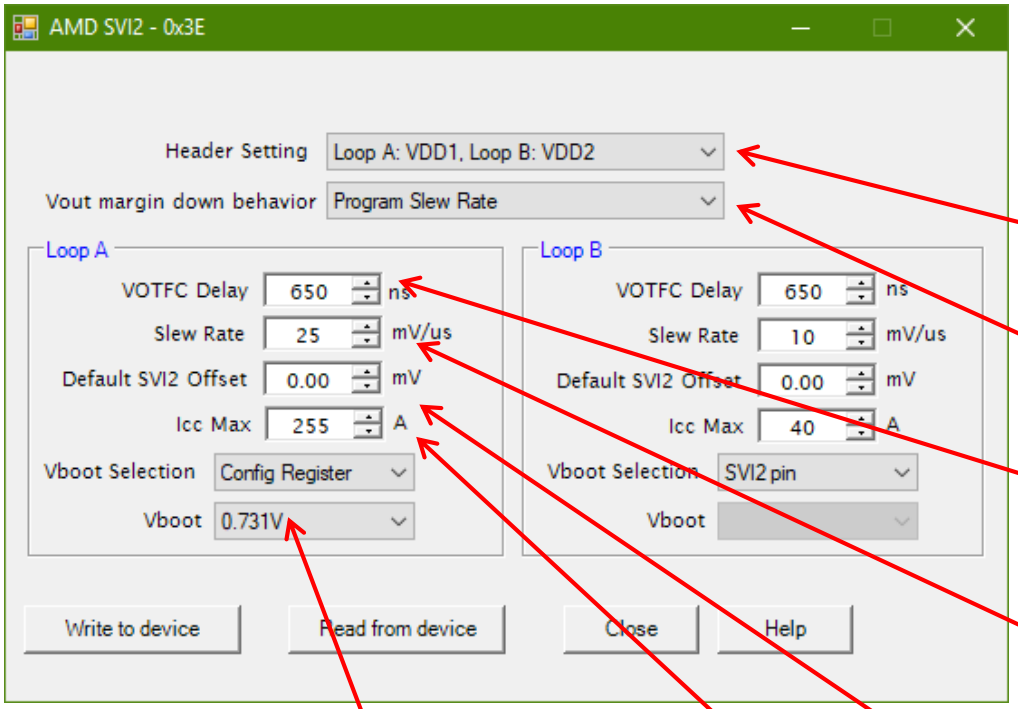
Iin, Pin: Slow filter like an analog lowpass filter or a block size that give average of all samples over one switching period

To change any value mark the **Enable Write function.**

Agenda

AMD SVI2...

This window contains the settings relevant to SVI2 operation to meet AMD requirements



Header Setting
Controls which of loop A and B are assigned to VDD1 and VDD2.

Vout Down behavior
Select if decay or slew voltage down

VOTFC Delay: Voltage On The Fly Complete signal. Can be set to delay the VOFTC signal after Vout ramp completed. Example: in case of a small overshoot the delay allow Vout to stabilize

Slew Rate is the setting for how fast voltage changes after a SVI2 or manual voltage command. Typical 25mV/us

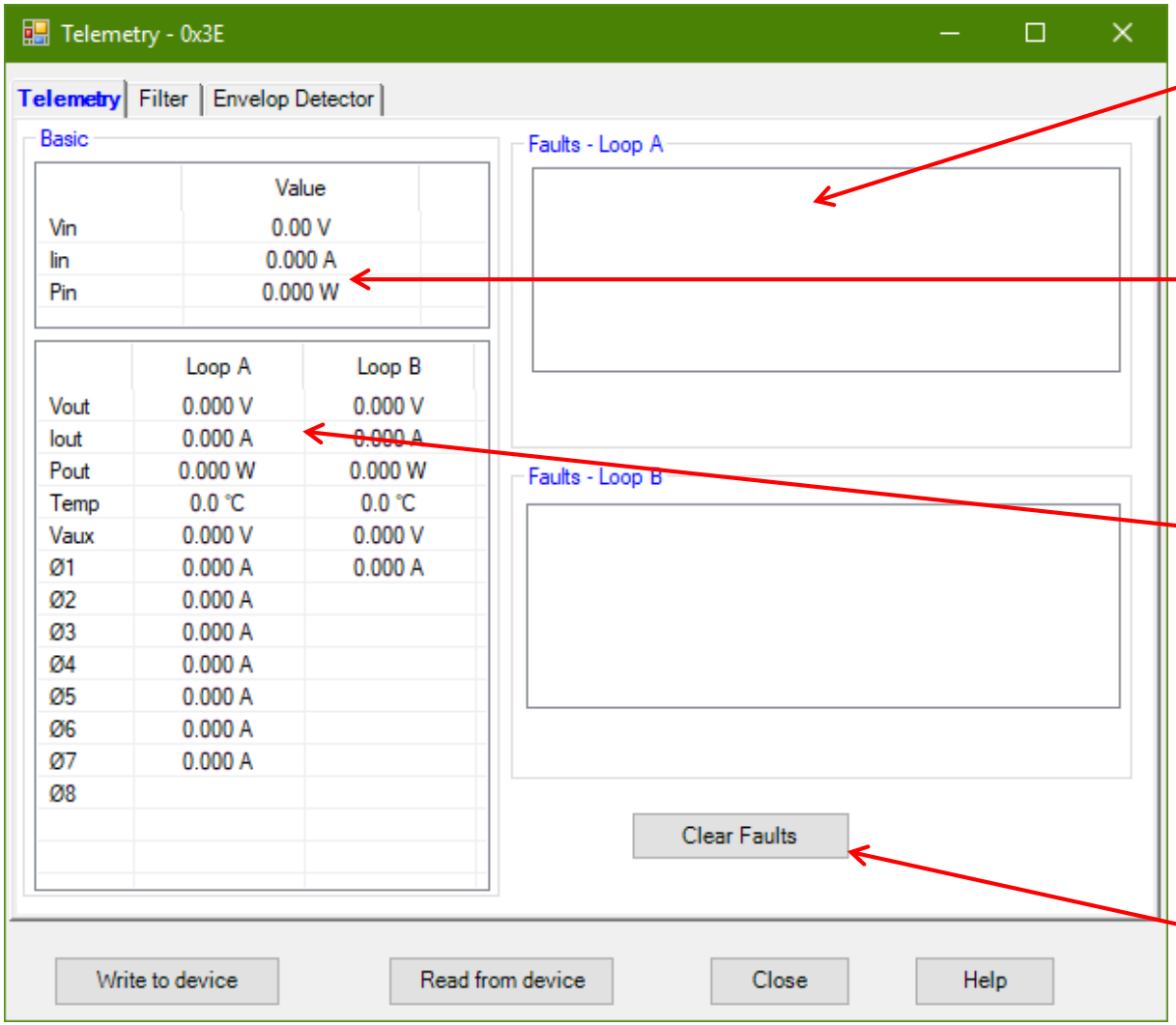
Default SVI2 Offset
Compensation for any offset from the requested SVI2 voltage level to what Vout really is.
On a design where the Vout do not match the SVI2 voltage this offset can be adjusted.
Reason for offset can as example be layout of the PCB causes some small voltage drop.

Icc Max is the setting for full scale current for the reporting via the SVI2 bus. Set it to the maximum current expected.

Vboot selection
Select if boot voltage is selected by the SVI2 pins or read from configuration Vboot. When **Config Register** selected it is possible to set the Vboot voltage here.

Agenda

Telemetry…



Faults
Shows what faults are detected

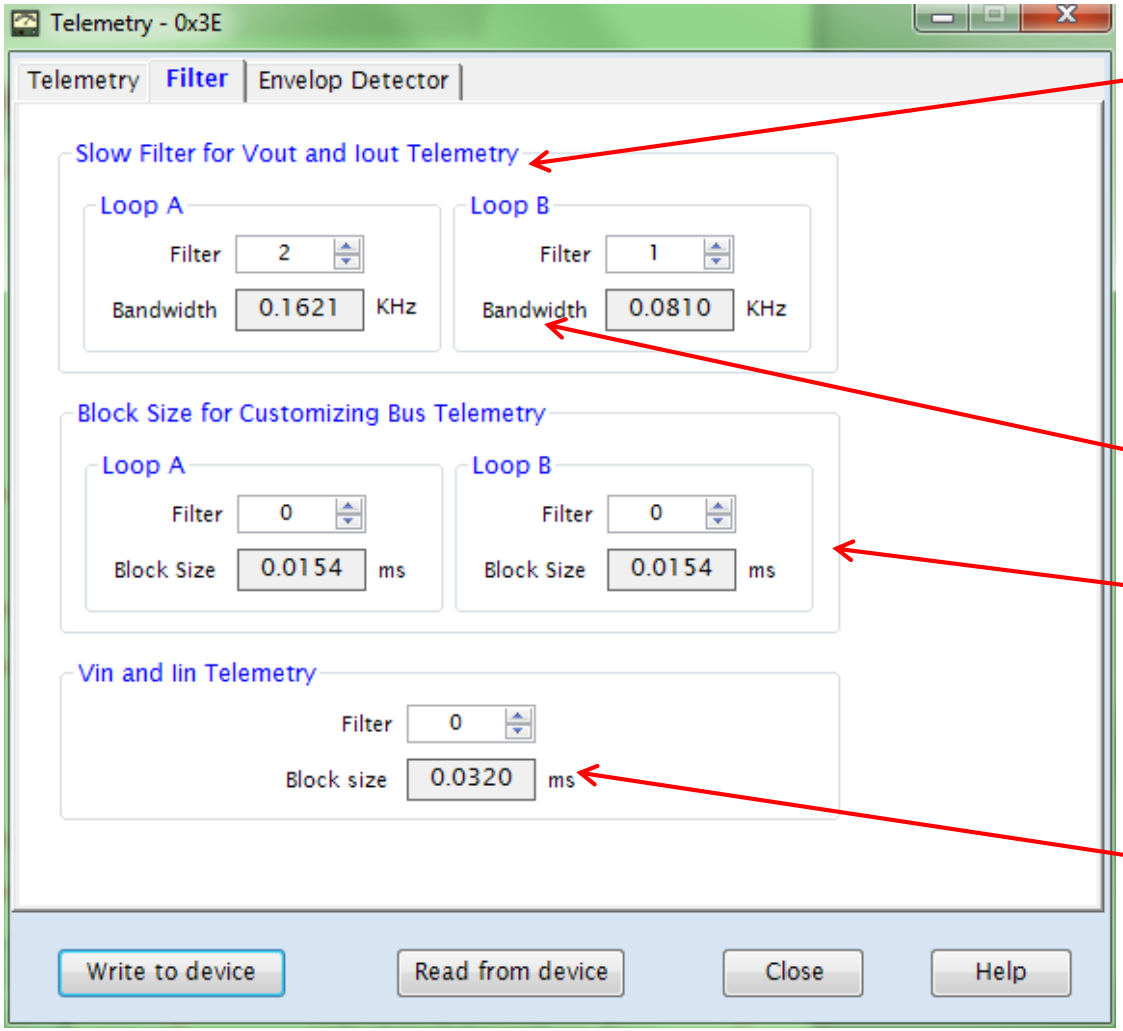
Basic
Shows measured values for input Voltage, Current and the calculated input Power

Loop A and loop B measurements
Shows measured values.
For the phase currents some phases may show 0A due to not all phases active. Typical for low load currents where i.e. Only 2 phases are active. Then it will show 0 A for the other phases as they are not active for the moment.

Vout values are filtered and sampled and due to sampling behavior and resolution in filter there can be up to a 0.25% error in reported Vout

Clear Faults button
Click this button to clear a fault.
Notice this only works if the fault condition is no longer existing. Otherwise the fault will immediately be listed again.

Telemetry... Filter



Slow Filter for Vout and Iout Telemetry

Adjusts the bandwidth of the slow telemetry filter. This is a single pole low-pass filter. Each telemetry component (Iout, Vout) has its own independent slow filter. However, the adjustment of the bandwidth is common to all slow filters for the same Loop.

Bandwidth

Indicates the bandwidth of the Slow Filter

Block size for SVID/SVI2 Telemetry

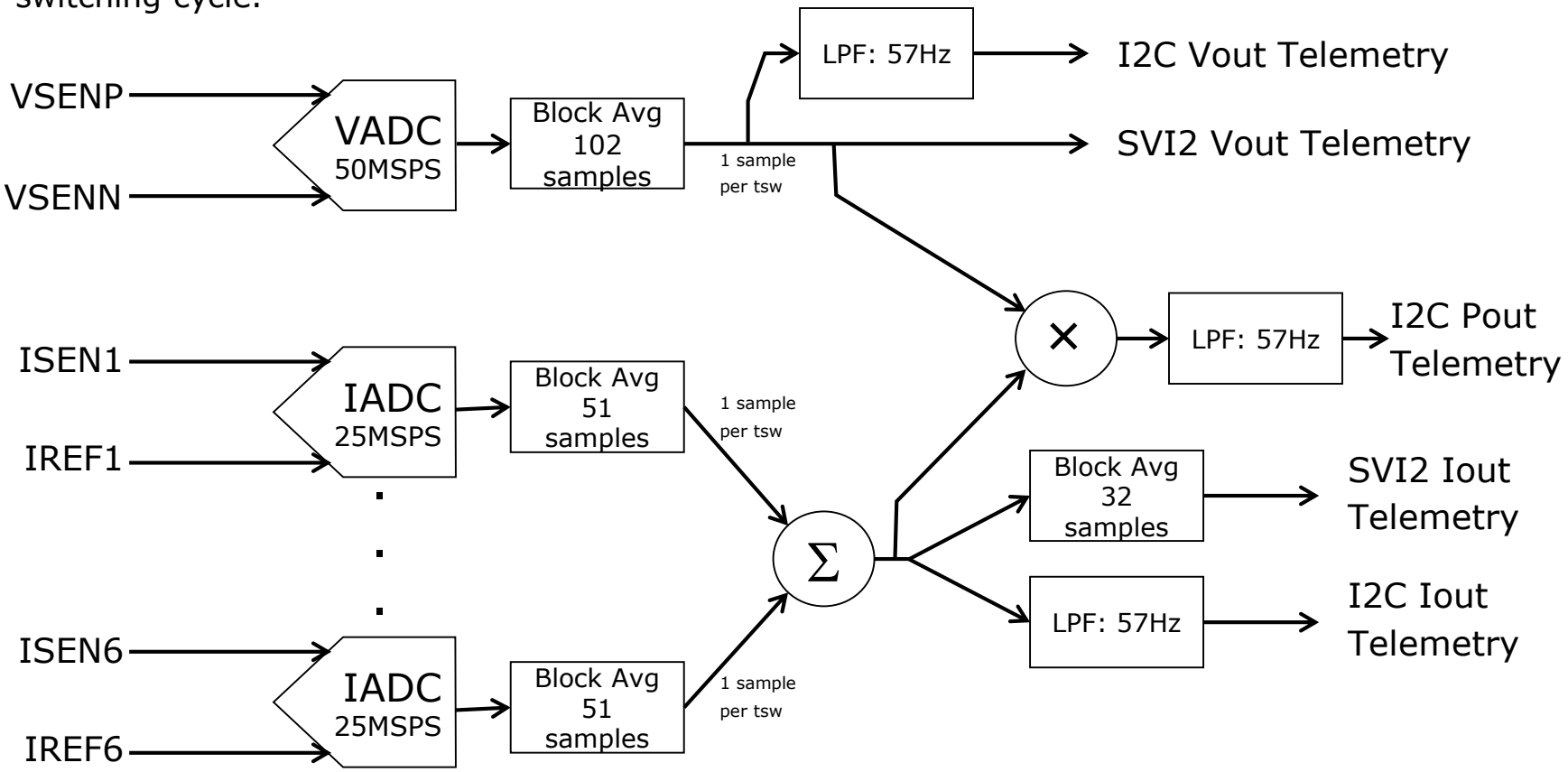
Adjusts the block size for the average value to be taken across for the fast telemetry. The fast filter calculates the average across a block of data at a time (different from a moving average).

Block Size

Block size of Input Voltage and Current telemetry. Set the length of time of the "block" that average the samples

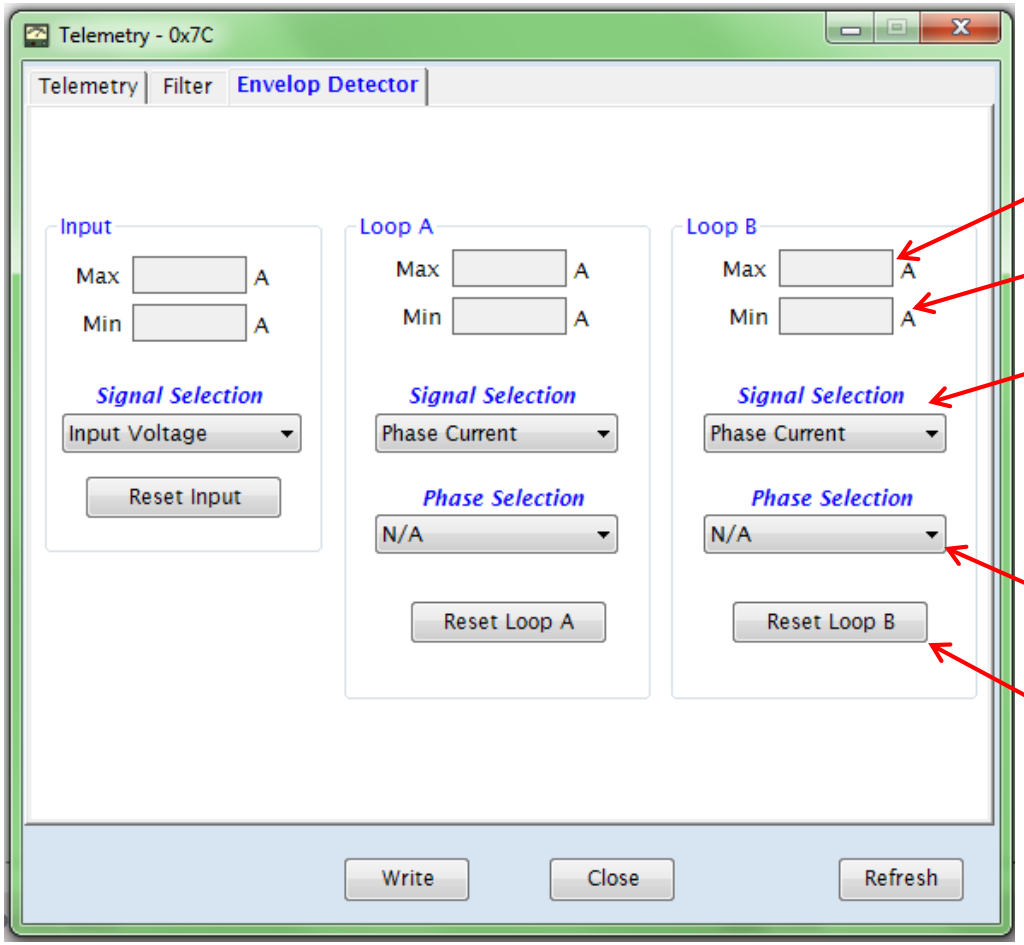
Telemetry… Filter theory

The ADC's are oversampling the inputs. For Vadc, there are 102 samples taken per switching cycle. For Iadc, 51 samples are taken in the same time period. These numbers depend on the switching frequency chosen. As fsw changes, the number of averaging samples will be different since the ADC sample rate is fixed. The averager will average all the samples in 1 switch cycle and output a block averaged number. Hence, the update rate of the ADCs for telemetry used is 1 block averaged sample per switching cycle.



*Above filter rate and samples is for a 490kHz switching frequency. Will change depending on filter setting and Switching frequency

Telemetry... Envelop Detector



Max
Maximum measured value of the selected Signal Selection

Min
Minimum measured value of the selected Signal Selection

Signal Selection:
Enables/disables of the envelope detector
Available Signals: Phase Current, Total Current, Output Power, Input Voltage, Output Voltage, Input Current, Input Power

Phase Selection
Available when Signal Selection -Phase Current signal is selected

Reset
Resets the Max and Min values recorded

Agenda

Multi Function... Pin Settings

The Multi-Function dialog gives the user access to the configuration settings pertaining to the fault pins on the device. The configuration settings allow users to:

- Enable or disable pins
- Map specific faults to external pins
- Configure how the pins are driven for system compatibility
- Firmware functions

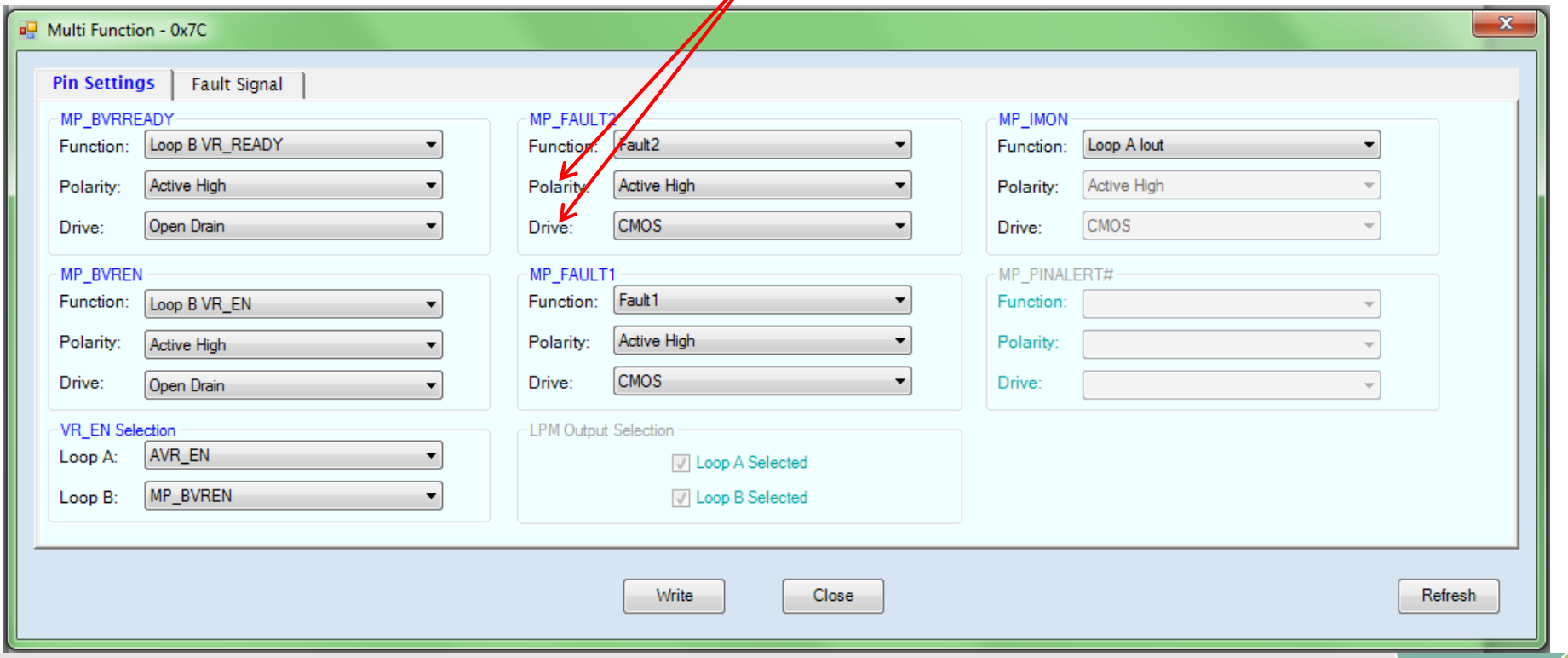
For all pins there are some common settings

Drive

- Output Buffer type to be use for the pin
- Open Drain: can pull to GND, need an external resistor for pullup
- CMOS: Actively driven output signal

Polarity

- Logic signal polarity for the pin. Should it be High or Low level when the related signal is active.



Multi Function... Pin Settings

Depending on selected part some selections may be grayed out and not available.

MP_BVRREADY Function
- Function that will be mapped to **MP_BVRREADY** pin

MP_BVREN Function
- Function that will be mapped to **MP_BVREN** pin

VR_EN Selection
- Pin that will be use for VR_EN function for a specific loop

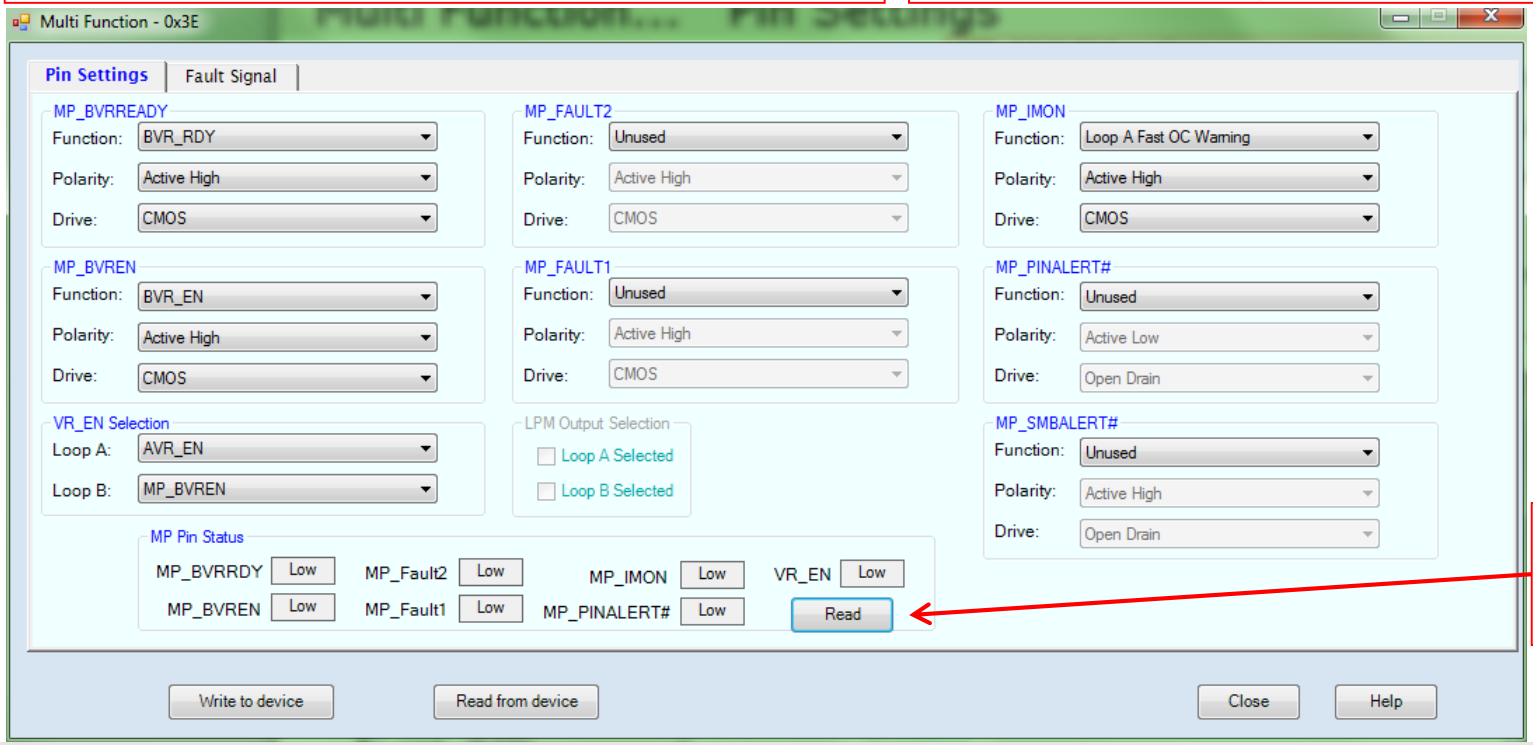
MP_FAULT2 Function
- Function that will be mapped to **MP_FAULT2** pin

MP_FAULT1 Function
- Function that will be mapped to **MP_FAULT1** pin

LPM Output Selection
- Low power mode selector that asserts the signal when the selected loop is either disabled or in PS4 active only when LPM is selected for a pin.

MP_IMON Function
- Function that will be mapped to **MP_IMON** pin

MP_PINALERT# Function
- Power In alert,



MP Pin status
Click Read button to see status of the different Pins

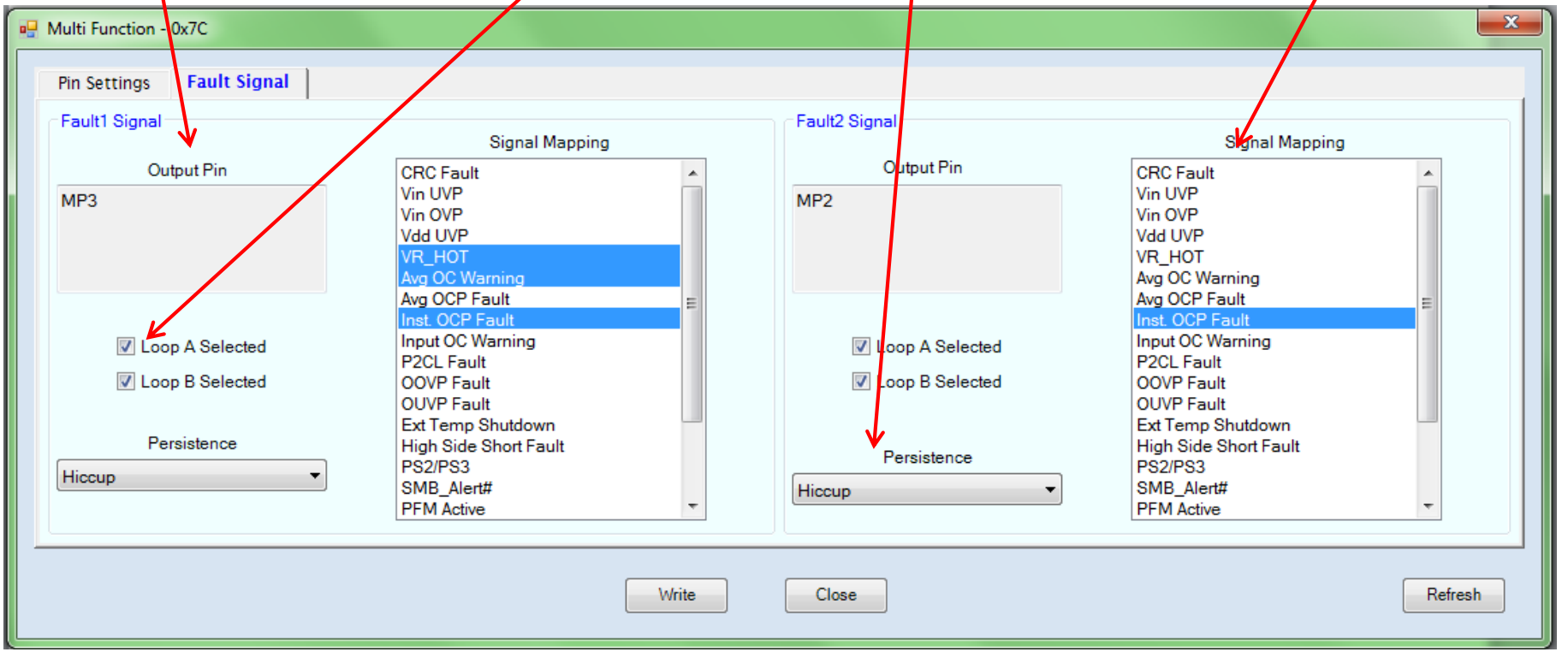
Multi Function... Fault Signal

Output Pin
Displays which controller pin the Fault1/2 signal will be routed to. Pin selected in previous tab

Loop A/B Selected
Checked: selected fault(s) from the corresponding loop(s) will be routed to the output pin
Unchecked: no fault from the loop will be routed to the output pin

Persistence
Duration of the indicated fault before being cleared
Latch: de-asserted by toggling OE, recycling 3.3V or sending CLEAR_FAULTS
Hiccup: de-asserted if fault condition is removed

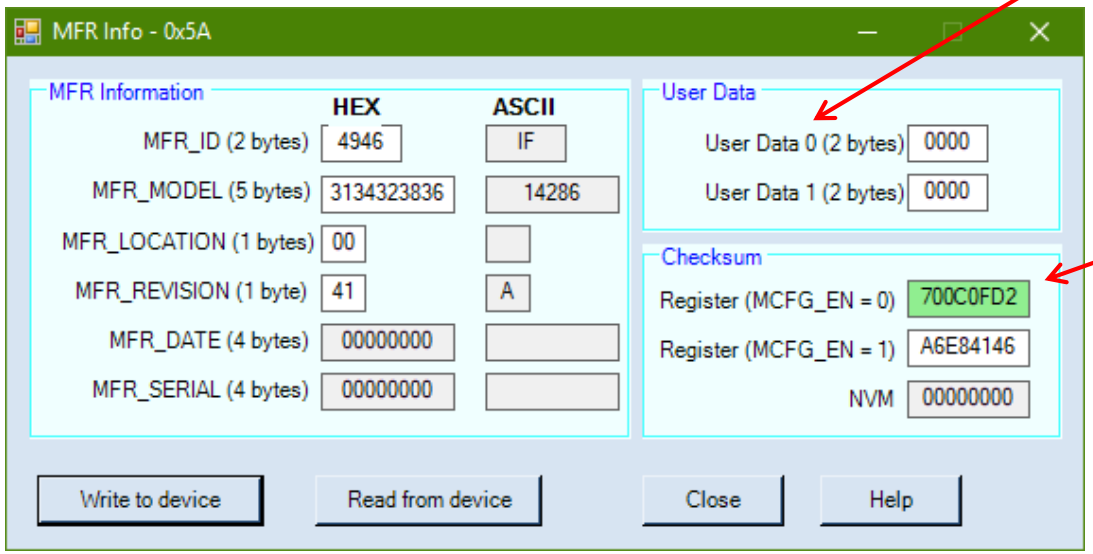
Signal Mapping
Selection panel for which fault signals should be reported and sent out to the Fault pin. Multiple Signals can be selected. Signal which is sent out will still appear in the Telemetry/Fault Detail



Agenda

Manufacturer Info...

MFR Information (Manufacturer Information)
MFR_ID (2 bytes)
2-byte programmable
MFR_MODEL (5 bytes)
5-byte programmable i.e partnumber in ASCII format
MFR_LOCATION (1 bytes)
1-byte programmable
MFR_REVISION (1 bytes)
1-byte programmable
MFR_DATE (4 bytes)
Reserved by Infineon for storing vendor log data
MFR_SERIAL (4 bytes)
Reserved by Infineon for storing vendor log data



User Data
memory location where a User can store any data.

Checksum
Register : Displays the cyclic redundancy code value calculated by PowerClient based on the current register values. Depending on use of multi-config or not it will be 2 different checksums
NVM (permanent memory in device): Displays the cyclic redundancy code value calculated by the device during download

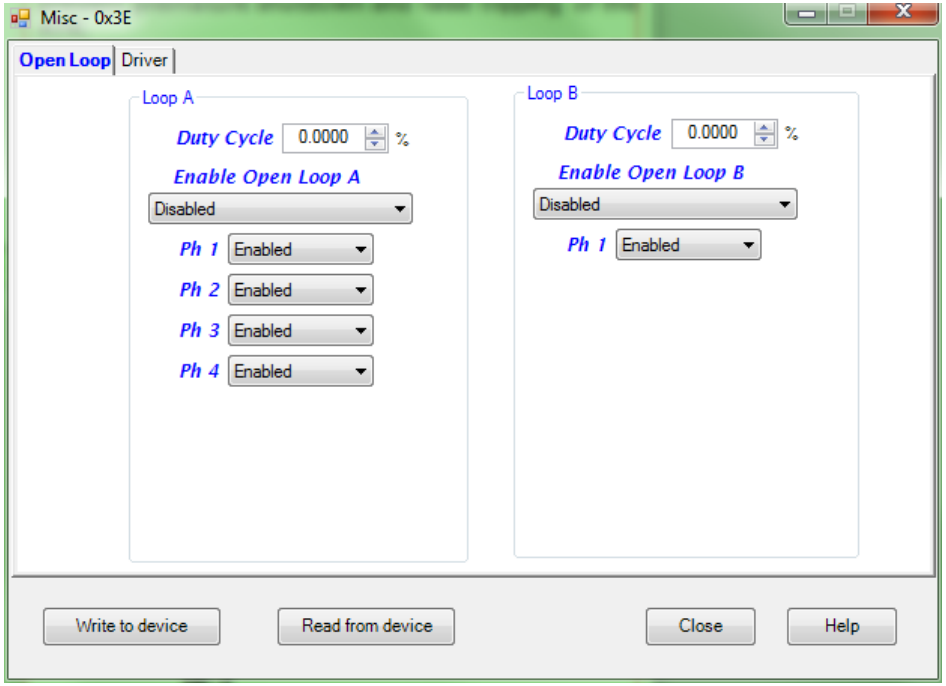
Agenda

MISC... Open Loop

Duty Cycle
- Fixed duty cycle in open loop

Open Loop Behavior
- *Disabled*: Open loop is disabled
- *Close Loop with Phase Control*
- *Open Loop with Phase Control* controller will send out a fixed **Duty Cycle** .

PH 1/2/3/4/5/6
- *Enabled*: phase 1/2/3/4/5/6 will operate in open loop test
- *Hi-Z*: phase 1/2/3/4/5/6 is not activated.



In open loop mode, output voltage faults (OUVP) protection and all ATR events must be disabled to prevent premature shutdown and false tripping of the ATR.

Step 1: (Important) make sure VR is turned off. i.e. Enable signal low
- It is strongly recommended that the VR be disabled when the user is disabling/enabling open loop function. Otherwise, undesired damage may occur at the power stage.

Step 2: Select the **Open Loop Behavior**
Closed Loop with Phase control
or
Open Loop with Phase Control

Step 3: Set the **Duty Cycle**
- Should be greater than 0%
- To check whether the power stage is operating, a low duty cycle is recommended, typically ~ 10%.

Step 4: Select **PH** x behavior for each Phase
Enabled
or
Hi-Z

Step 5: Click the **Write** button to activate the settings

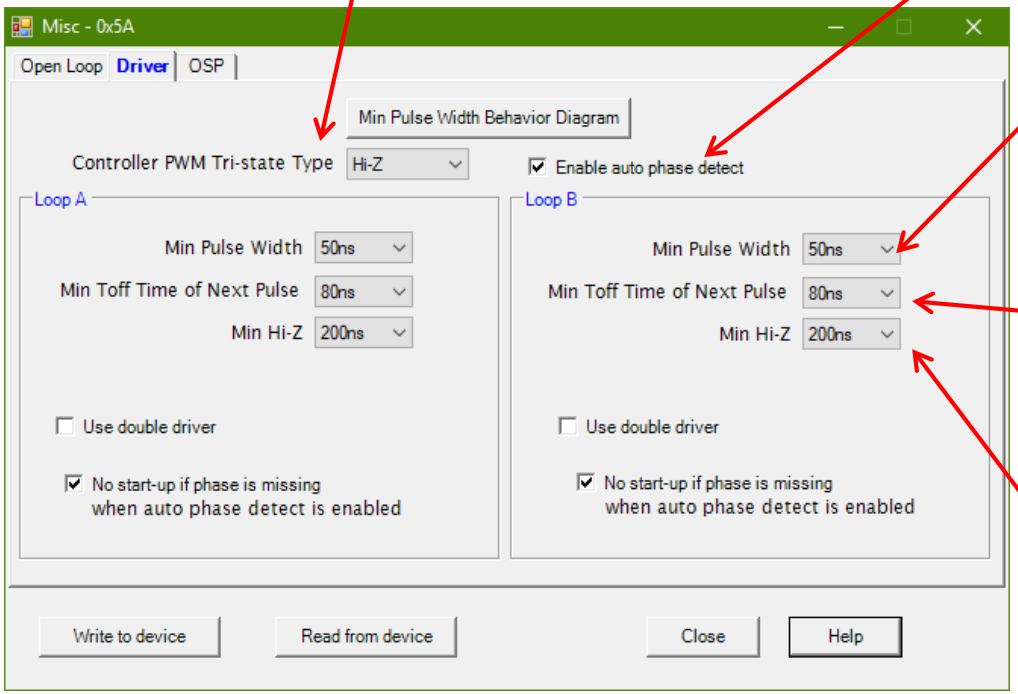
Step 6: turn on regulator i.e. by enable signal

MISC... Driver

Controller PWM Tri-state type

1.5V: PWM will be forced to 1.65V when controller would like to turn off both HSFET and LSFET. This setting is used for drivers which do not have an internal divider to force a Tri-state condition.

Hi-Z: PWM will stay hi impedance when controller would like to turn off both HSFET and LSFET. The voltage on the PWM for Hi-Z will be determined by the driver's internal divider and any stray capacitance may delay the entry to Tri-State.



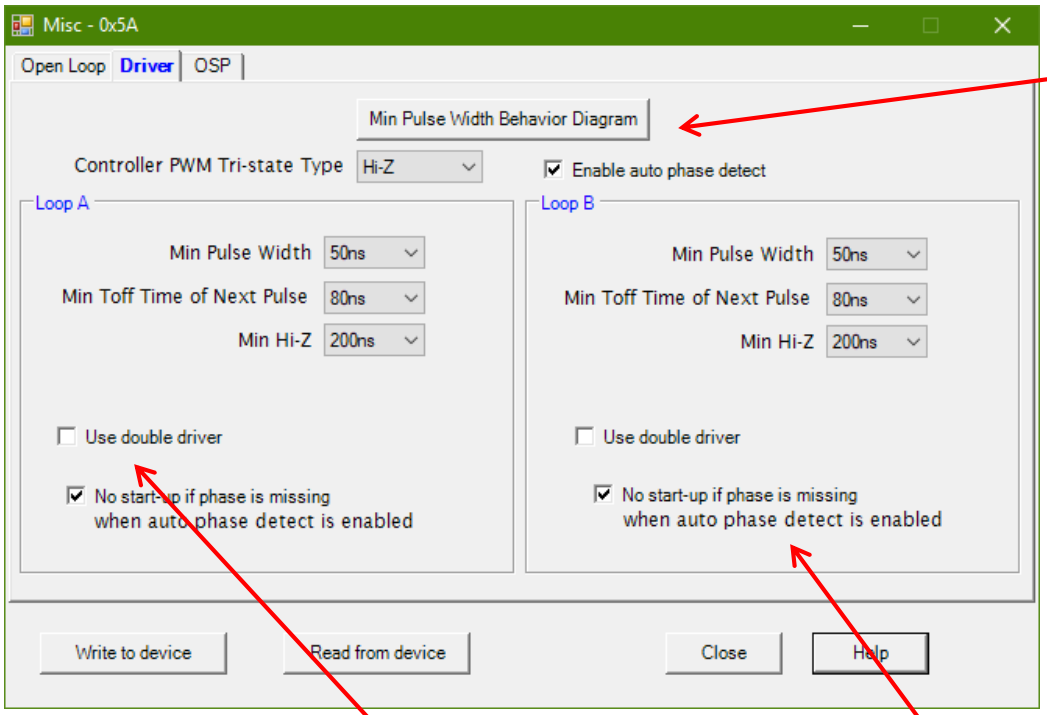
Enable auto phase detect:
During startup the controller can measure each PWM signal and detect if there is a powerstage connected or not.

Min pulse width
Some powerstages do not work well if the PWM is too short. This setting allow to set what the shortest PWM pulse width is to match the need of the powerstage.

Min Toff Time
Minimum time off between PWM pulses

Min Hi-Z
Minimum time for the Hi-Z output.
Allow time for the PWM signal to reach the Hi-Z status as it is not active driven.
Stray capacitance can make it a longer time to enter Hi-Z status and therefor a longer time is needed

MISC... Driver



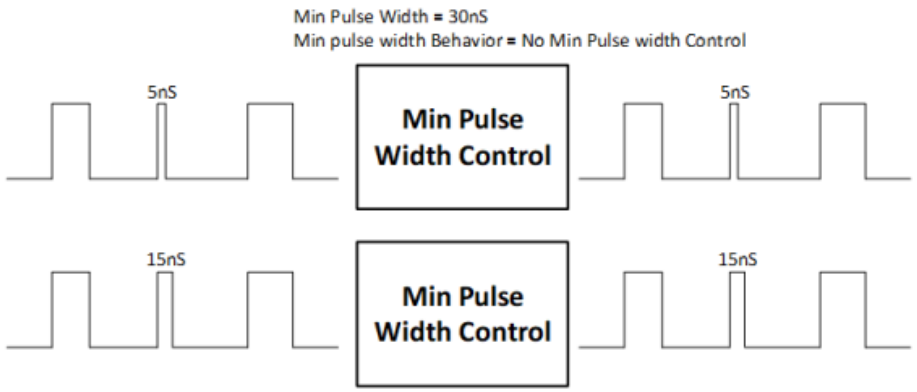
Behavior Diagram
Gives a visual explanation of the different settings and how PWM pulse is treated. See next page in this presentation for diagrams.

Use Double driver
In systems with many phases i.e. 16 a doubler driver can be used that split the PWM signal to two separate Powerstages. But it divide the frequency at same time. Marking this box make controller to know and double switching frequency and know a doubler is used.

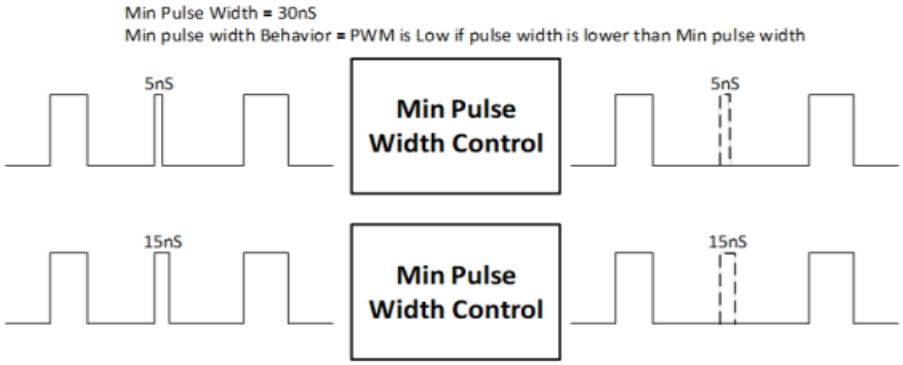
No startup if phase missing:
If the detection of PWM outputs during startup find a not connected powerstage a selection can be mad to start up anyway or not start if all expected powerstages are not detected

MISC... Driver

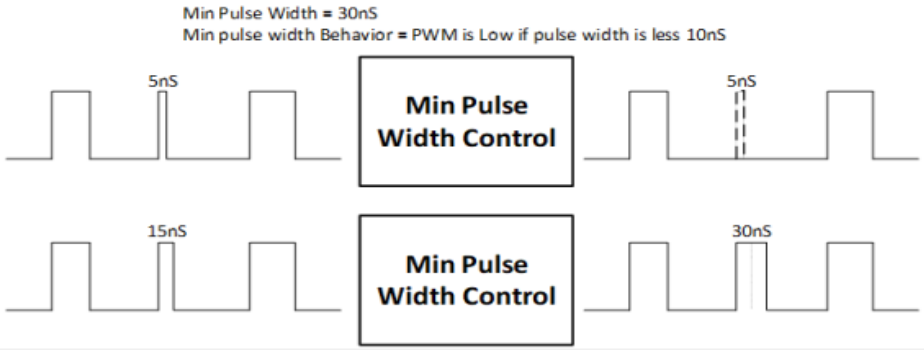
- 1
- No Action



- 2
- Suppressed

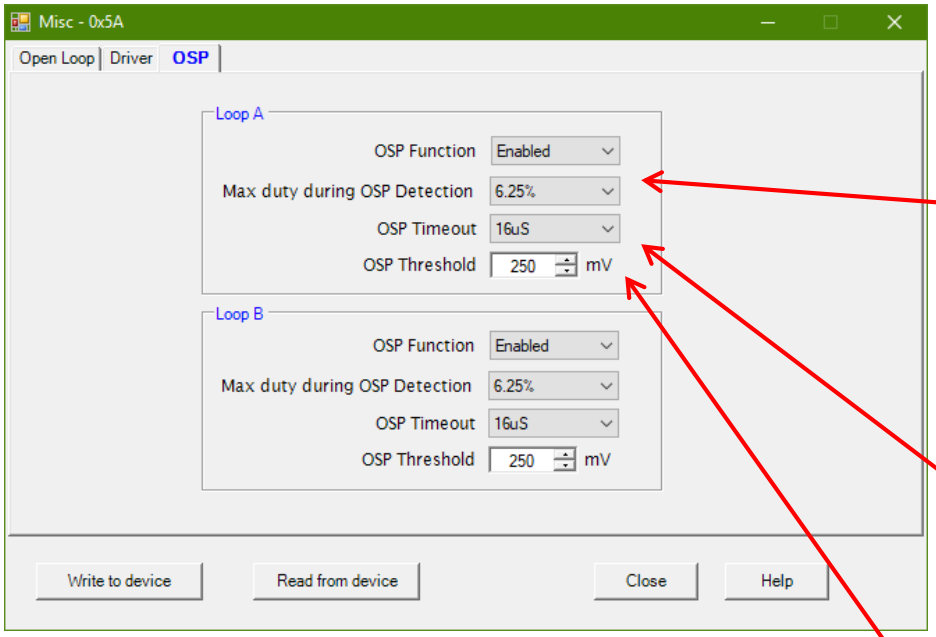


- 3
- Suppress if less than 10us
- Stretch to the set value if longer



MISC... OSP

OSP Output Sense protection
In case of shorted or open feedback this function try to detect this and stop switching if output voltage is not above a threshold within a certain time.



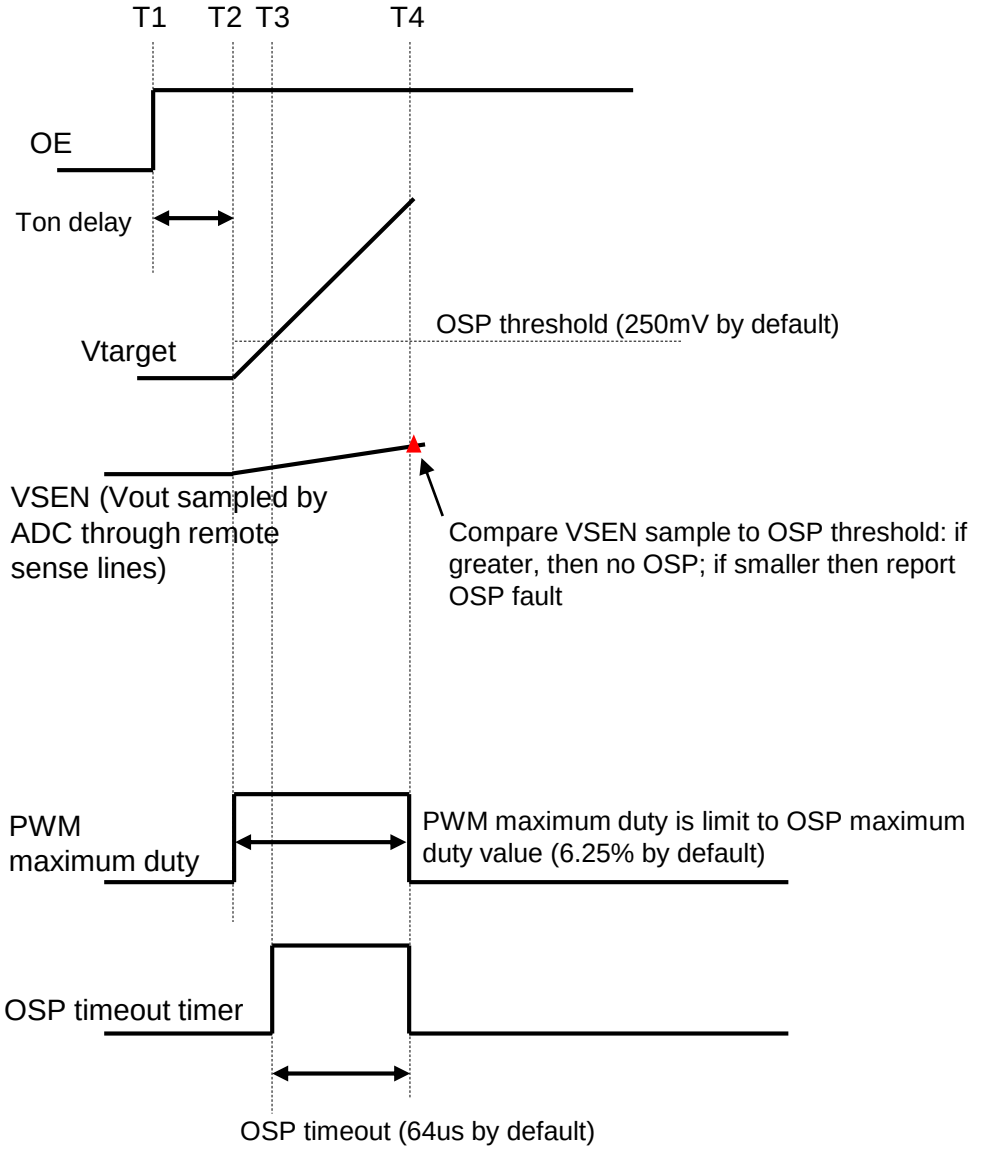
Max Duty during OSP detection
Limits the dutycycle and the output voltage during startup.
Typical 6.25%

i.e. With 12 Volt input and max 6.25% dutycycle Vout can reach 0.75 Volt

OSP timeout
How long time is allowed for Vout to reach the threshold before turning off and signal OPS fault.
Typical 64us When using slow startup slew rates 1mV/us or less the timeout have to be longer 128us.
Or even disable OSP function in these cases.

OSP threshold
Voltage expected to be higher than this within the set time to continue normal startup.
Typical 250mV

MISC… OSP timing diagram



- T1: Output enable is asserted.
- T2 (Ton delay after T1)
  - Internal Vtarget starts ramping if Vboot=non zero (note: if Vboot=zero, then no OSP detection until Vtarget starts ramping because of VID change commands.
  - VSEN (Sampled Vout through the differential voltage across remote sense lines):
    - Normally VSEN follows Vtarget.
    - However if remote sense lines are shorted or open, then VSEN voltage can be be near zero.
  - PWM maximum duty is limit to OSP maximum duty cycle from T2 to T4. (this prevent Vout from going too high in case of open feedback)
- T3:
  - Vtarget reaches OSP threshold.
  - OSP timeout timer starts timing.
- T4:
  - OSP timeout timer is expired.
  - Compare VSEN sample to OSP threshold: if greater, then no OSP; if smaller then report OSP fault.
  - PWM maximum duty limit goes back to nominal maximum duty limit.

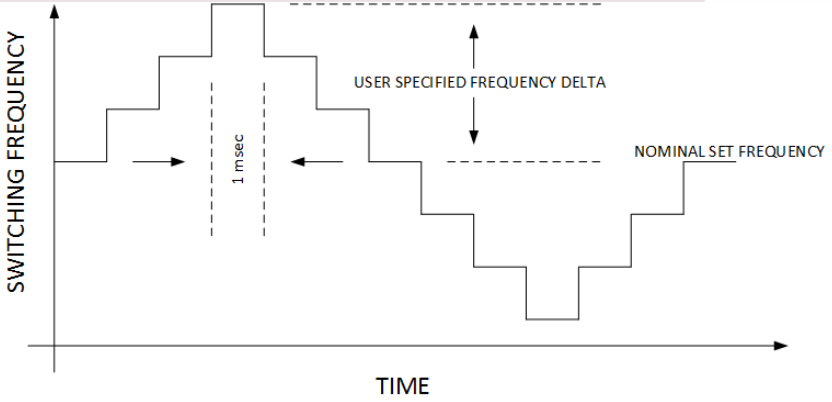
Agenda

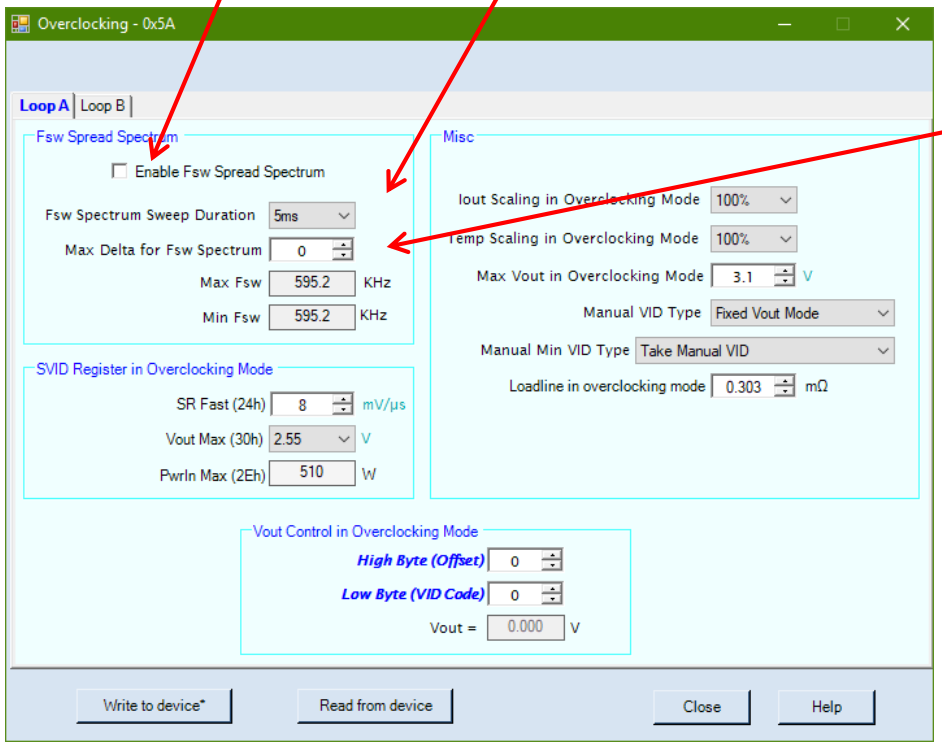
Overclocking...

Fsw Spread Spectrum
Frequency will step up and down between a Maximum **Max Fsw** and a Minimum frequency **Min Fsw.** Step size will depend on number of phases and the set duration

Enable Fsw Spread Spectrum
If marked the frequency will shift between a max and a min value with a selectable repetition frequency

Fsw Spectrum Sweep Duration
How long time for a full cycle of frequency change





Max Delta for Fsw Spectrum
If changing from one **Max Delta** value to another you must first set it to 0 and write to the controller to stop the present spectrum and then write the new value for the new spectrum to take effect.

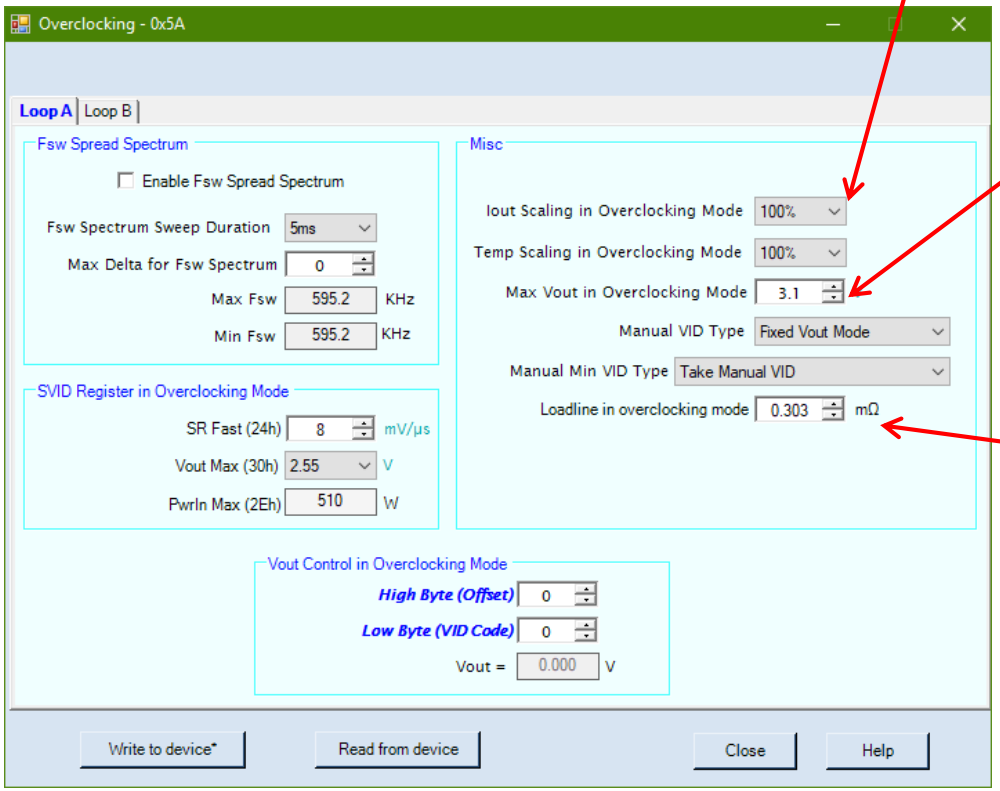
Overclocking…

Iout Scaling in Overclocking Mode and **Temp Scaling in Overclocking Mode**
will allow the user to select 25%, 50% or 100% reporting of IOUT(SVID/SVI2) and temperature(SVID) per loop.

These scaling settings will be valid when VOUT is set by the Manual VID or overclocking is enabled.

Only SVID/SVI2 telemetry will be scaled
I2C and PMBUS reporting will not be scaled, they will report 100% of the actual IOUT and temperature.

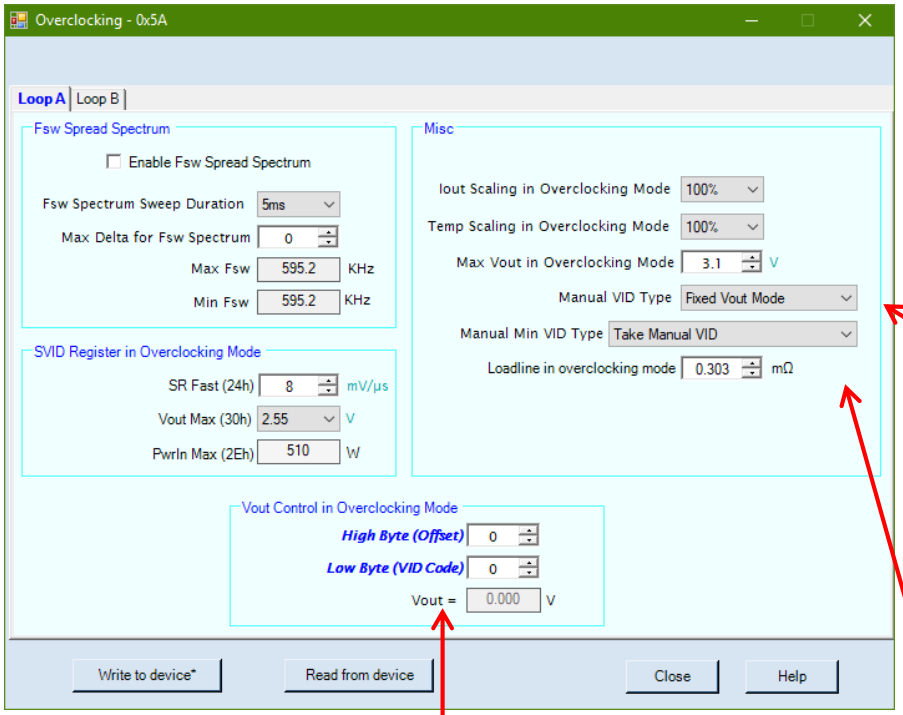
Over temperature shutdown will be based on the unscaled (100%) temperature value
OCP will be based on the unscaled (100%) IOUT value



Max Vout in Overclocking Mode:
Allow a maximum Vout to be set. Any command to set a higher Vout will be ignored and actual Vout will stop at the selected voltage even if commanded to go higher.
Valid for Intel mode and Pmbus. Not active for AMDmode.

Icc Max
and
Loadline:
As default this gets copied from regular loadline setting. Can be changed here if other values are wanted for overclocking mode.

Overclocking…



Manual VID type:
Fixed Vout Mode
Fixed offset mode
In 'Fixed VOUT' Mode, VOUT is set by the VID code specified by the operating mode.
In 'Fixed VOUT' Mode, the SVID ALERT# will assert immediately upon receipt of an SVID command to change VOUT.

Because VOUT will not change, T_alert assertion will **not** be delayed by VID_DELTA/SLEW_RATE
In AMD SVI2, VOTF Complete will not assert in Fixed VOUT mode

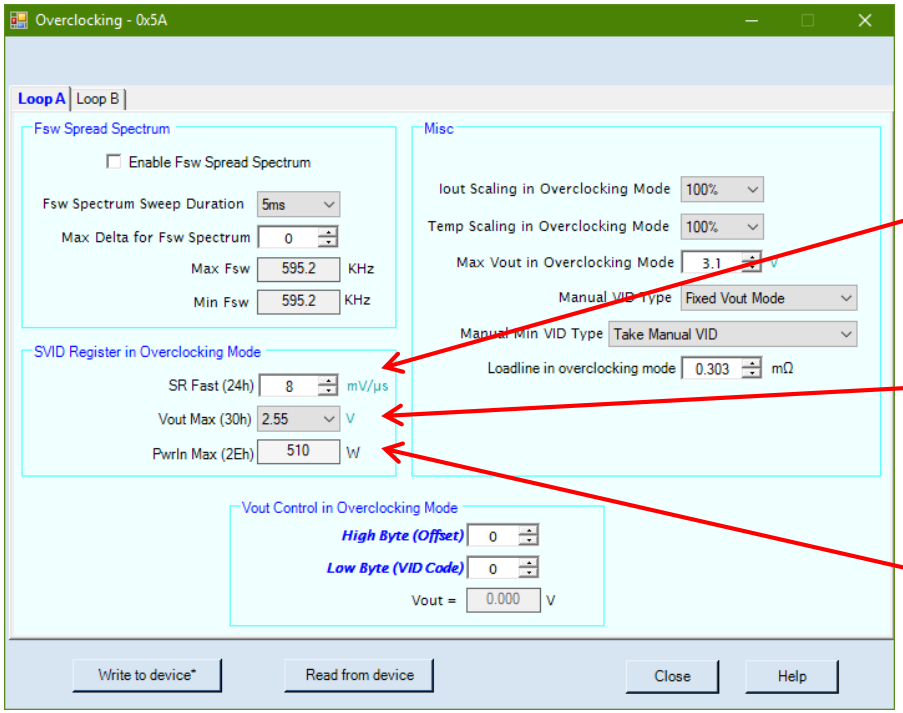
In 'Fixed VOUT' Mode, changes to the Manual VID register will cause VOUT to change but will not cause SVID ALERT# to assert.
Writing the Manual VID register to 0 will cause VOUT to return to the SVID/SVI2 commanded voltage

Manual Min VID type
Select between "Take Manual VID" or
"Take MAX of SVID or Manual VID"
The last setting will limit the voltage to the lowest of the 2 settings.

Vout control in overclocking mode
Allow MANUAL VID settings
Offset : can be + or – offset values >80 count as negative. 2 complement hex
VID code: Vout follows the AMD VID table except for 0 that will cause VOUT to return to the SVID/SVI2 commanded voltage

This function also work in non overclocking mode to manually enter VID code to set Vout.

Overclocking…



SR fast
Allow another setting for slew rate while in overclocking mode

Vout Max
Allow another setting for maximum Vout while in overclocking mode

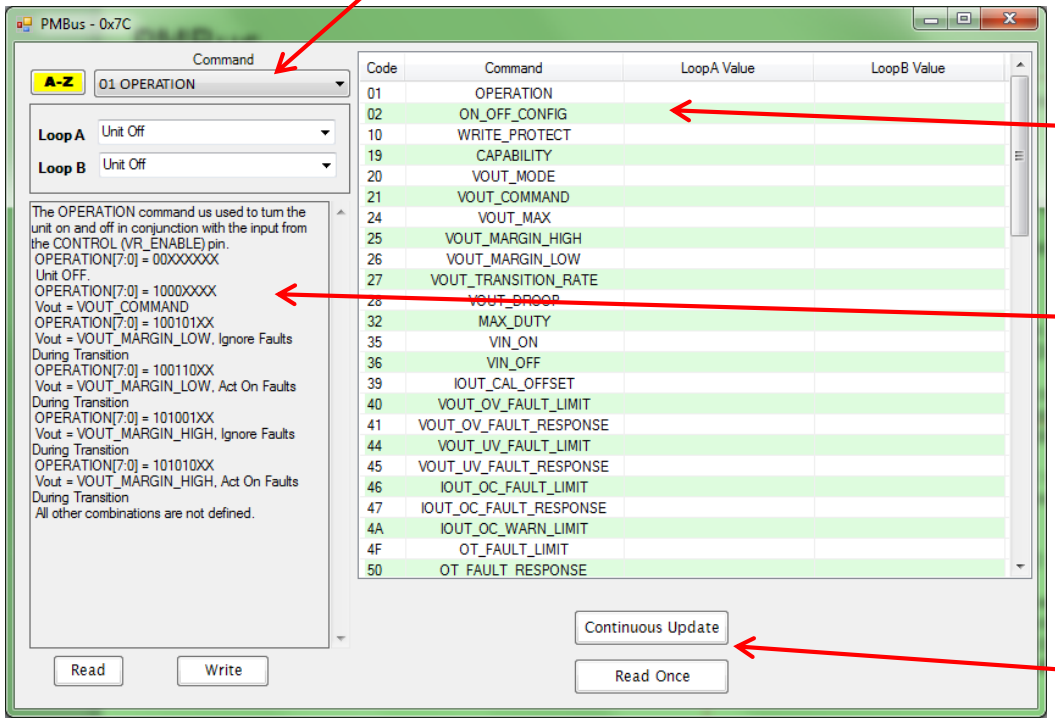
PwrIn max
Allow another setting for maximum input power while in overclocking mode

Agenda

PMBus Commands

Each PMBus command can be selected and the values read or written to.

Depending on command it may be read or write only. In such case the different buttons get grayed out.



List of each PMBus command and if a controller is connected it will read out the settings and list them in easy to read formats.

Volt, Ampere etc…

The selected PMBus command is explained with more details

Continuous Update – reads the PMBus continuously.

Read Once – Read PMBus once every time button is clicked

Agenda

nVidia

Purpose

Describe the settings needed to run in nVidia mode

Target audience:

Design engineers that have some experience with digital power and nVidia needs as the explanations focus on settings in XDPE12xxx and XDPE 14xxx family of controllers.

nVIDIA PWM VID Overview

A pulse width modulated I/O that controls the Voltage Regulator VID set point (output voltage) by modulating the duty cycle of the signal sent

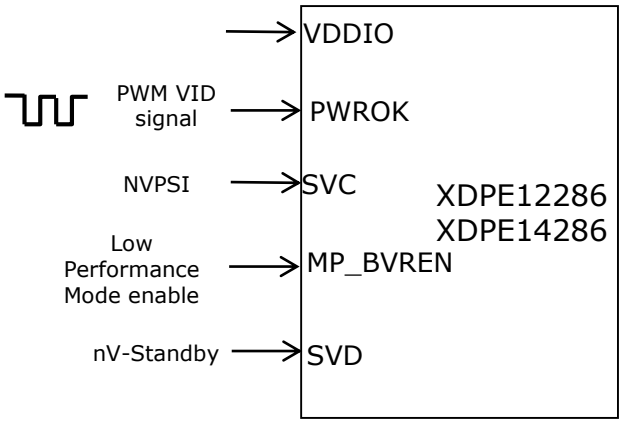
- PWM VID functionality applies to Loop 0 only
- An optional method of control is to digitize an analog voltage (VAUX) and generate an output voltage proportional to this input.

PWM VID implementation allows for

- Wider range of VID set points using a single I/O pin
- VID target change can be communicated in a single cycle
- PSI entry/exit is instantly communicated

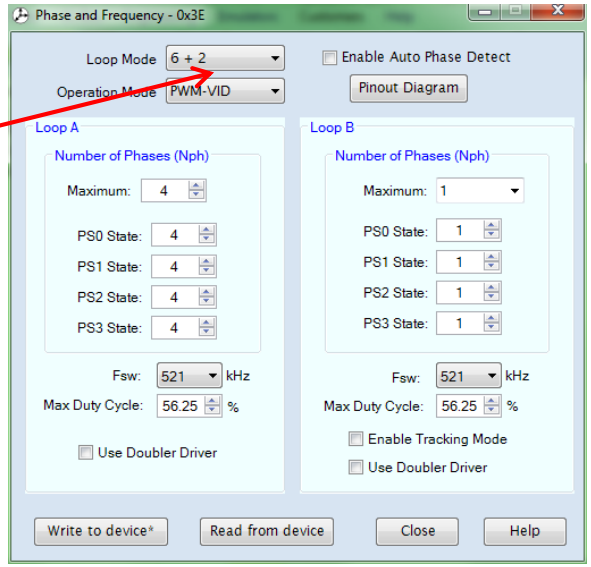
nVidia PWM VID connections

In nVidia PWM mode some pins get a new function in parts that do support the PWM-VID function

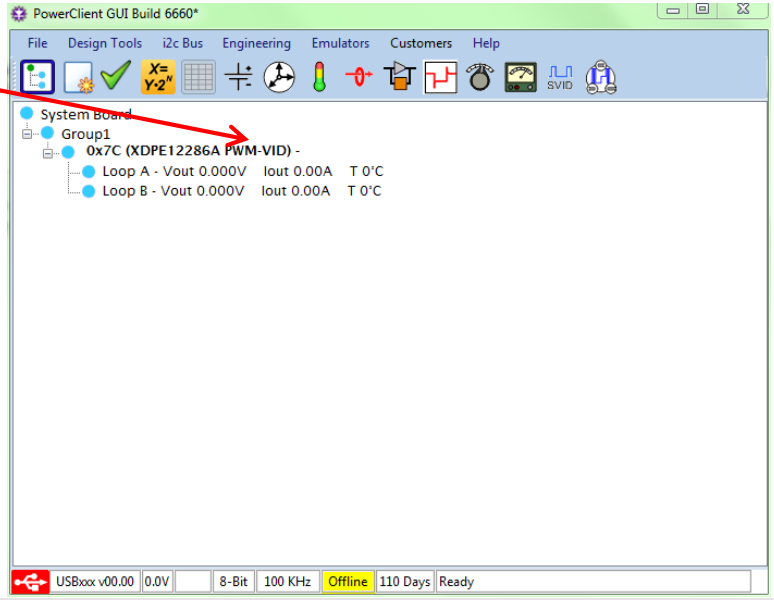


Select nVidia mode

Select the PWM-VID to enter nVidia mode

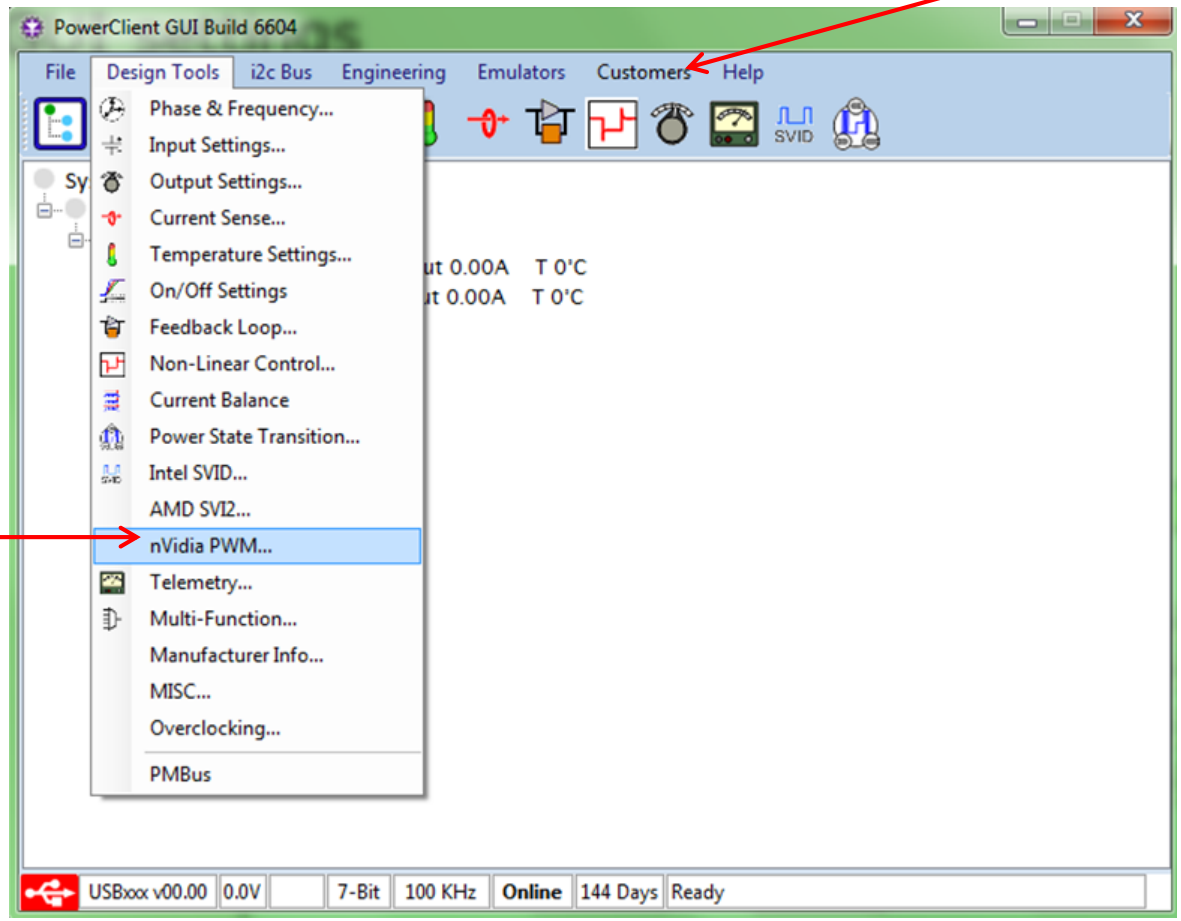


The selected mode is visible after the component name



Find nVidia settings in GUI

You may need a password to activate the nVidia settings. Enter it in the Customers tab
Ask your Infineon FAE if you do not have a password.

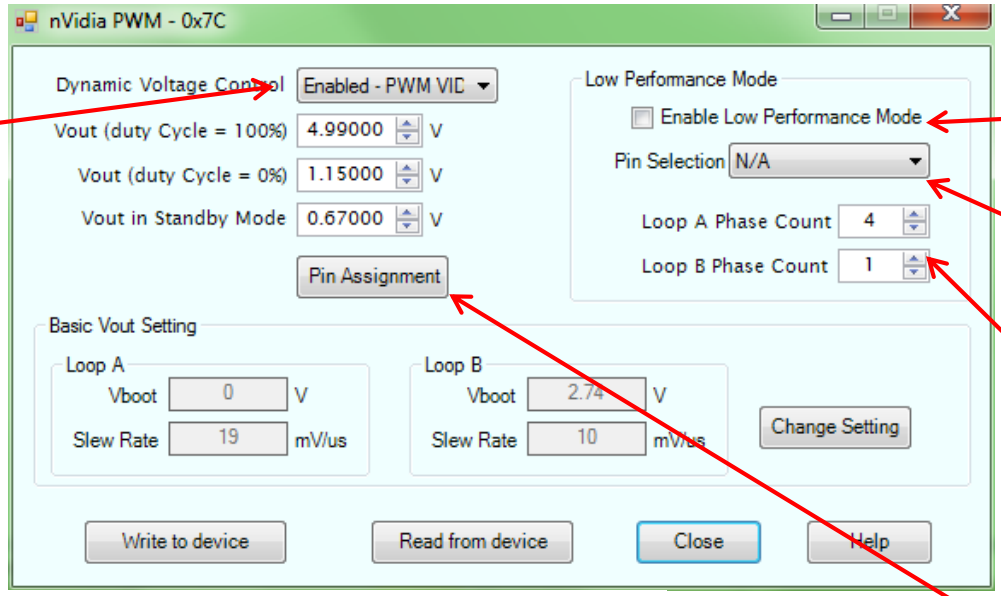


GUI settings

I2C (Disabled) or PWM VID control of Vout (=Enabled)

Start up with Vboot or the value set by the PWM signal.

If PWM signal comes later then starting with Vboot and as soon PWM signal is applied the voltage will change to the voltage set by the PWM



Tick box to enable nVidia Low Performance Mode

Select which pin will act as the enable for Low Performance Mode

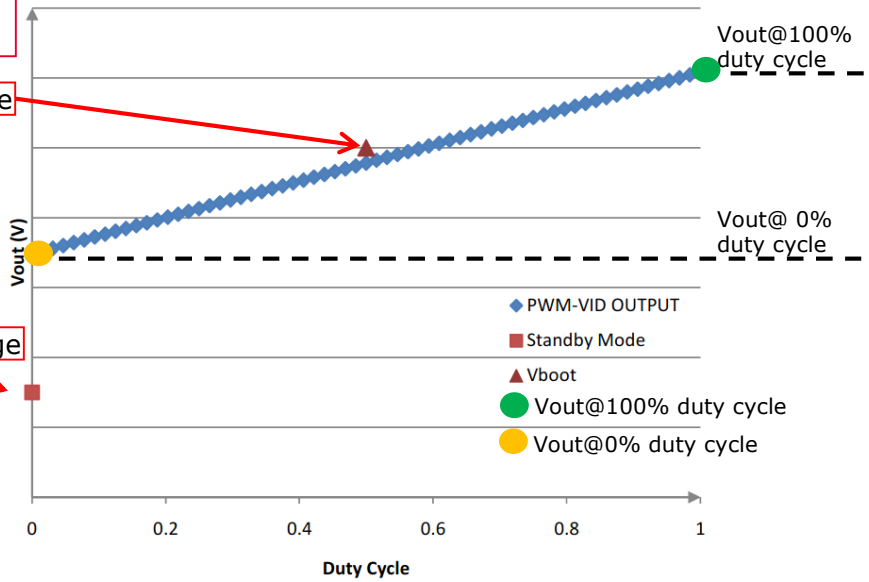
Select number of phases when in Low Performance Mode

Pin Assignments

Will show what pins to connect the signals too.

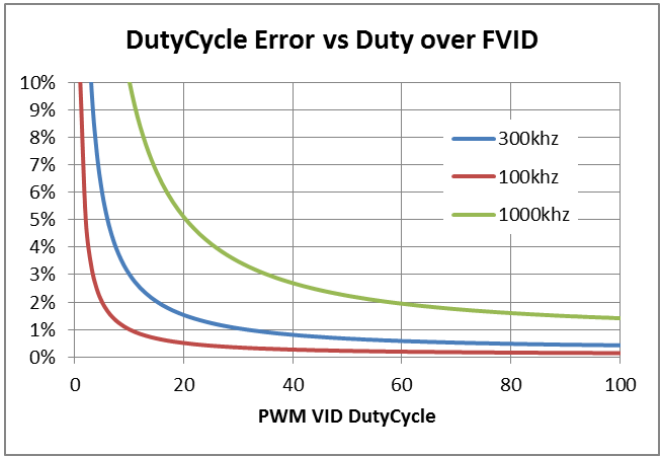
Vboot voltage

Standby voltage



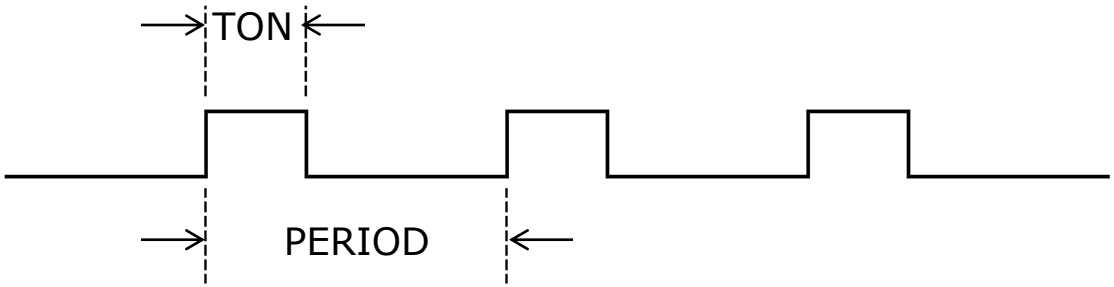
Sierra Digital Solution

- Digital NVPWM connect directly to the SVD pin
- Signal digitized by 100MHz clock (10ns resolution)
  - Typical FVID 300kHz
  - Usable FVID range 100kHz ←→3MHz
- Digital offset can be added via I2C



Digital PWMVID Measurement

- The dutycycle is calculated as the quotient of the ON time of the NVPWM over the PERIOD of the signal.
  - ON time is measured from the rising edge to the falling edge of the NVPWM
  - PERIOD is measured from a rising edge to the next rising edge



- The calculation is updated on every rising edge of NVPWM
- A continuous moving average of 4 dutycycles calculations is used to set the target voltage

Digital Solution Equations

- Duty = Ton/Period
- Vout = vout_vid_vmin + duty · pwm_vid_slope
  - pwm_vid_slope = (Vmax-Vmin)/(5mV(VIDtable)) per 100% duty cycle change

Other notes

- The SVC pin is used for the NVPSI function. Pulling the pin low would set the VR to a low power state

nVidia PWM... Slewrates

- Digital solution
  - the slewrate can be set in the Output Settings window. The fast slew rate setting is used.

Revision History

- 2.0: Added XDPE142xx information

Part of your life. Part of tomorrow.