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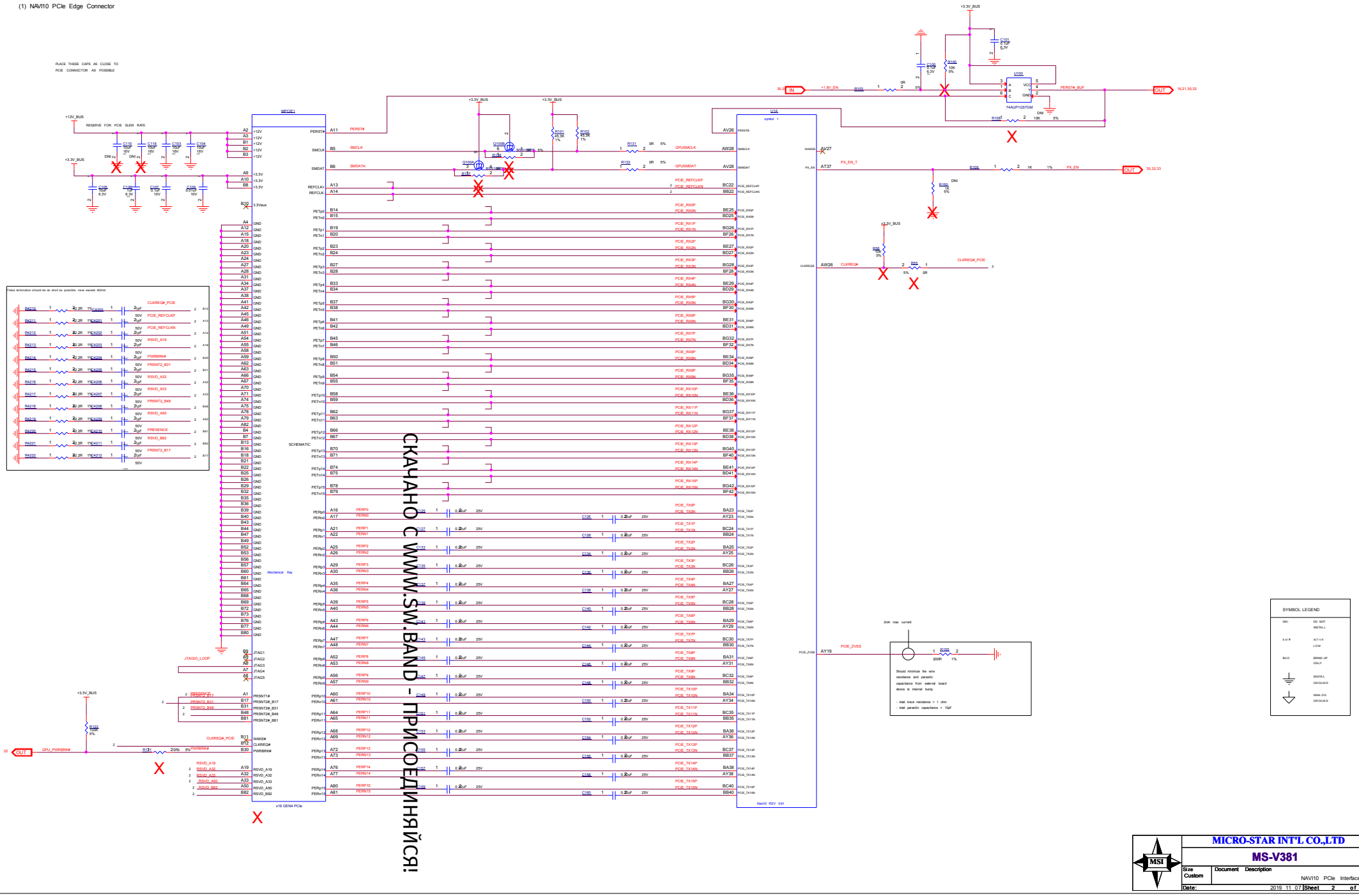
(1) NAVI10 PCIe Edge Connector



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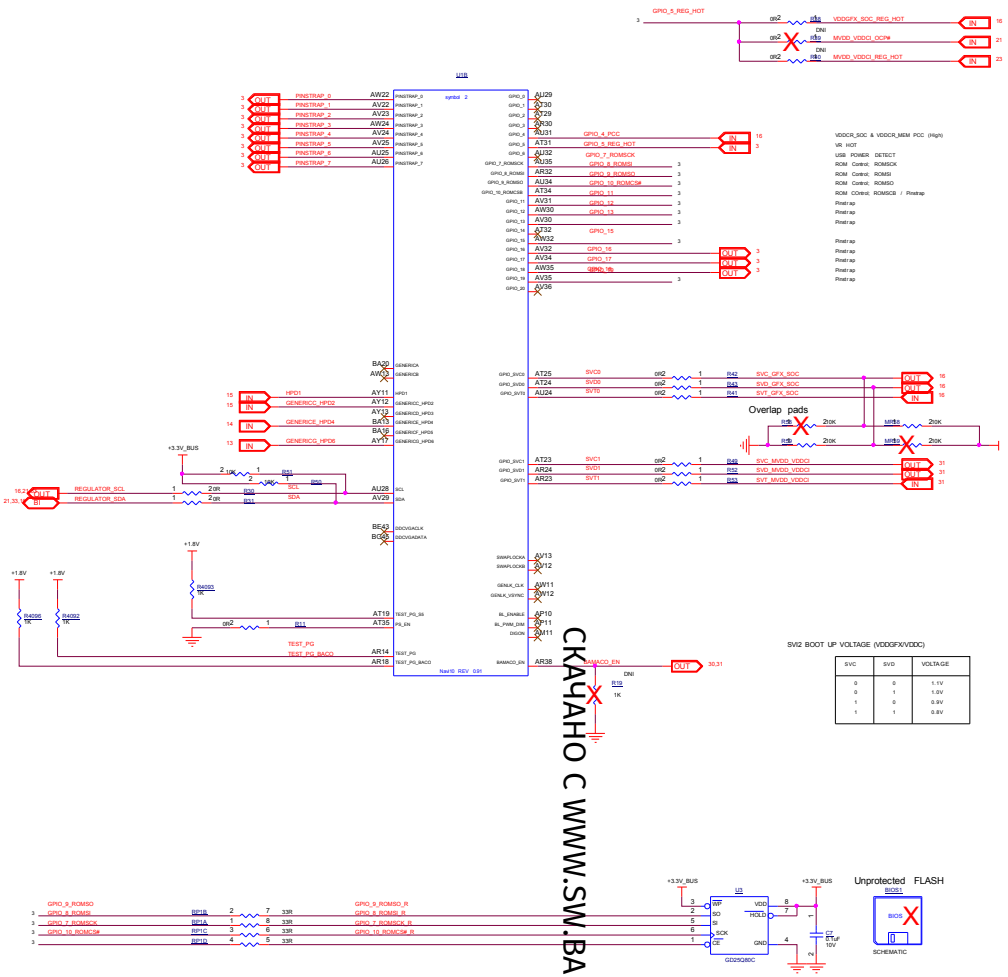

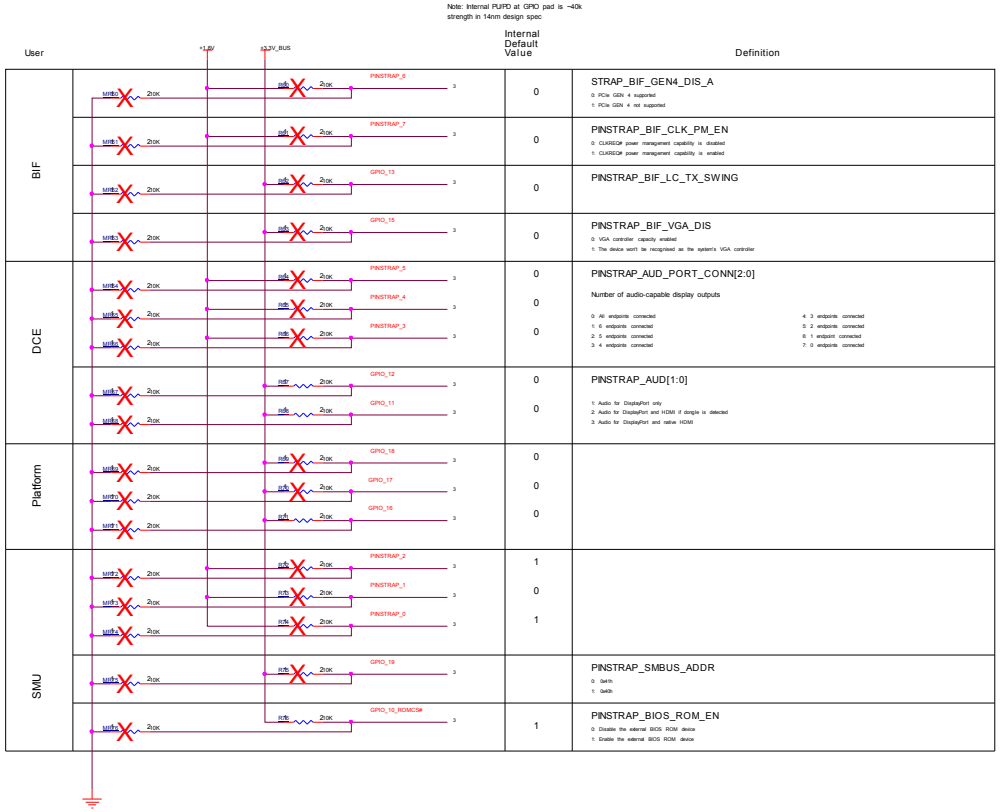

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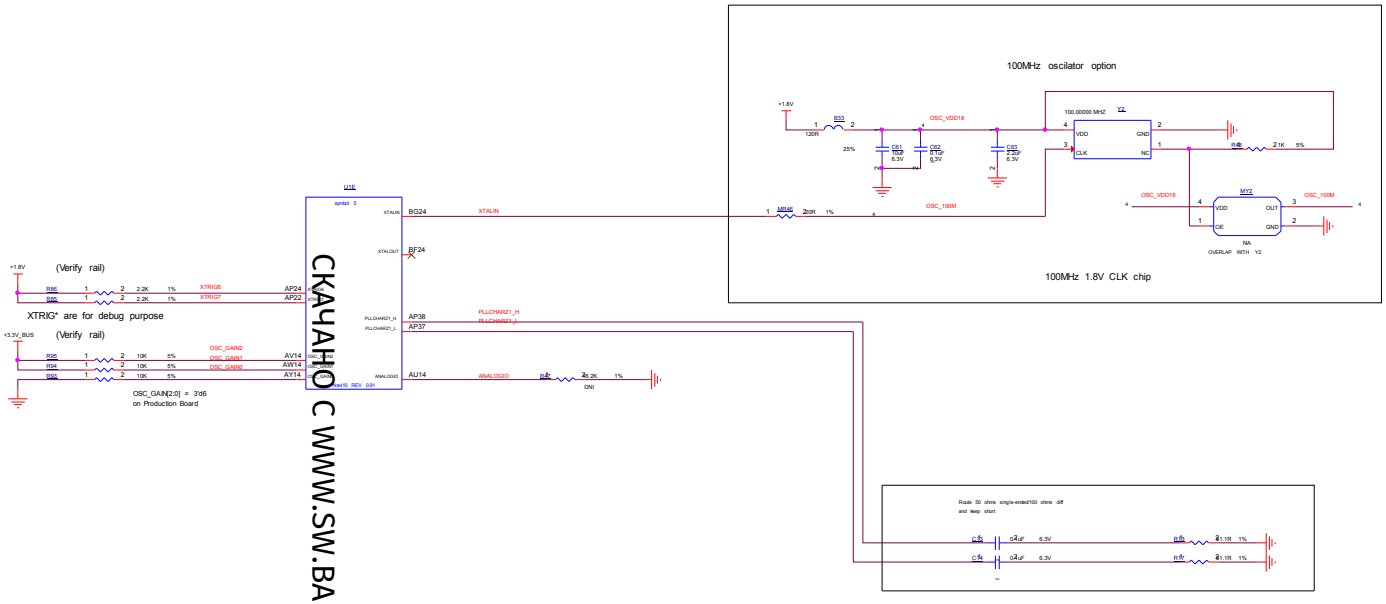

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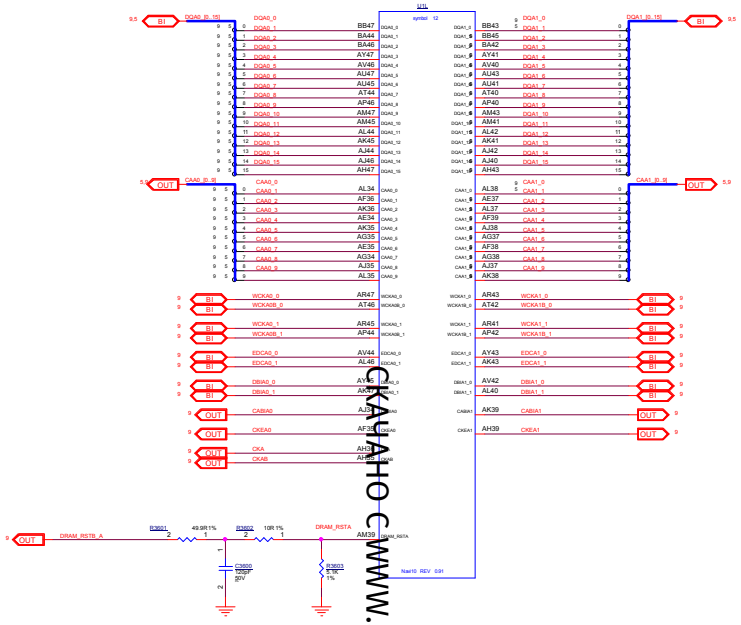
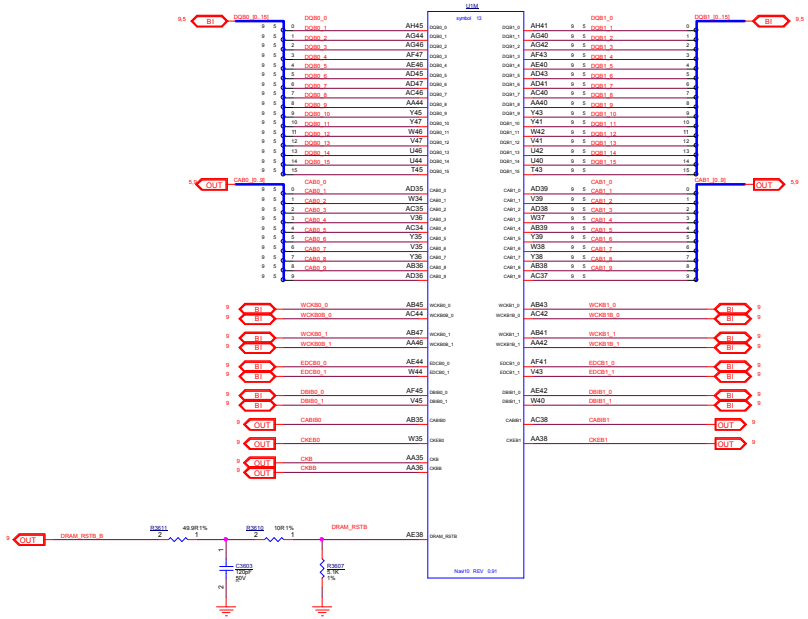
NAVI 10 MEM INTERFACE CH A/B





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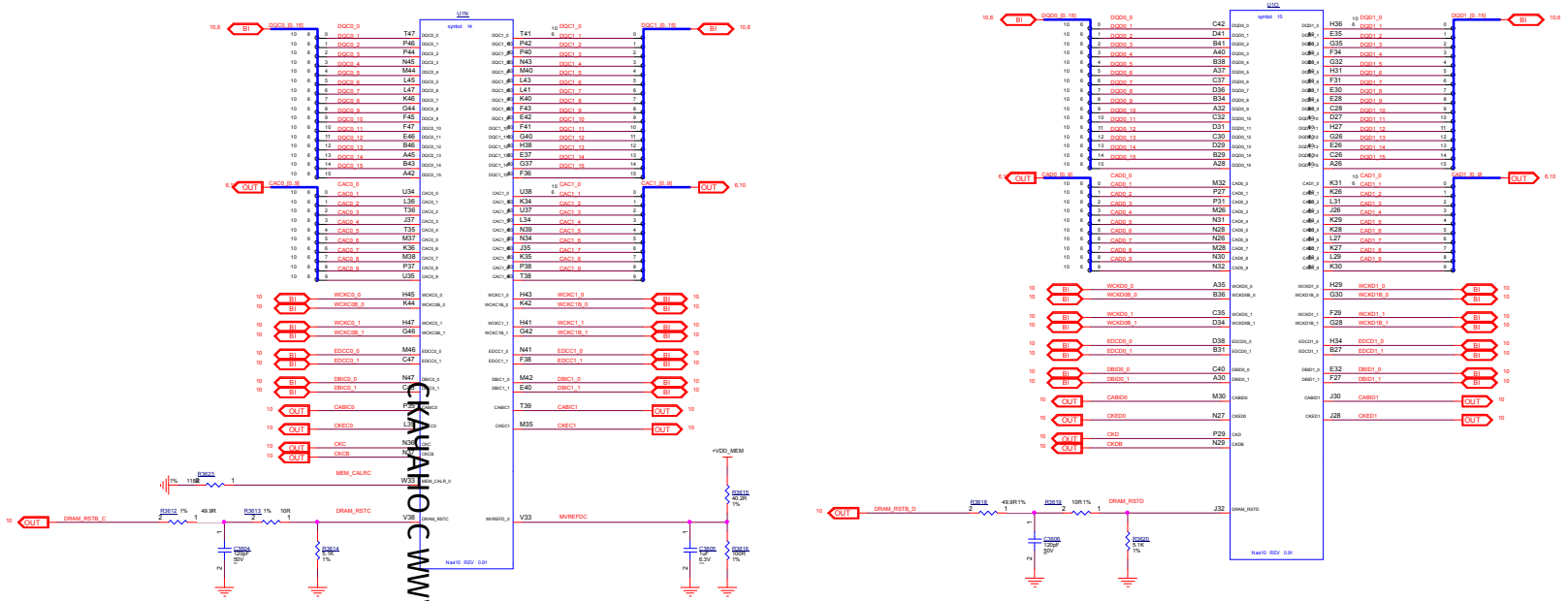

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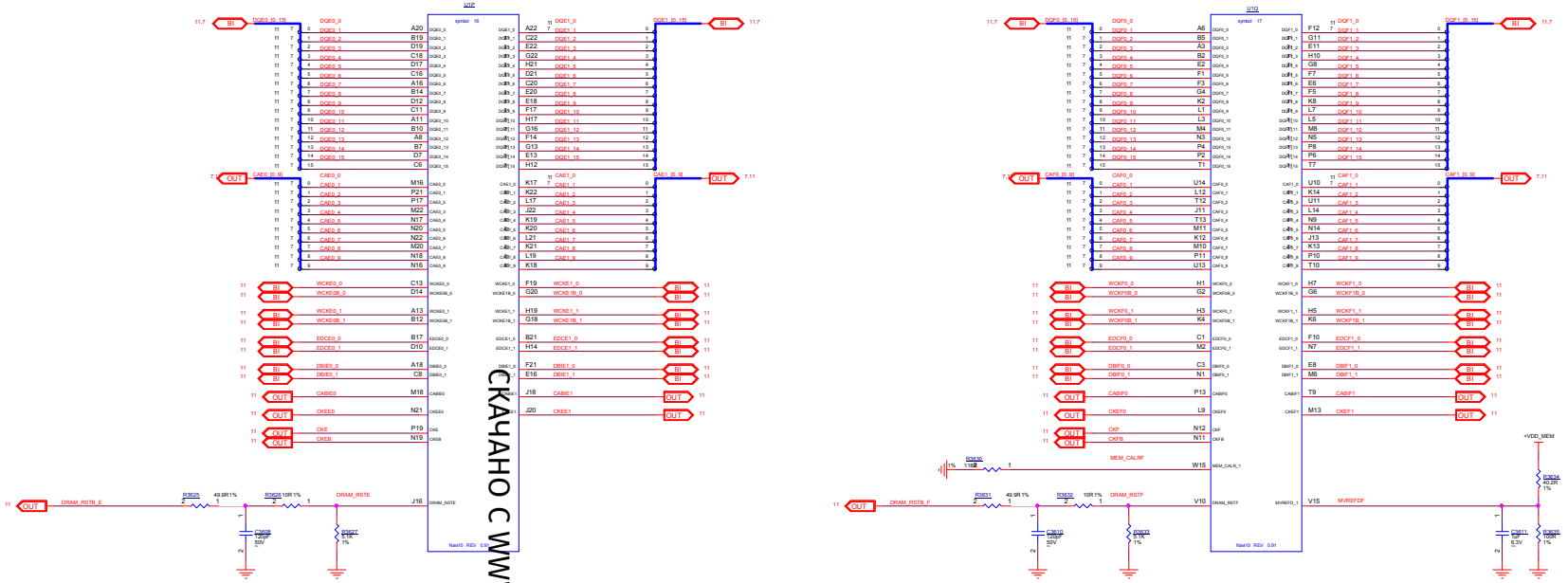

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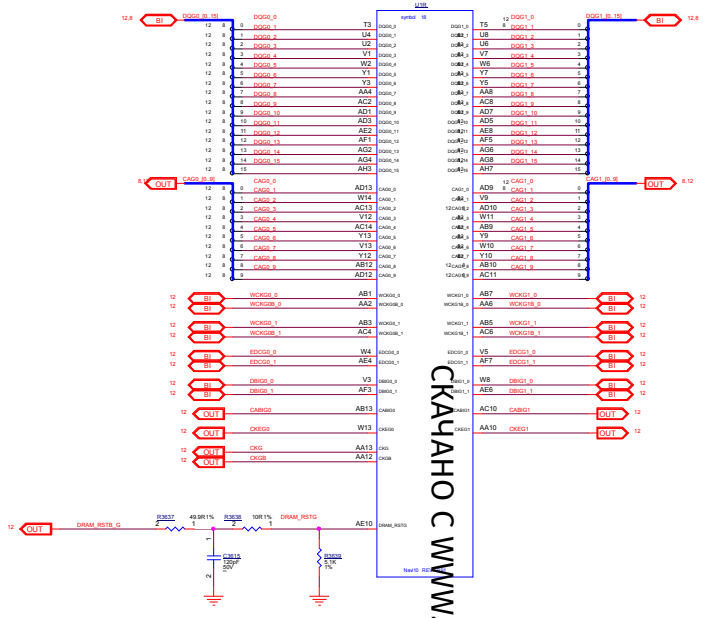

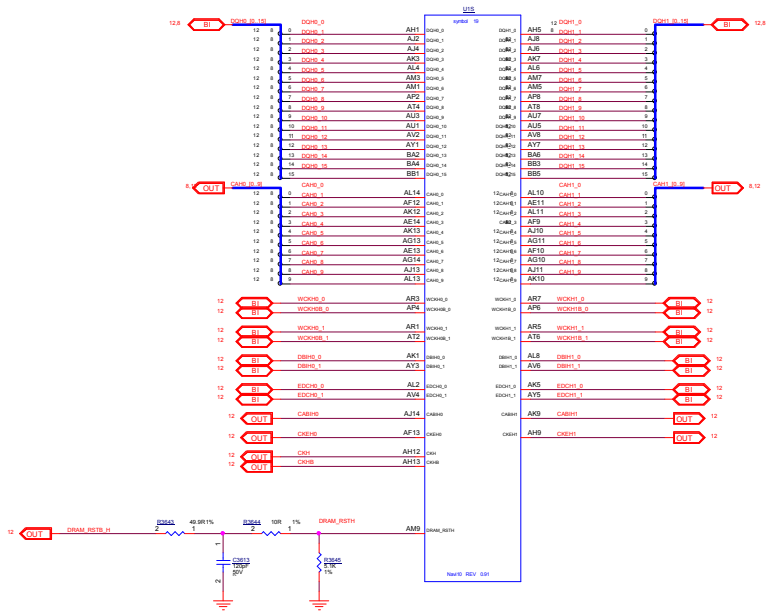

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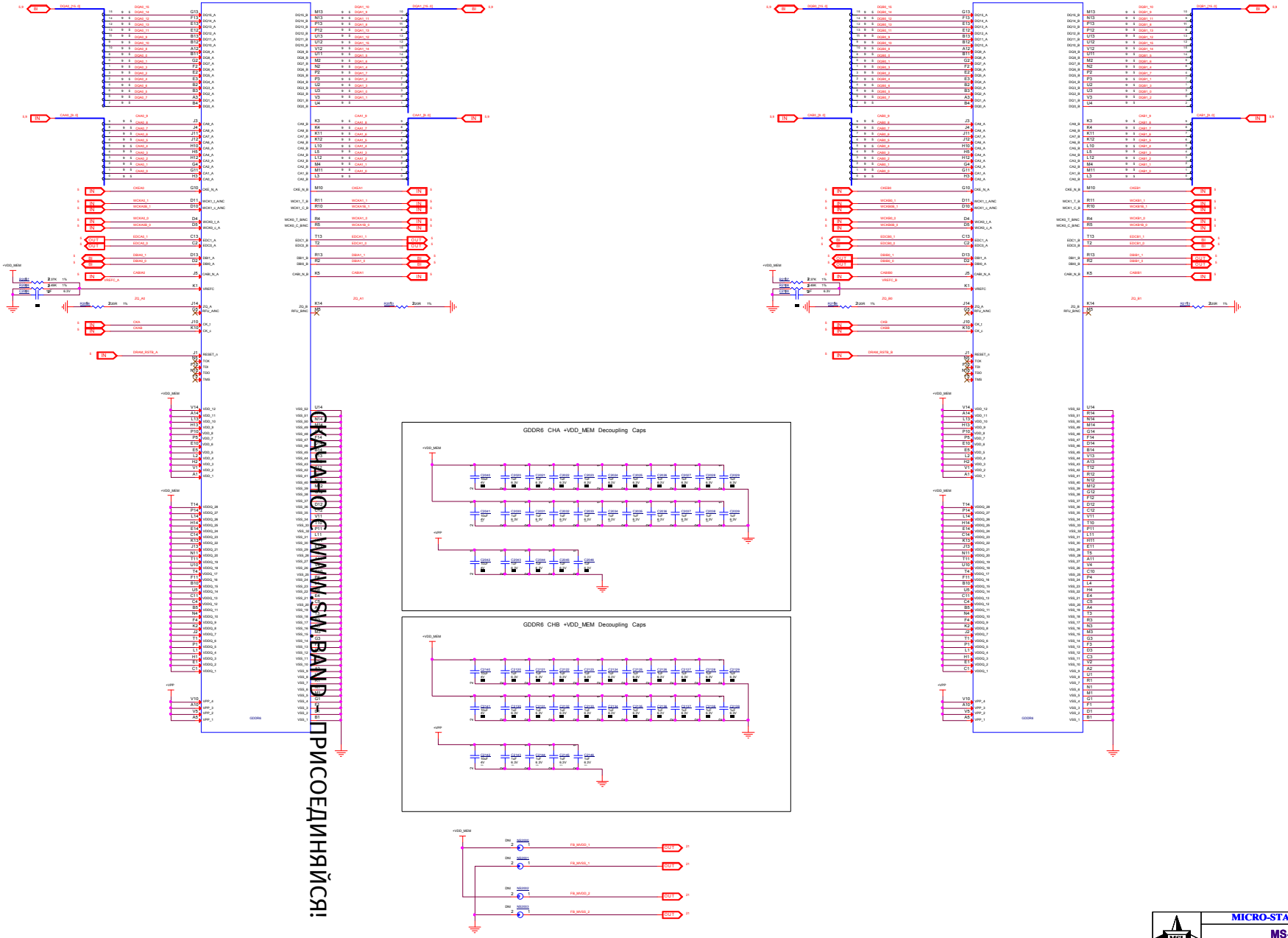

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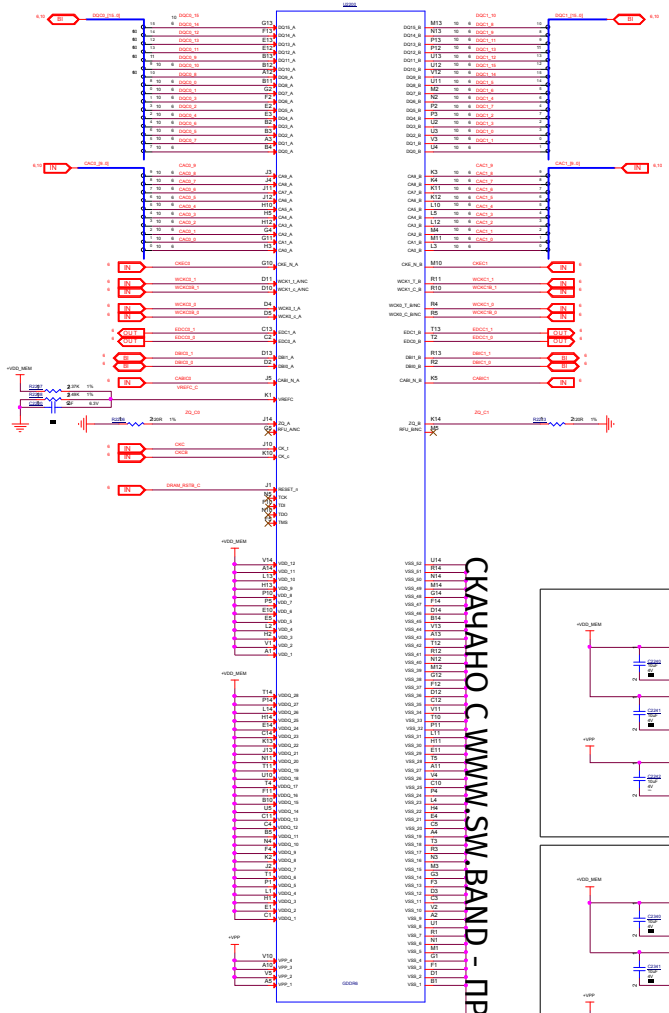

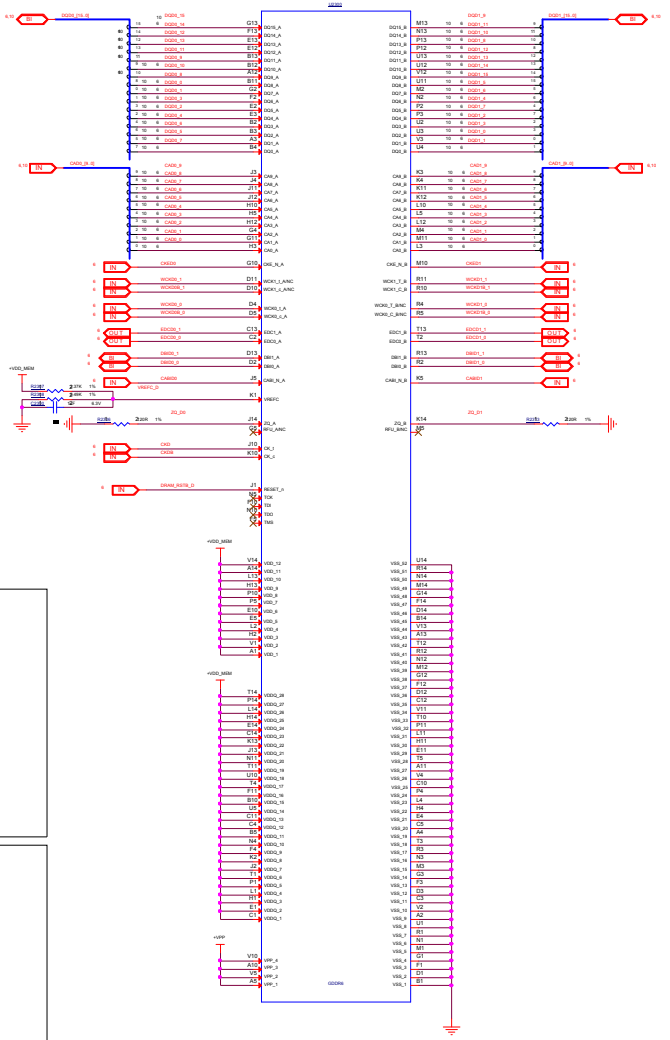

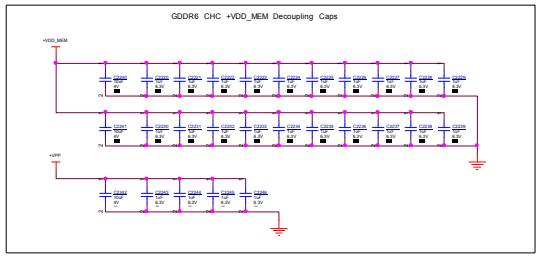

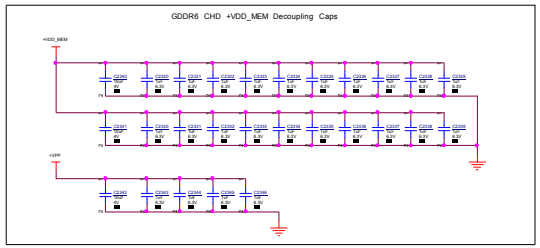

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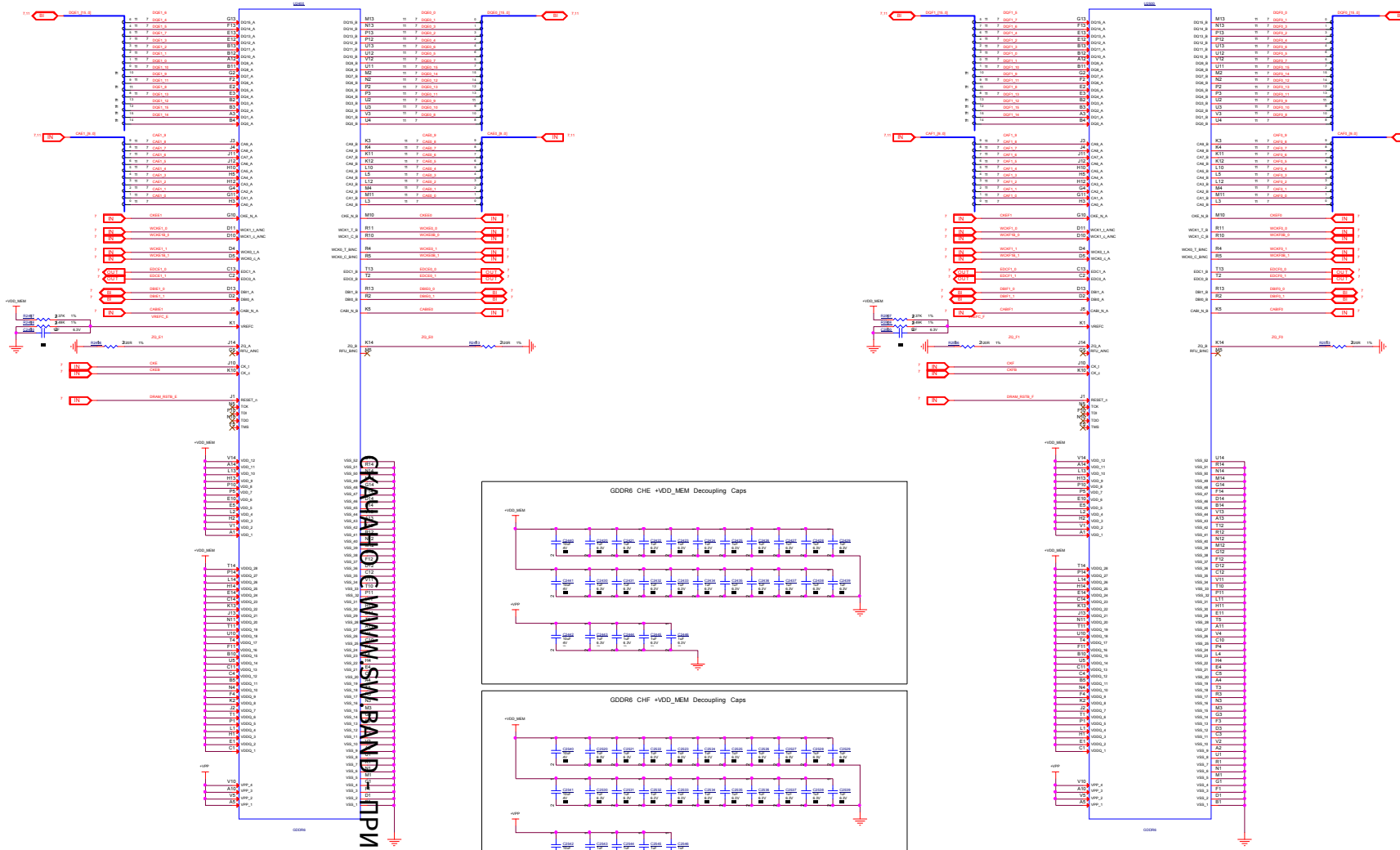

GDDR6 CHE +VDD_MEM Decoupling Caps

GDDR6 CHF +VDD_MEM Decoupling Caps

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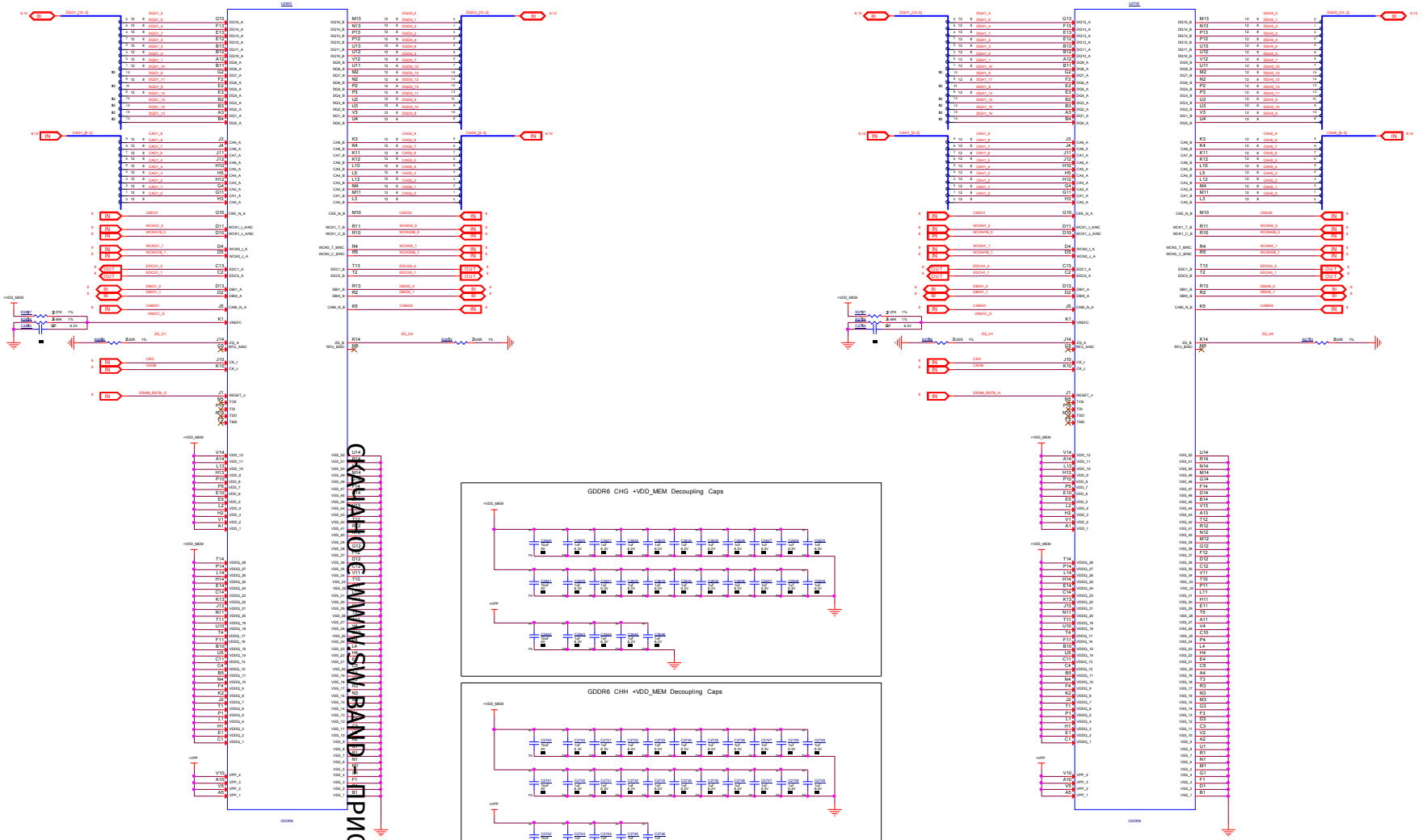

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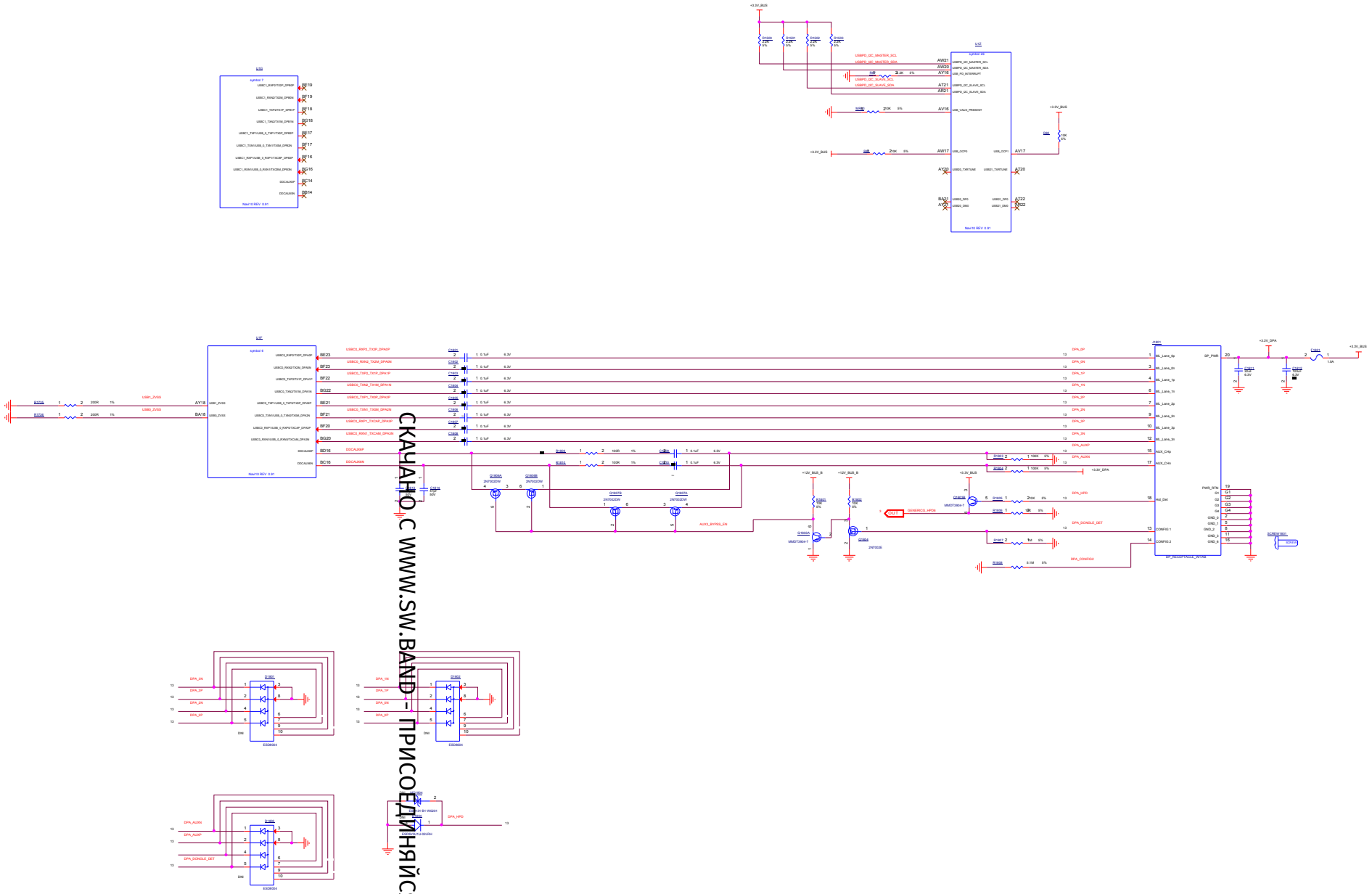

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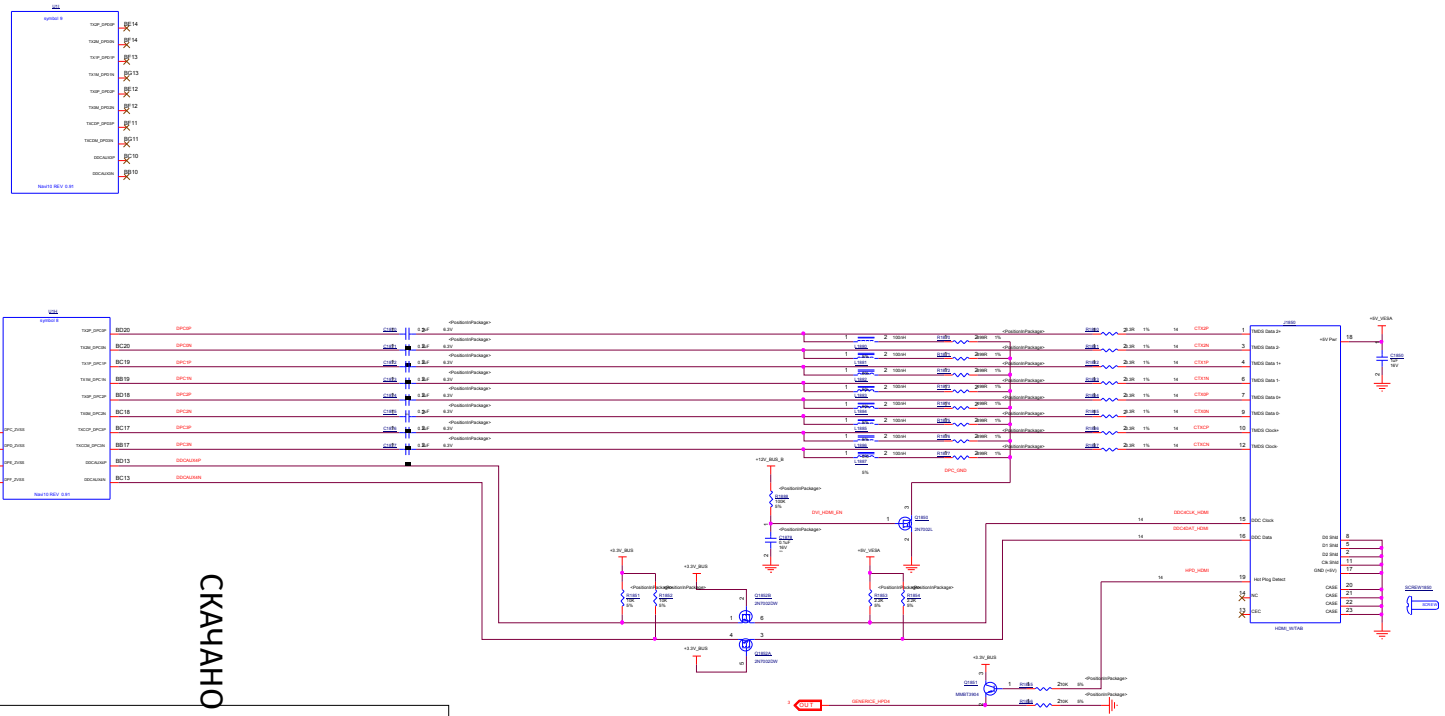

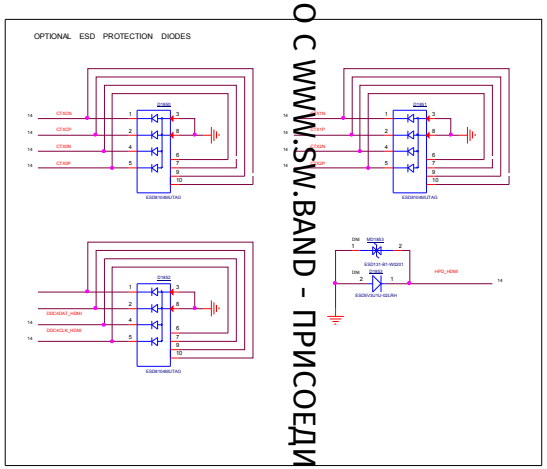

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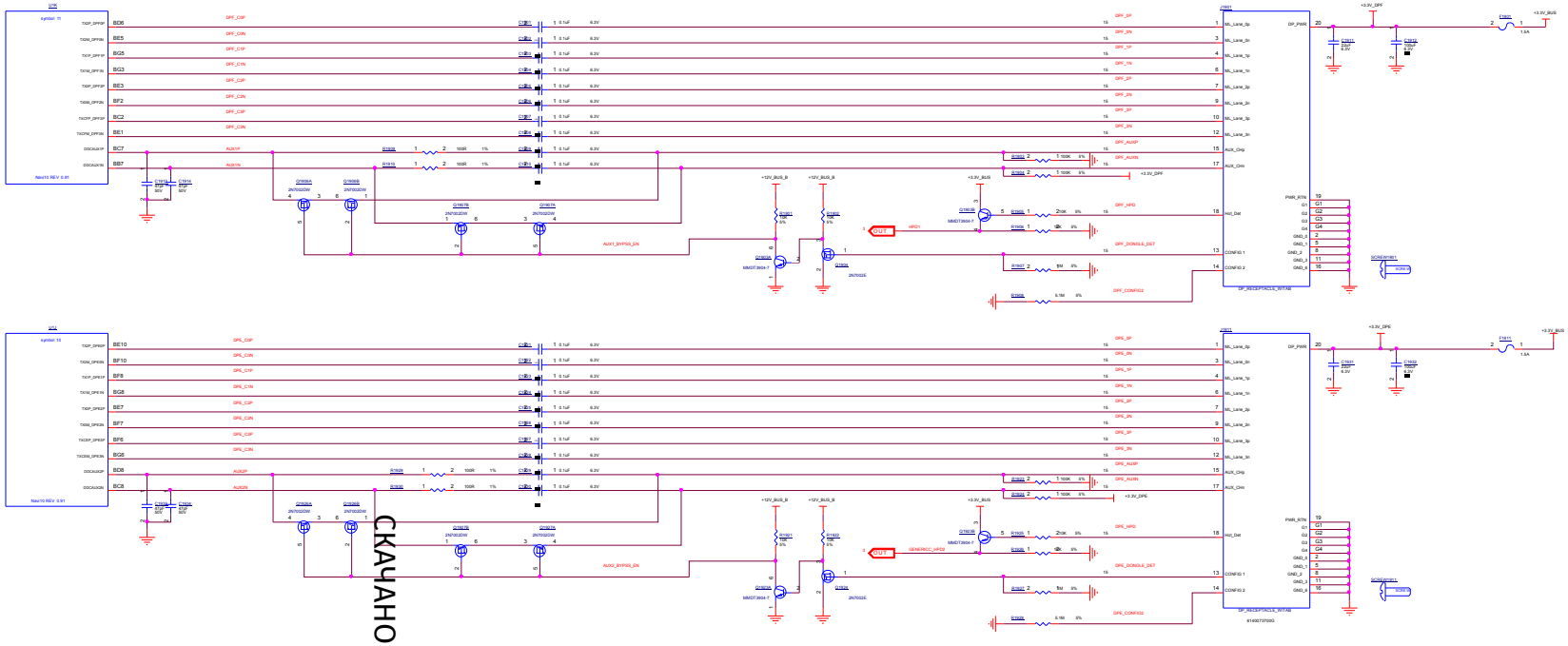
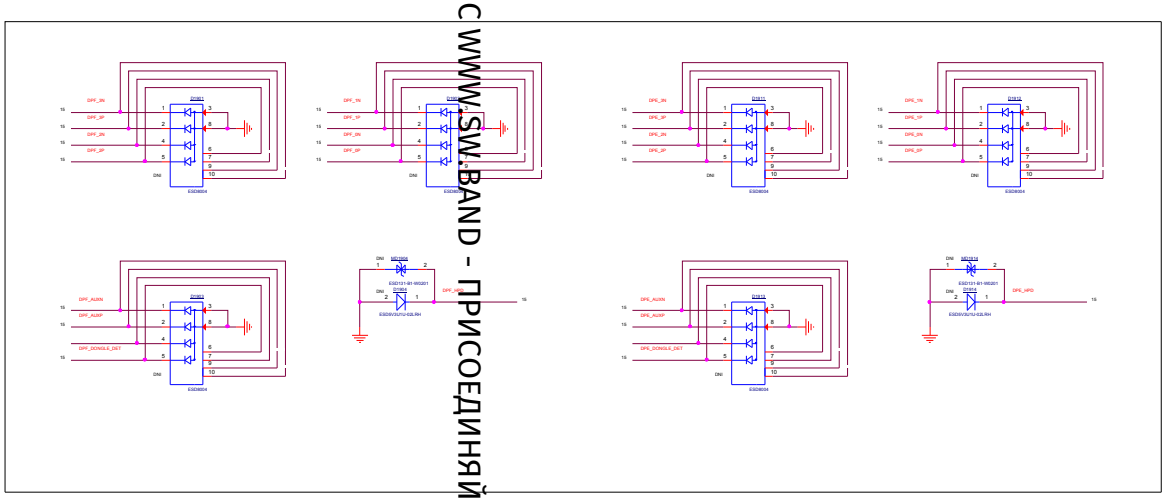
(9) NAVI10 TMDP E/F





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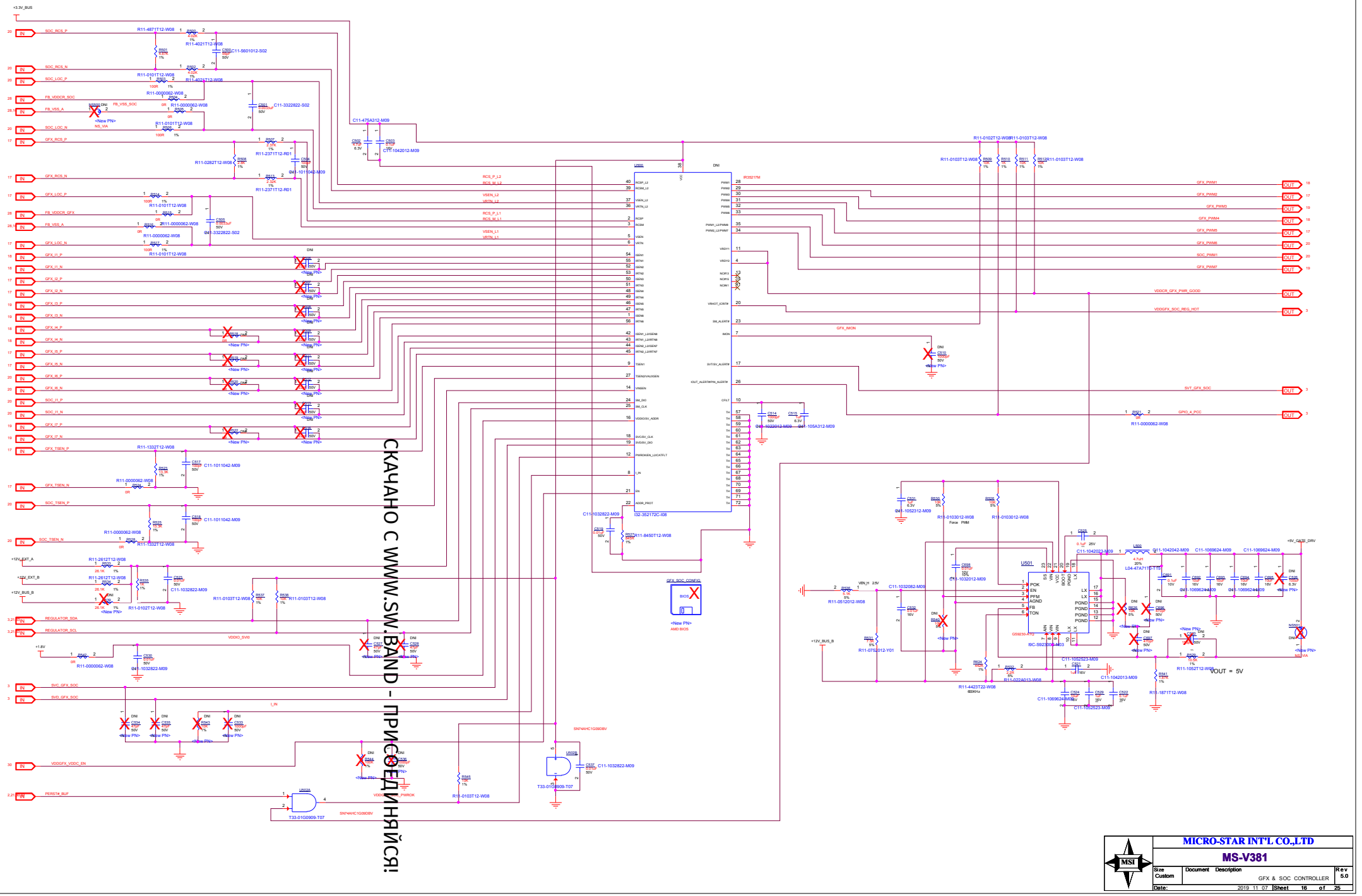
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SOC_RCS_N
SOC_LOC_P
SOC_LOC_N
GFX_RCS_P
GFX_RCS_N
GFX_LOC_P
GFX_LOC_N
GFX_TSEN_P
GFX_TSEN_N
SOC_TSEN_P
SOC_TSEN_N
REGULATOR_SDA
REGULATOR_SCL
SVC_GFX_SOC
SVD_GFX_SOC
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PERST#_BUF
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GFX_PWM5
GFX_PWM6
SOC_PWM1
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VDDGFX_SOC_REG_HOT
SVT_GFX_SOC
GFX_IMON
+5V_GATE_DRV
+12V_BUS_B
+12V_EXT_A
+12V_EXT_B
+1.8V
VDDIO_SVI0
PWROK
AMD BIOS
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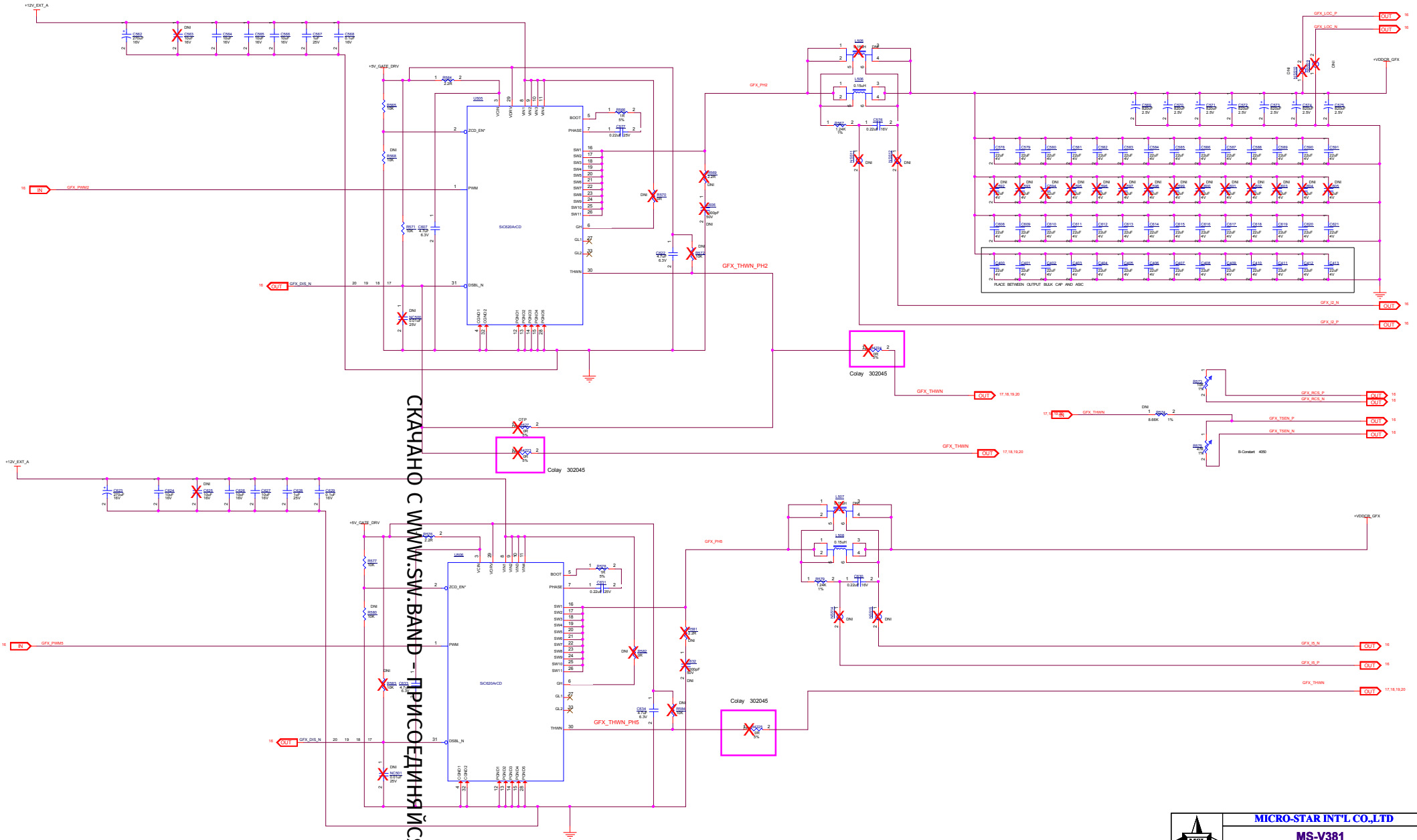
СКАЧАНО С WWW.SW.BAND - ПРИСОЕДИНЯЙСЯ!



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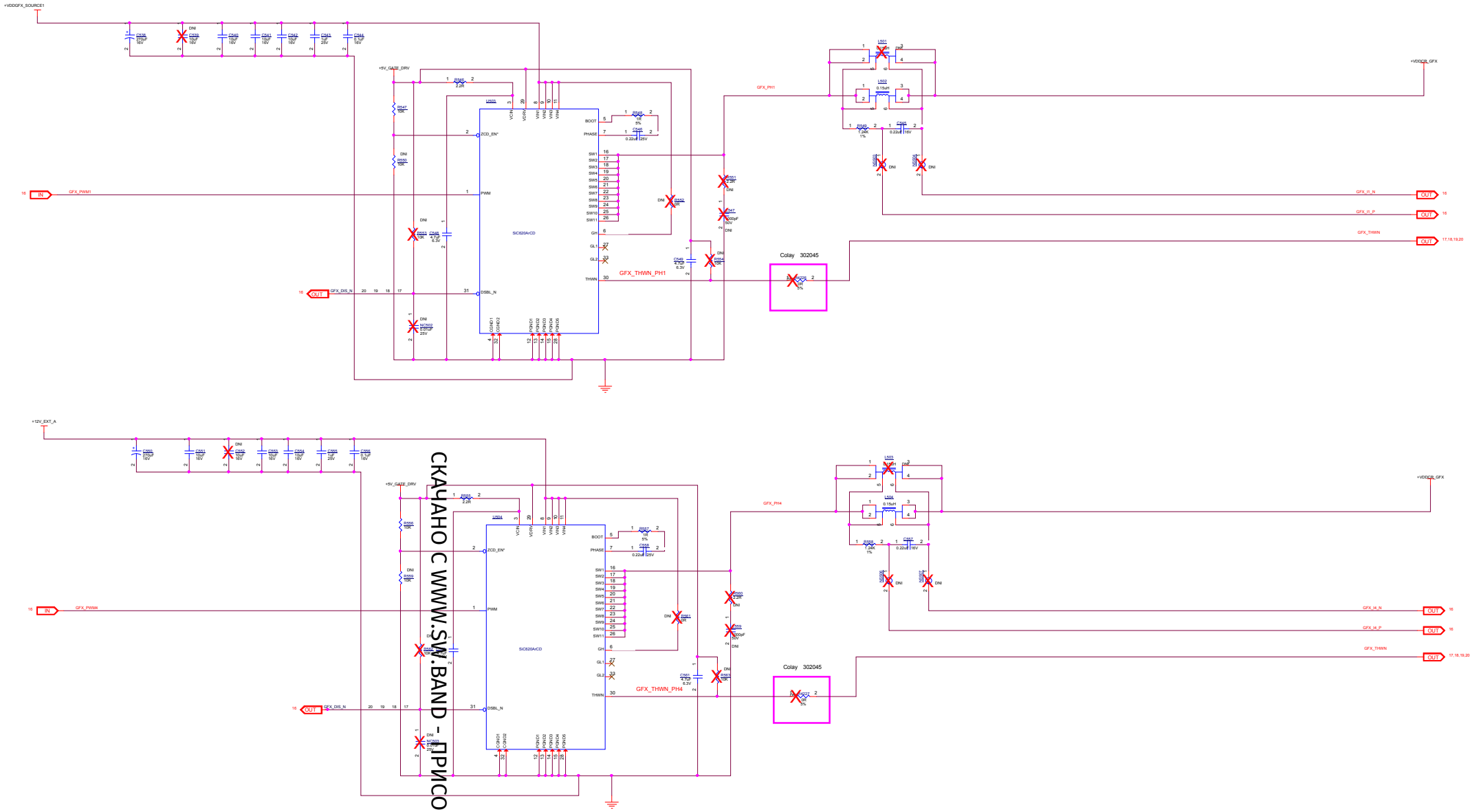

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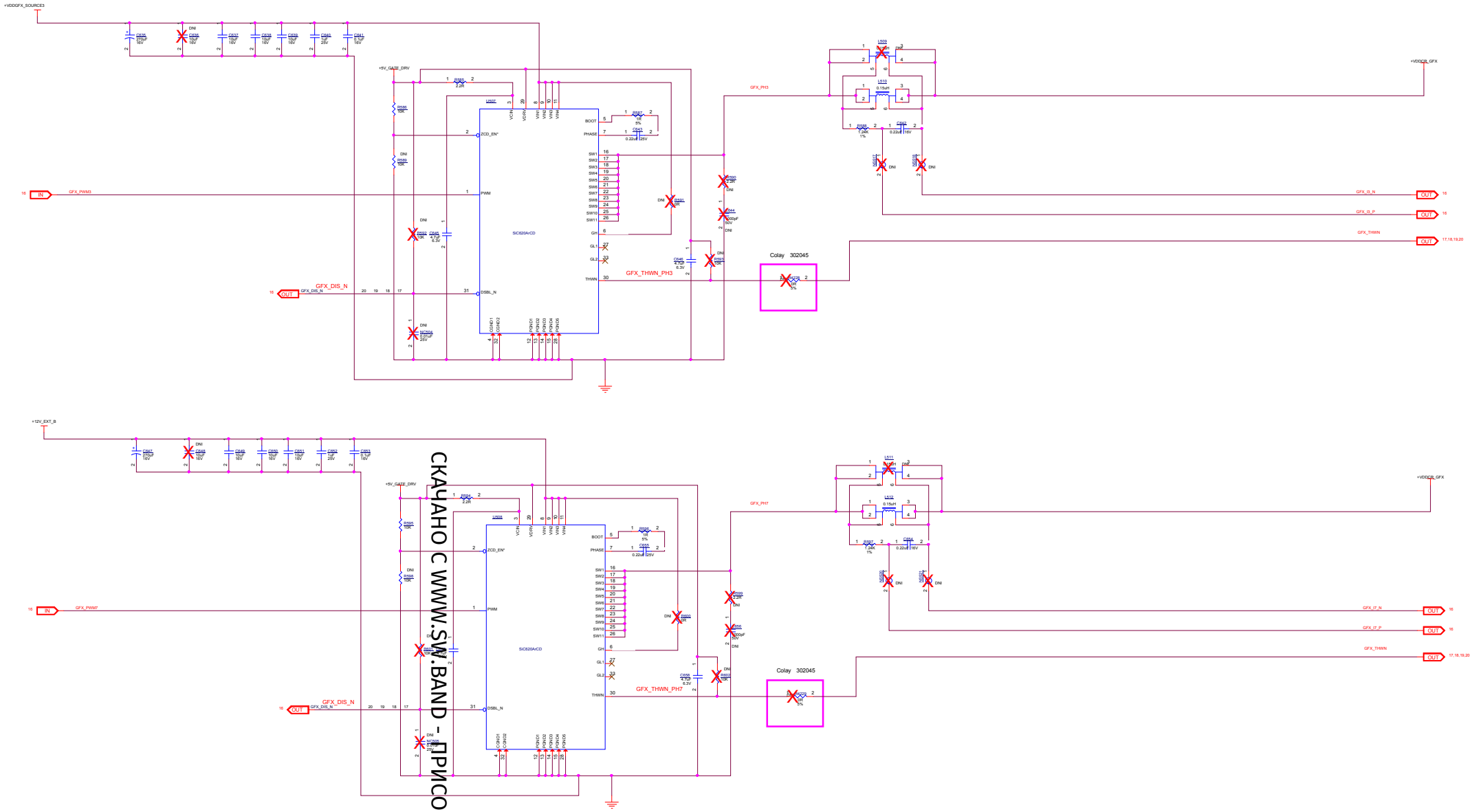

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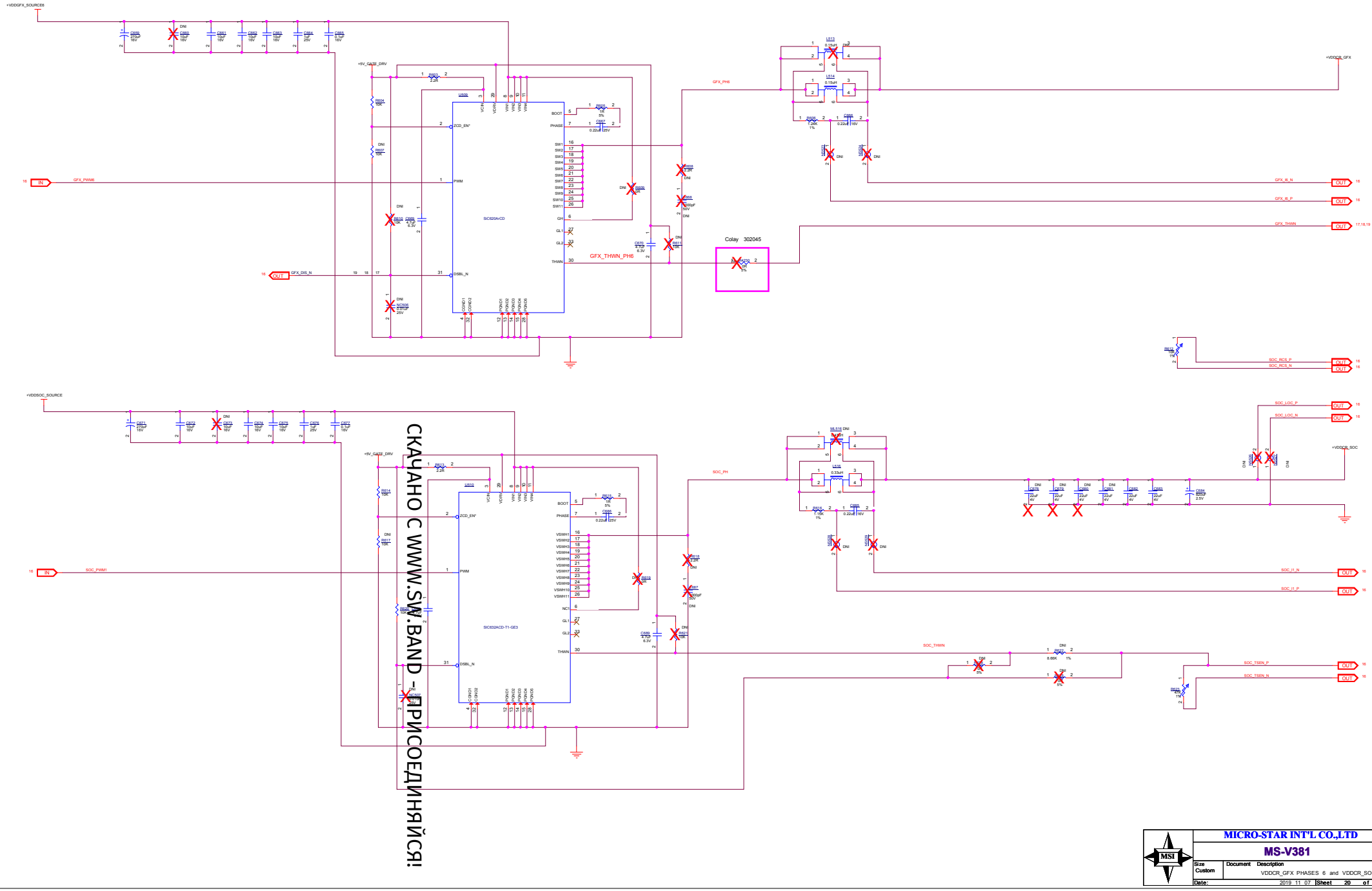

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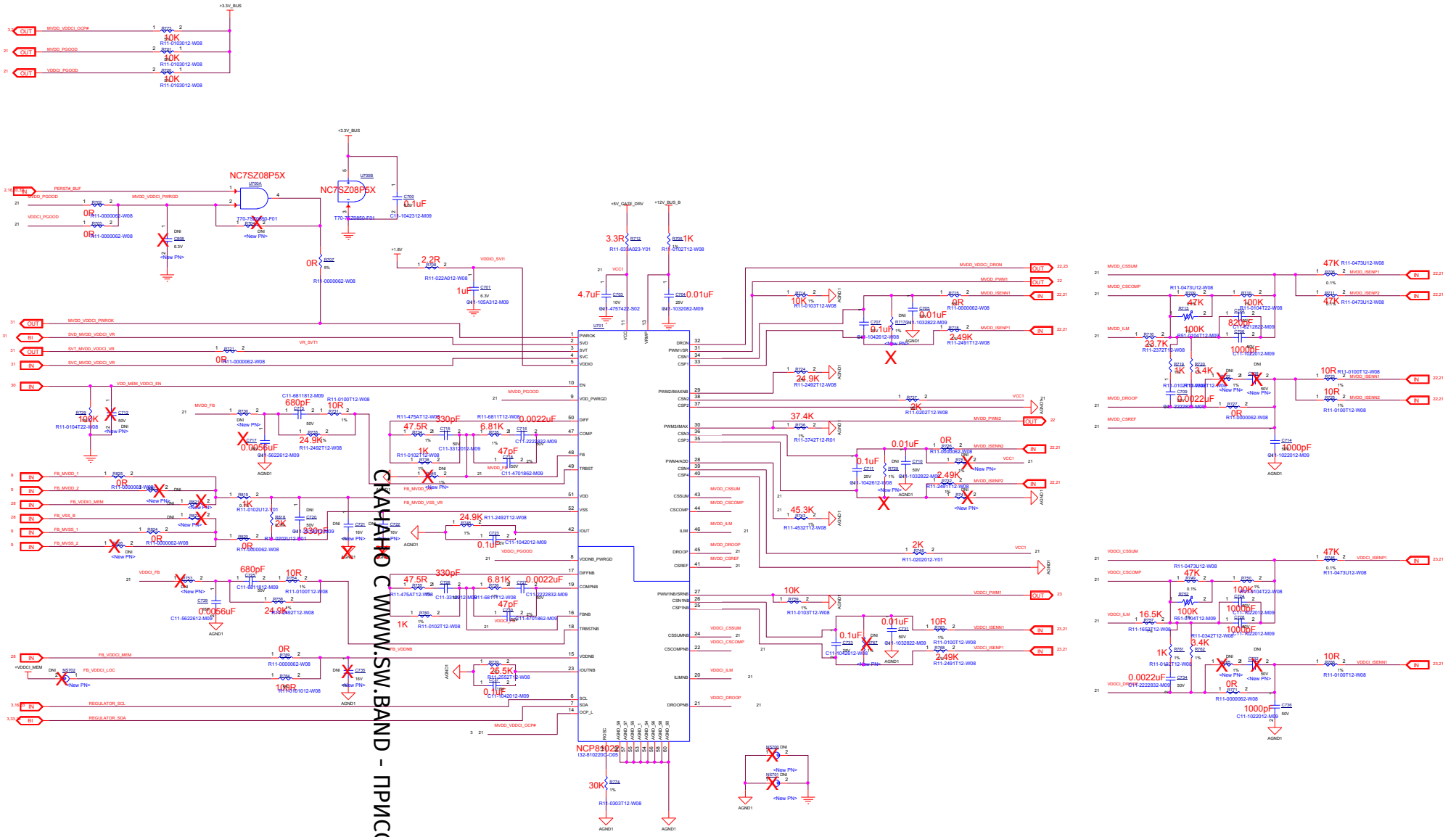

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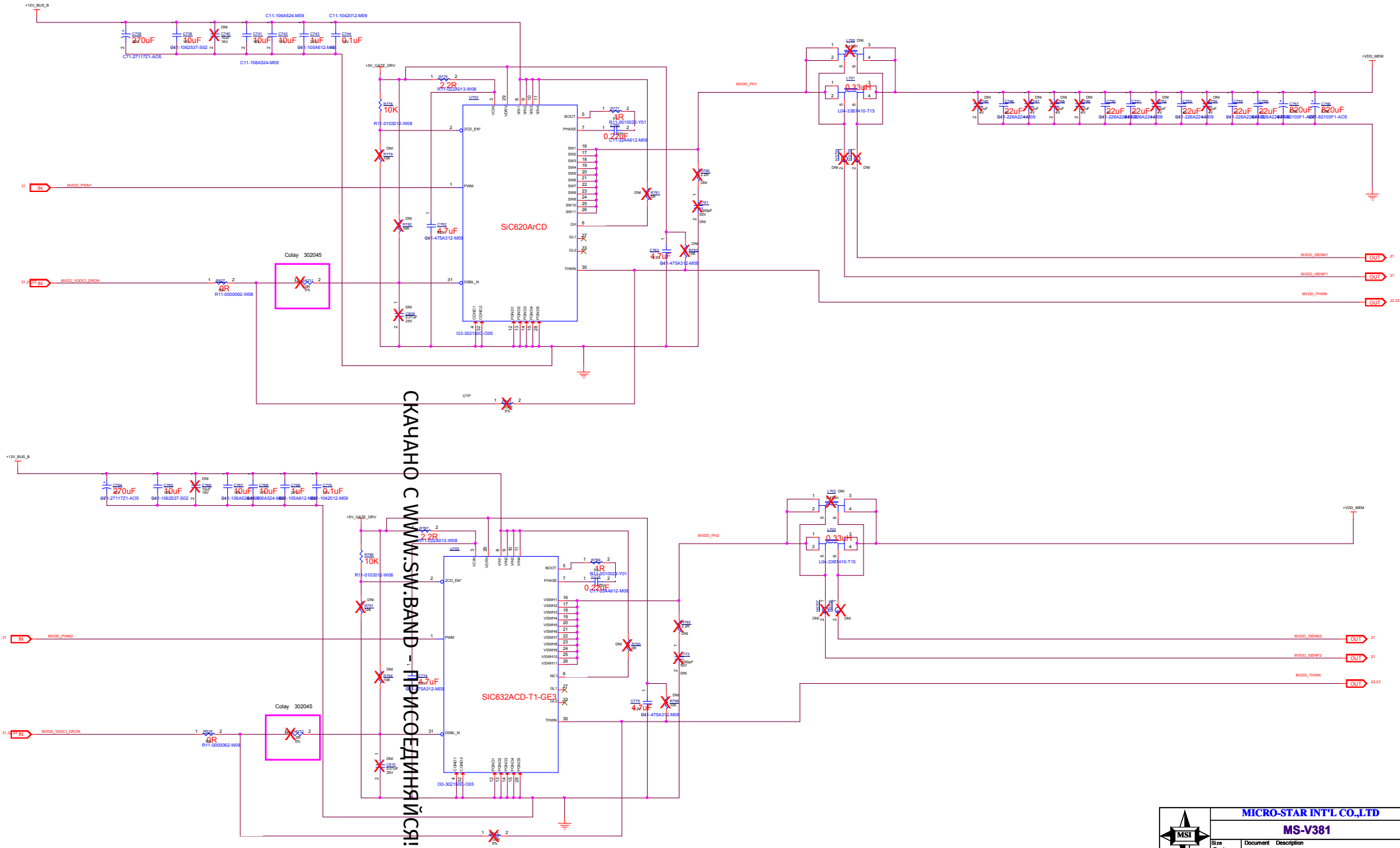

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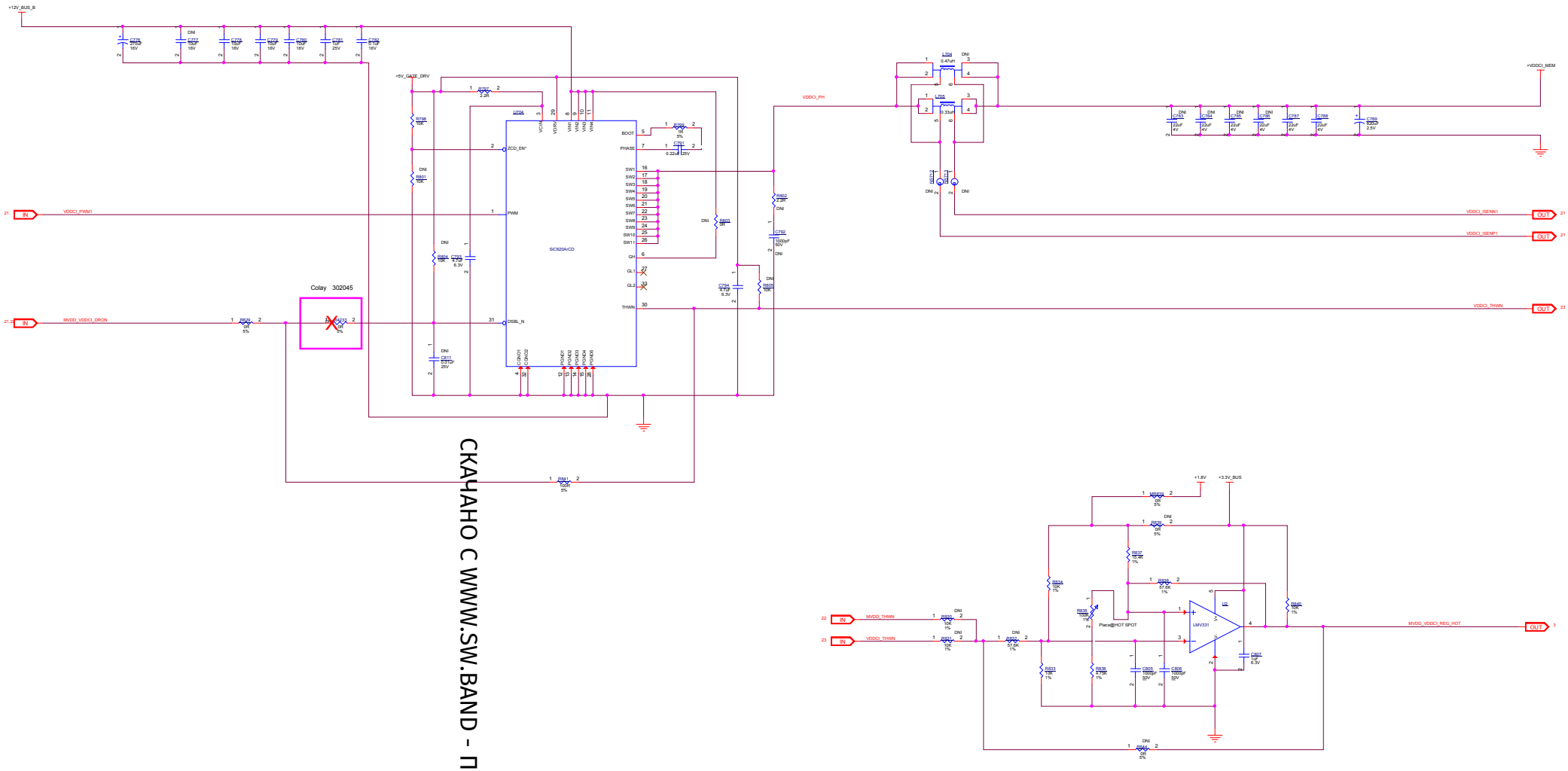

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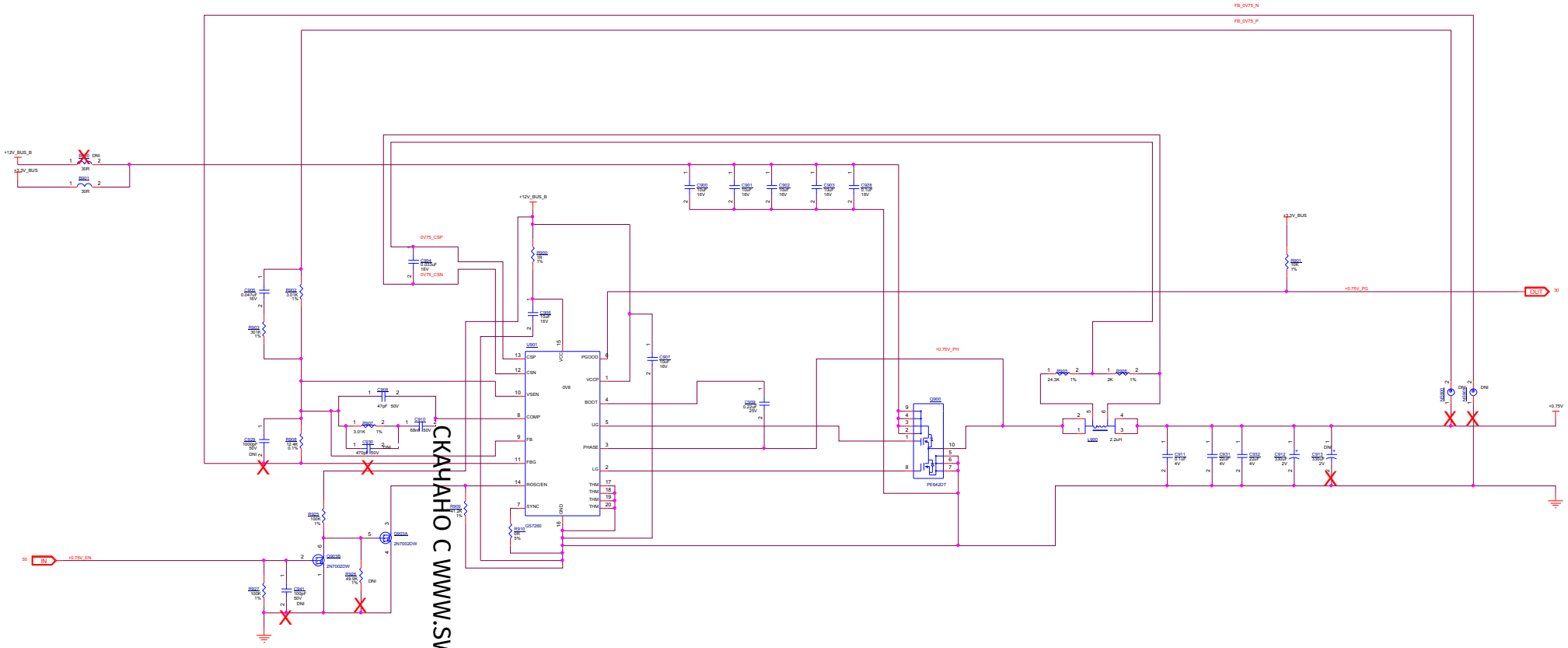

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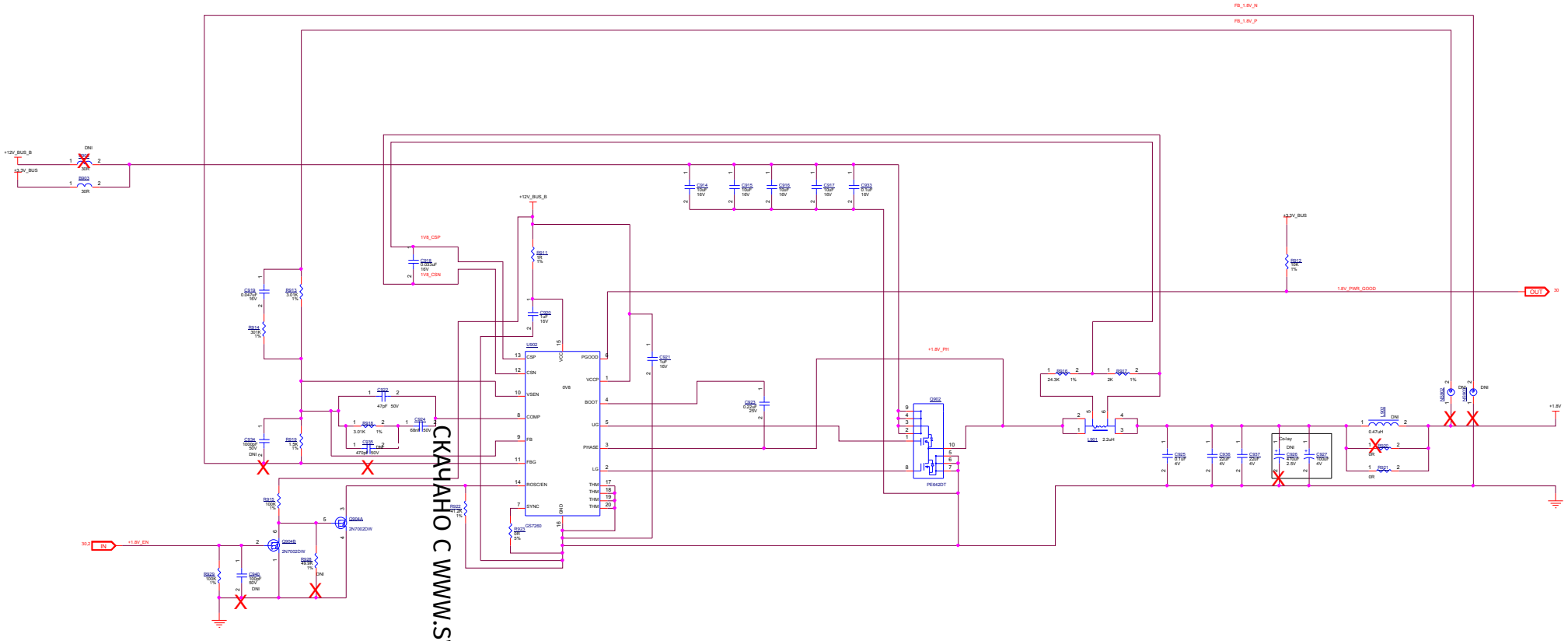

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REGULATOR FOR +5V RAILS

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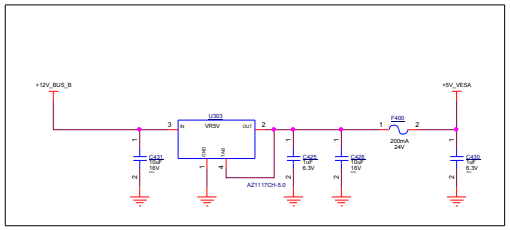

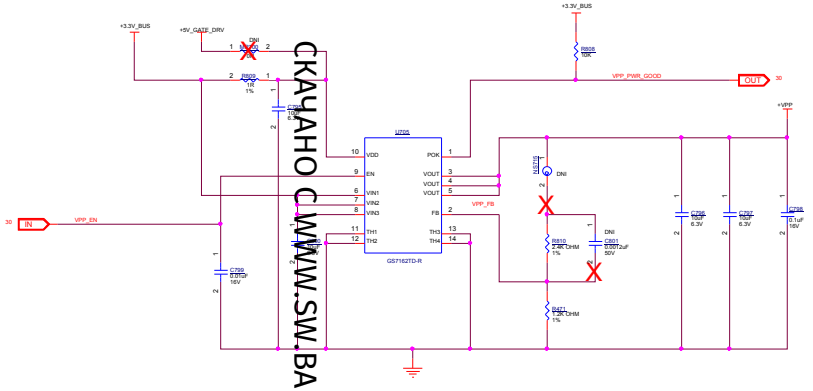

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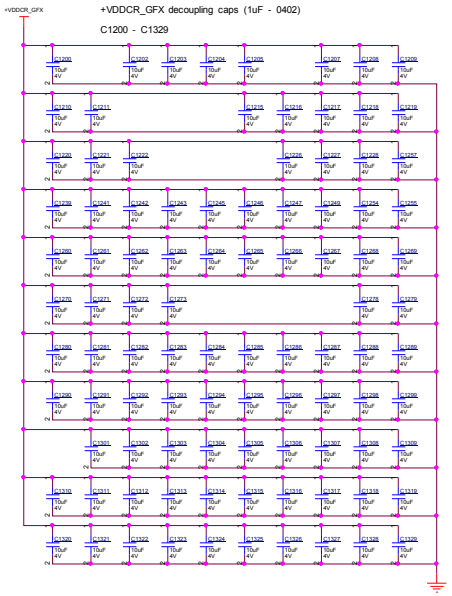
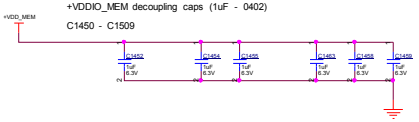
+VDDCR_GFX decoupling caps (1uF - 0402)

C1200 - C1329



+VDDIO_MEM decoupling caps (1uF - 0402)

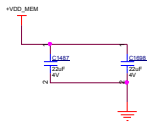
C1450 - C1509



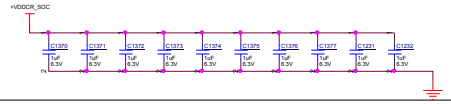
+VDDIO_MEM decoupling caps (22uF)

C1510 - C1539

0805



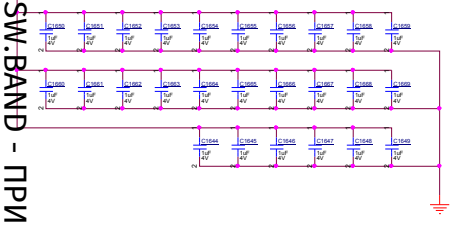
+VDDCR_SOC decoupling caps (1uF - 0402)



+VDDIO_MEM decoupling caps (1uF)

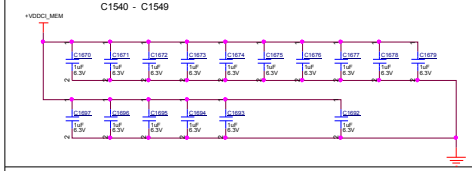
C1650 - C1669

0201



+VDDCI_MEM decoupling caps (1uF - 0402)

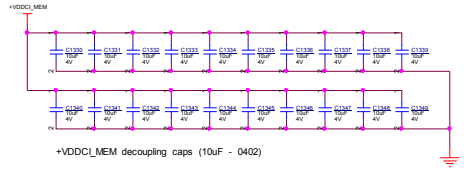
C1540 - C1549



+VDDCI_MEM decoupling caps (22uF - 0805)

C1684 - C1687 C1640 - C1642

+VDDCI_MEM decoupling caps (10uF - 0402)



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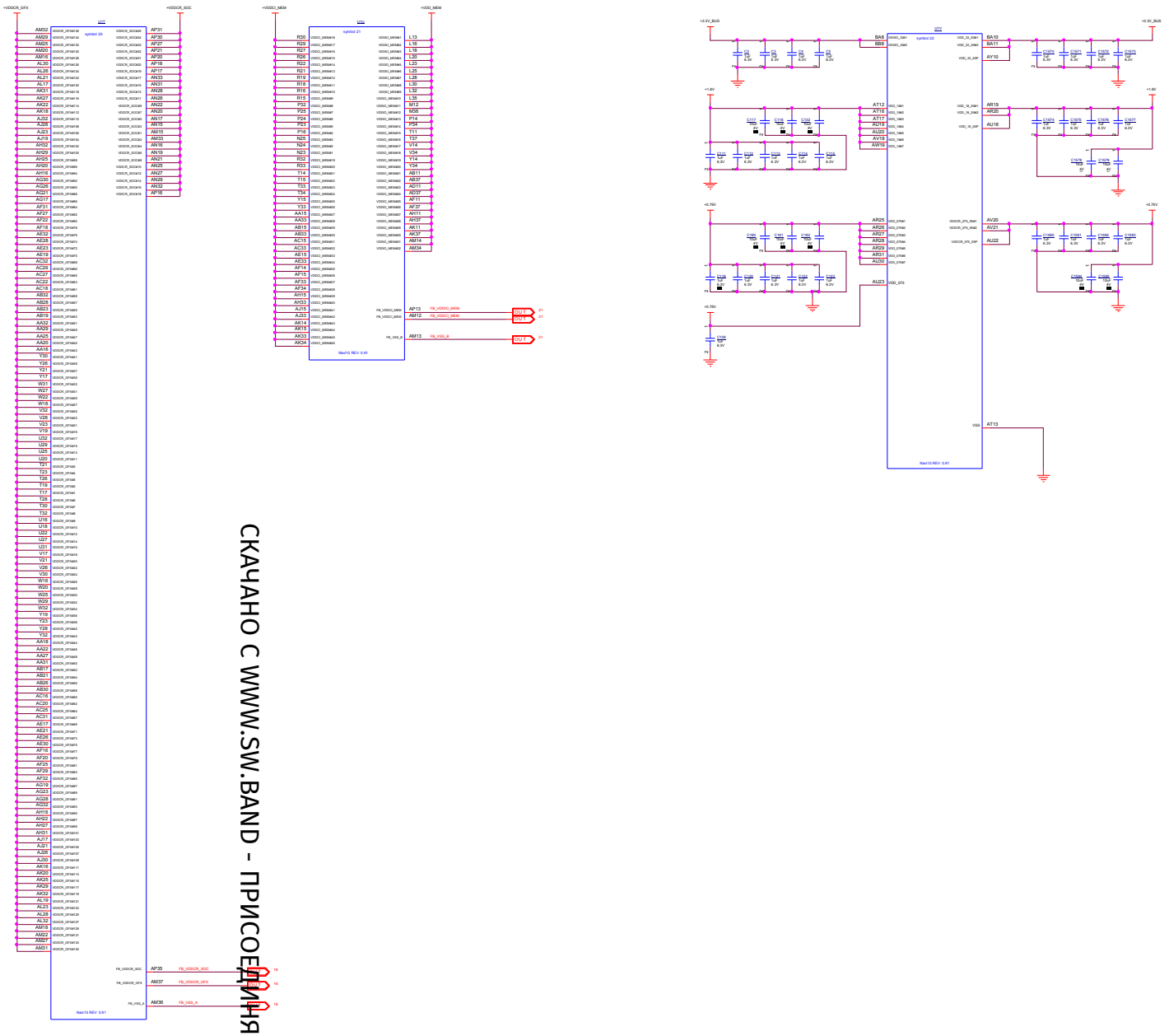

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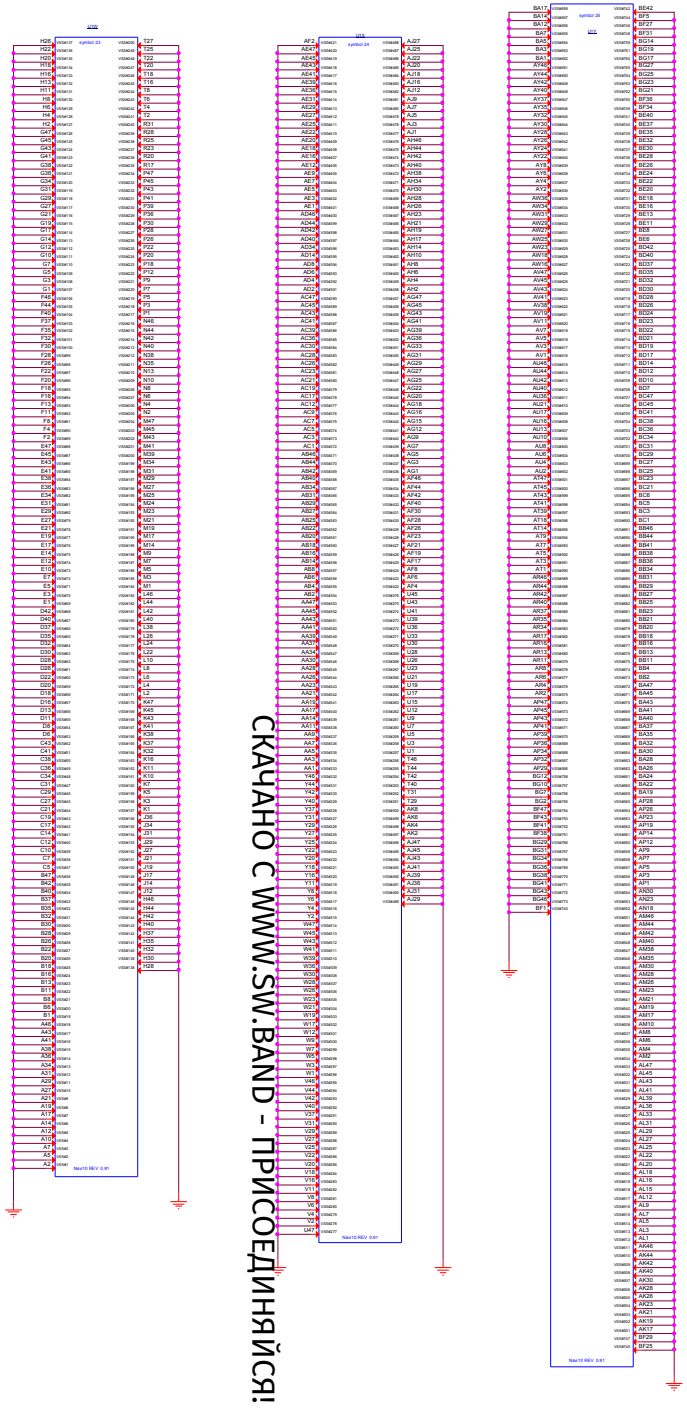

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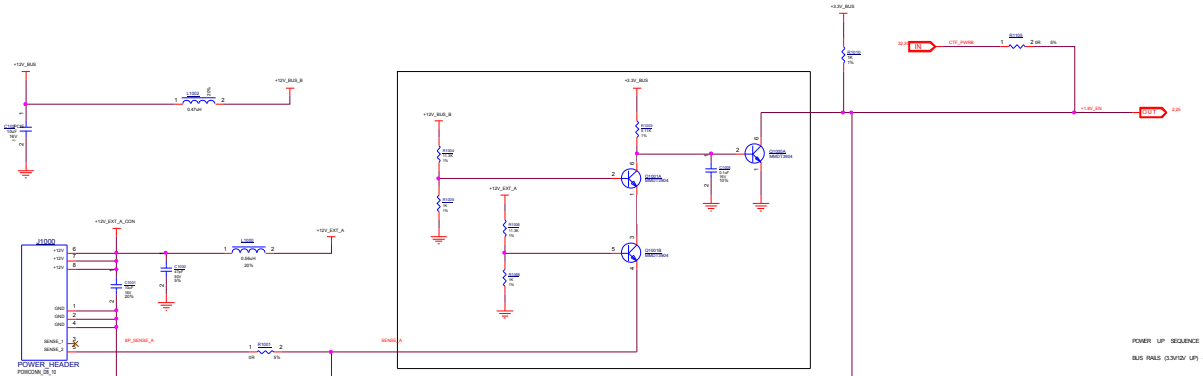
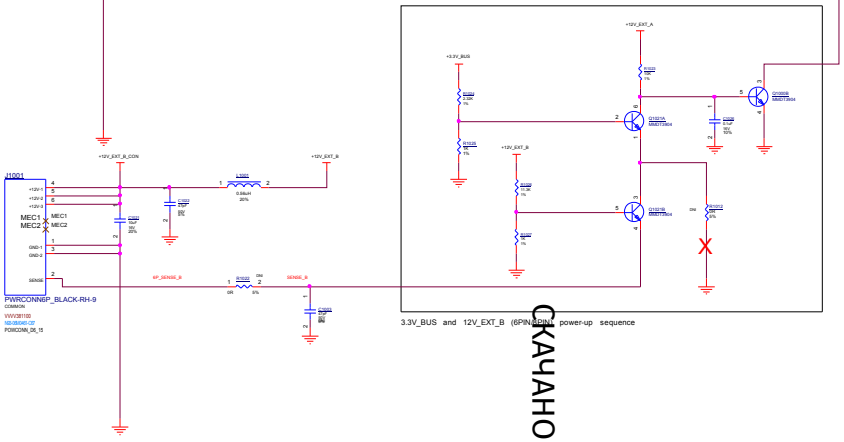
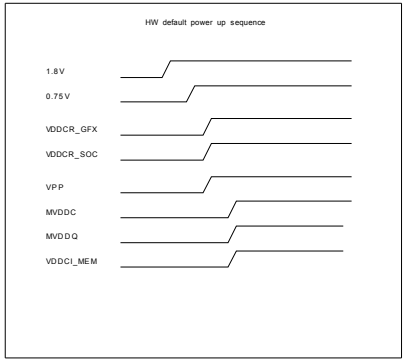
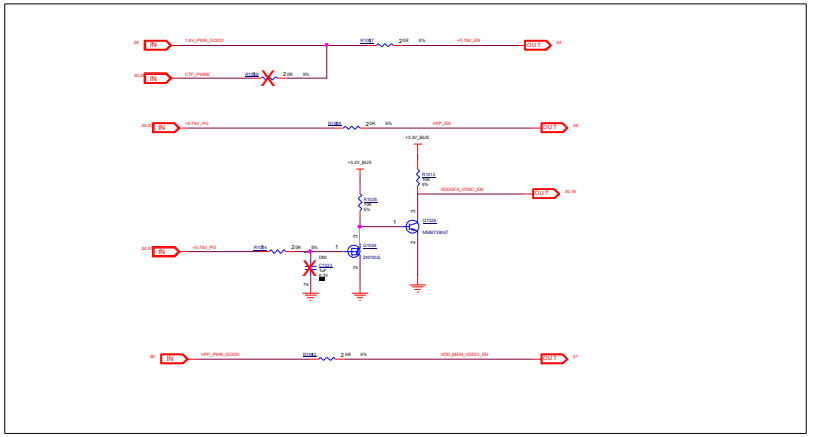






POWER UP SEQUENCE

BUS RAILS (3.3/12V UP) -> +1.8V -> 0.75V -> VDDGFX/VDDSOC -> VPP -> VDDCI/MVDD

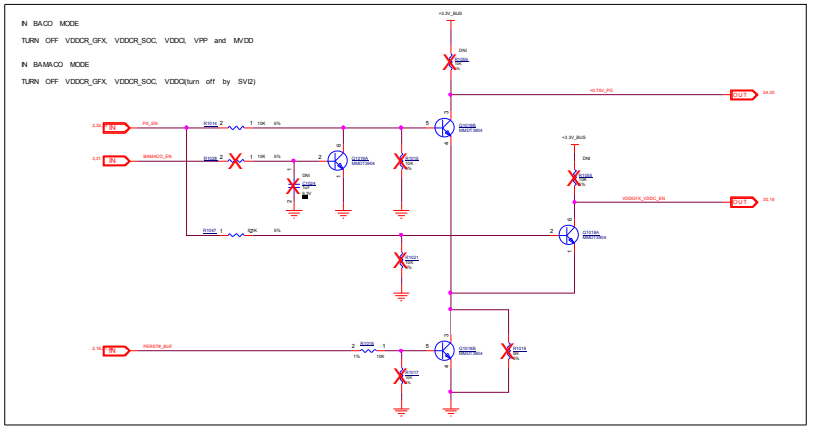


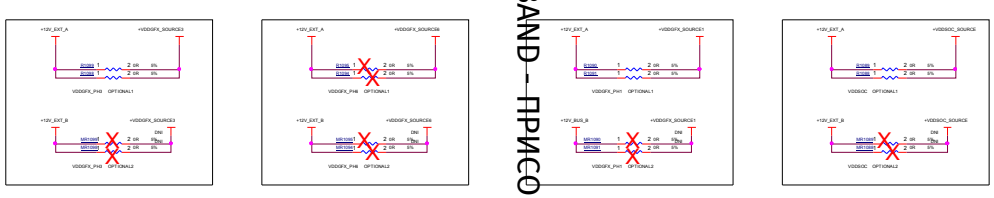
IN BACO MODE

TURN OFF VDDCR_GFX, VDDCR_SOC, VDDCI, VPP and MVDD

IN BAMACO MODE

TURN OFF VDDCR_GFX, VDDCR_SOC, VDDCI(turn off by SVI2)





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MS-V381			
Size: Custom	Document Description: POWER MANAGEMENT		Rev: 5.0
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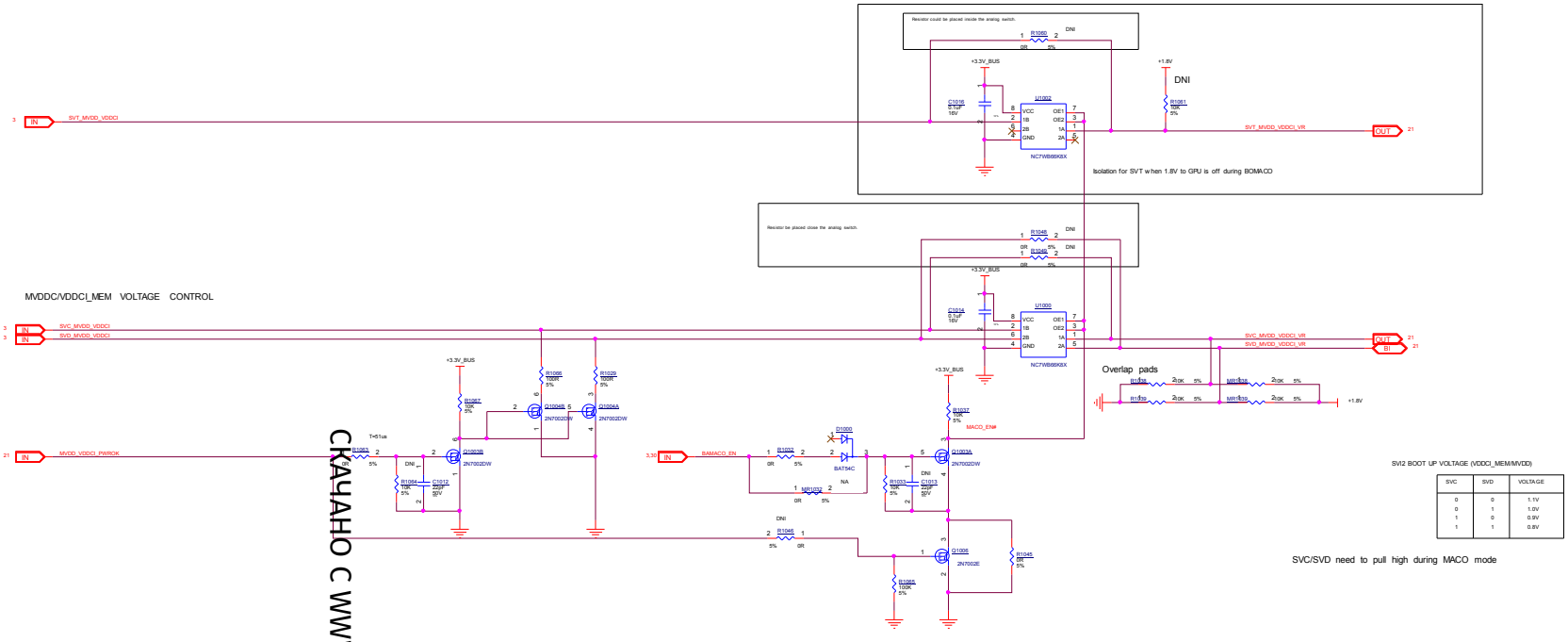

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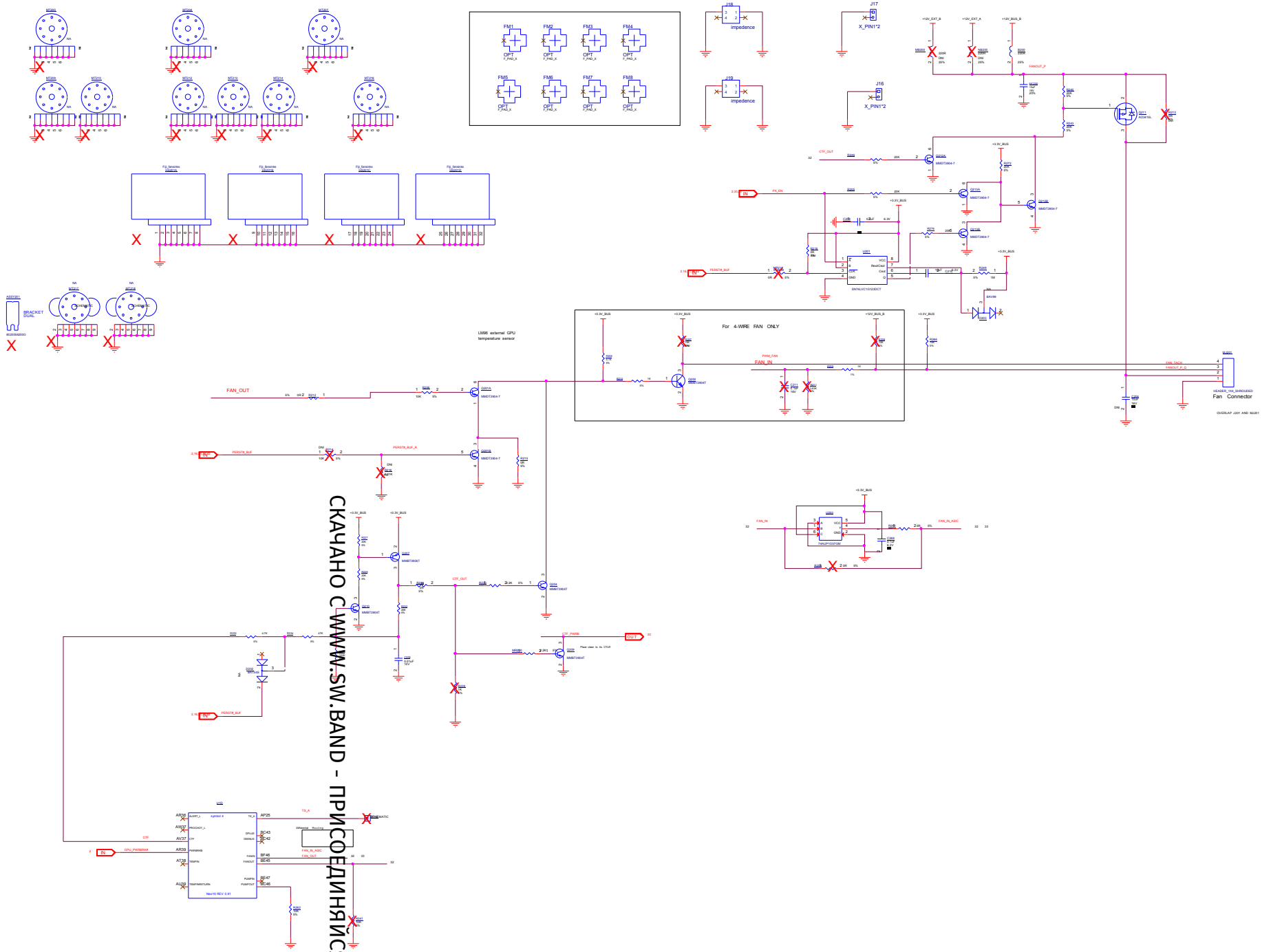

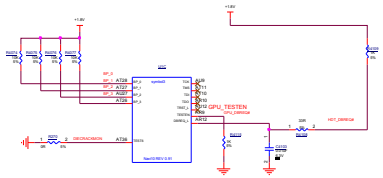

RADEON Lightbar header

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	MS-V381	
Size: Custom	Document Description: DEBUG	Rev: 0.0
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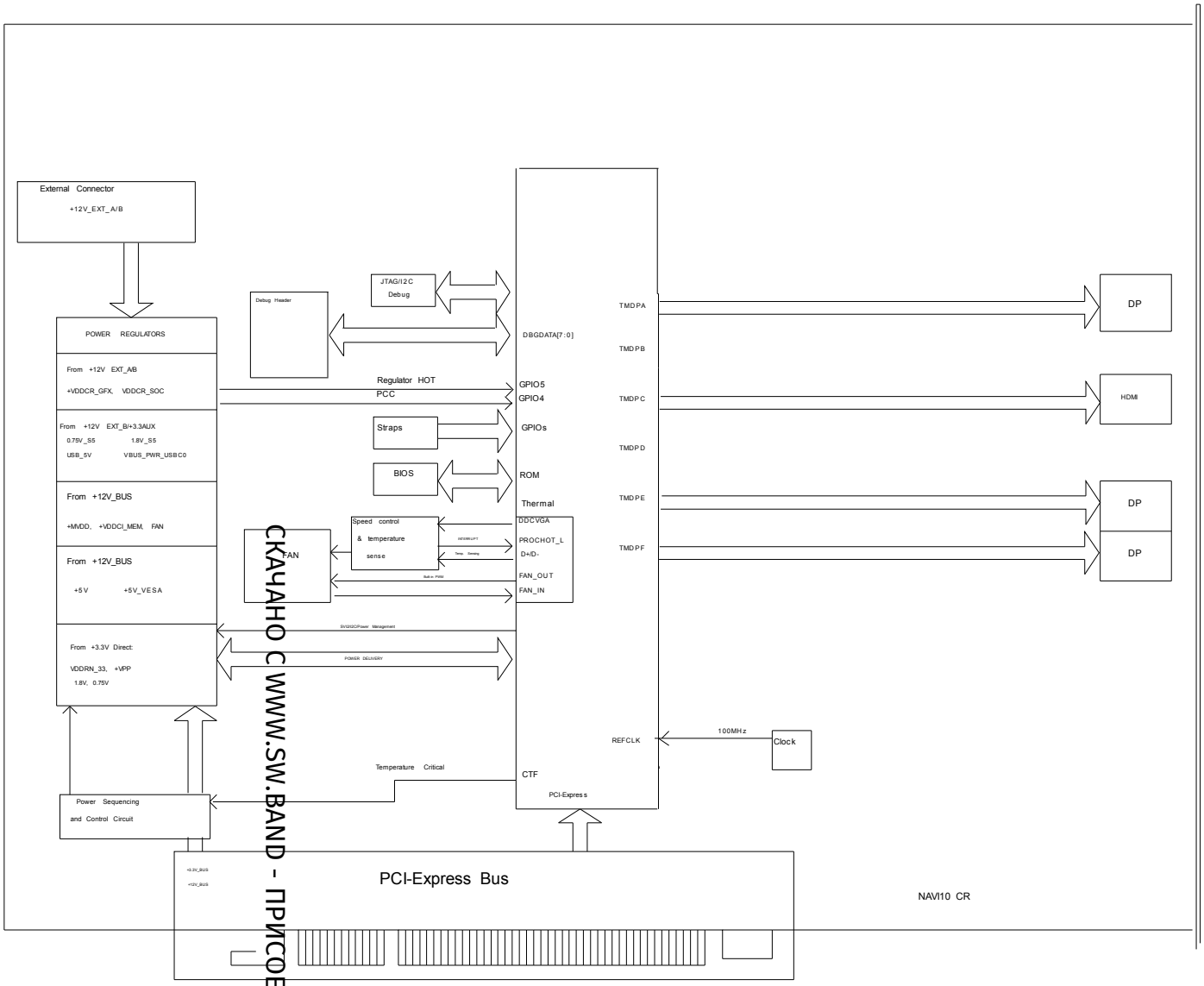

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Size: Custom	Document Description: BLOCK DIAGRAM	Rev: 5.0
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AMD

TITLE: NAVI10 G6X16mode DP DP HDMI DP

DOCUMENT NUMBER: 105_D199xx_00B

DATE: Fri Jun 21 03:44:58 2019

SHEET NUMBER: 35 OF 35

REV: 1.00

REVISION HISTORY

ENGINEER: Peak, Dong

NOTES: NOTE

AMD - PLATFORM HARDWARE ENG
No.669, HUANKE ROAD
SHANGHAI, CHINA 201203

SCH Rev	PCB Rev	Date	REVISION DESCRIPTON
1	-00A	FEB 11 2019	-00A schematics
2	-00B	JUN 21 2019	ADD PULL HIGH ON THE PWRBRKB

2019_11_07 GFX_MEM_SOC_VDDCI Co-Lay 302045 and Power PIN fix to 8+6 reverse type Only

2019_11_11 Add Fan_IN output back Page 32, Change Footprint con_dp_astron_r6890020_tab > con_tab , edgecon_pci_express_gen4_16 > edgecon_16 , Remove MT203, MT 211, MT208 Screw Hole
2019_11_14 add Cross Light point , Remove Page 2 TP detect point, Remove lightbar header, Remove CTF & J4100 debug Pin