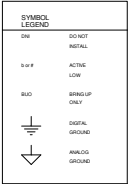
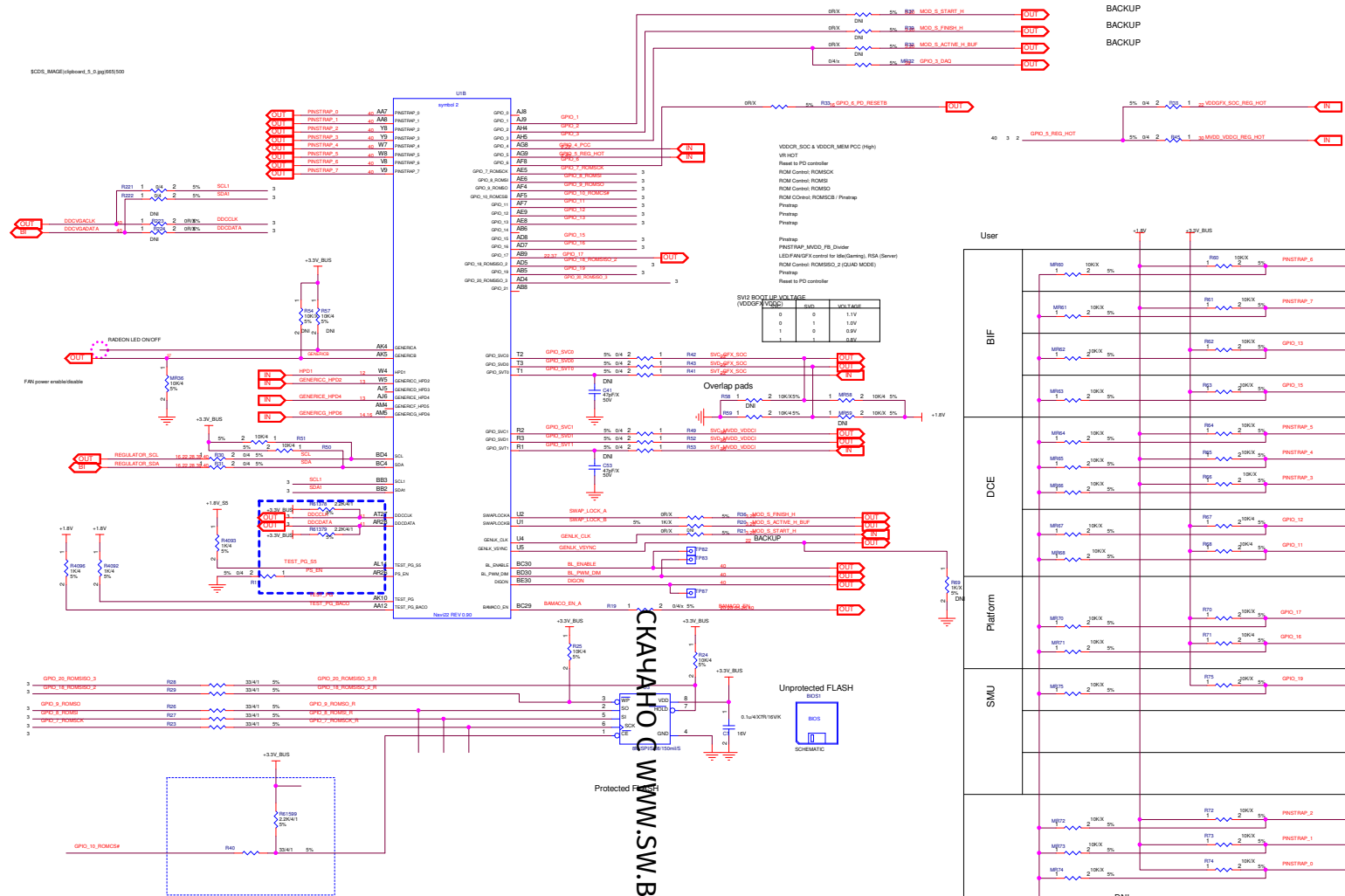


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| 3         | NAVI22 GPIOs             | 28        | MVDD_VDDCI CONTROLLER   |
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| 21        | REG_5V_BUCK              |           |                         |
| 22        | VDDGFX_SOC CONTROLLER    |           |                         |
| 23        | VDDCR_GFX PHASES 2 and 5 |           |                         |
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СКАЧАНО С WWW.S.W.BAND - ПРИСОЕДИНЯЙСЯ

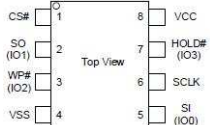




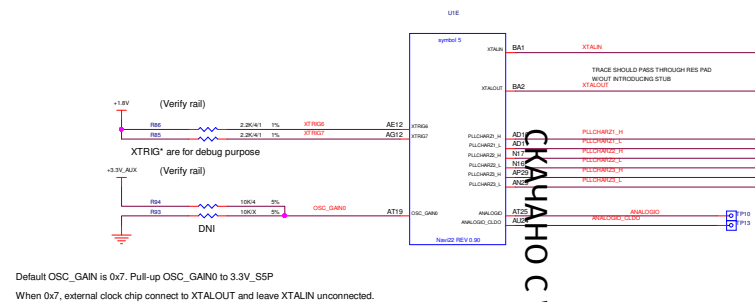
BACKUP  
BACKUP  
BACKUP

Note: Internal PU/PD at GPIO pad is  
length in 14nm design spec

| User     | Internal Default Value | Definition                                                                                                                                                                                                        |
|----------|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BIF      | 0                      | STRAP_BIF_GEN4_DIS_A<br>0: PCw GEN4 is supported<br>1: PCw GEN4 is not supported                                                                                                                                  |
|          | 0                      | PINSTRAP_BIF_CLK_PM_EN<br>0: CLARESC power management capability is disabled<br>1: CLARESC power management capability is enabled                                                                                 |
|          | 0                      | PINSTRAP_BIF_LC_TX_SWING<br>0: VGA controller capability is enabled<br>1: The device won't be recognized as the system VGA controller                                                                             |
| DCE      | 0                      | PINSTRAP_BIF_VGA_DIS<br>0: VGA controller capability is enabled<br>1: The device won't be recognized as the system VGA controller                                                                                 |
|          | 0                      | PINSTRAP_AUD_PORT_CONN[2:0]<br>Number of audio-capable display outputs<br>0: 0 endpoints connected<br>1: 1 endpoint connected<br>2: 2 endpoints connected<br>3: 3 endpoints connected<br>4: 4 endpoints connected |
|          | 0                      | PINSTRAP_AUD[1:0]<br>1: Audio for DisplayPort only<br>2: Audio for DisplayPort and HDMI if display is detected<br>3: Audio for DisplayPort and native HDMI                                                        |
| Platform | 0                      | PINSTRAP_BOARD_CONFIG[2:0]<br>LEDFanGPIO control for idle power                                                                                                                                                   |
|          | 0                      | PINSTRAP_MVDD_BOOT_VID_CONFIG<br>0: Pullup without feedback divider<br>1: Pullup with feedback divider enabled                                                                                                    |
|          | 0                      | PINSTRAP_SMBUS_ADDR<br>0: 0x40<br>1: 0x40                                                                                                                                                                         |
| SMU      | 0                      | PINSTRAP_ROM_CONFIG[2:0] 101<br>0: Disable the external BIOS ROM device<br>1: Enable the external BIOS ROM device                                                                                                 |
|          | 1                      |                                                                                                                                                                                                                   |
|          | 0                      |                                                                                                                                                                                                                   |
| DNI      | 0                      |                                                                                                                                                                                                                   |
|          | 1                      |                                                                                                                                                                                                                   |
|          | 0                      |                                                                                                                                                                                                                   |

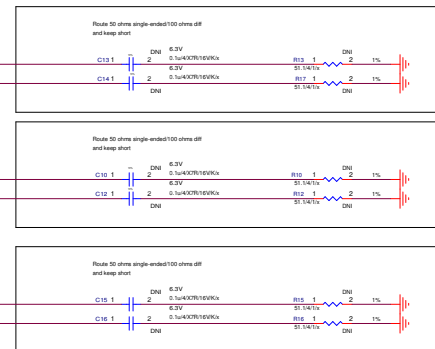
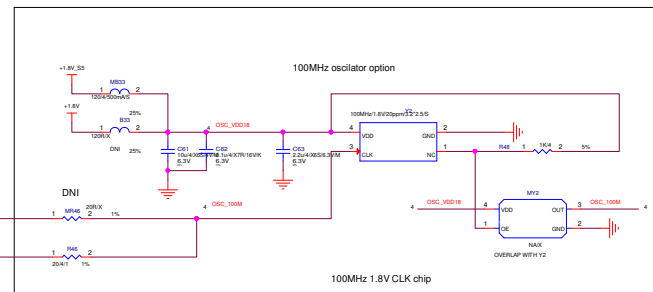


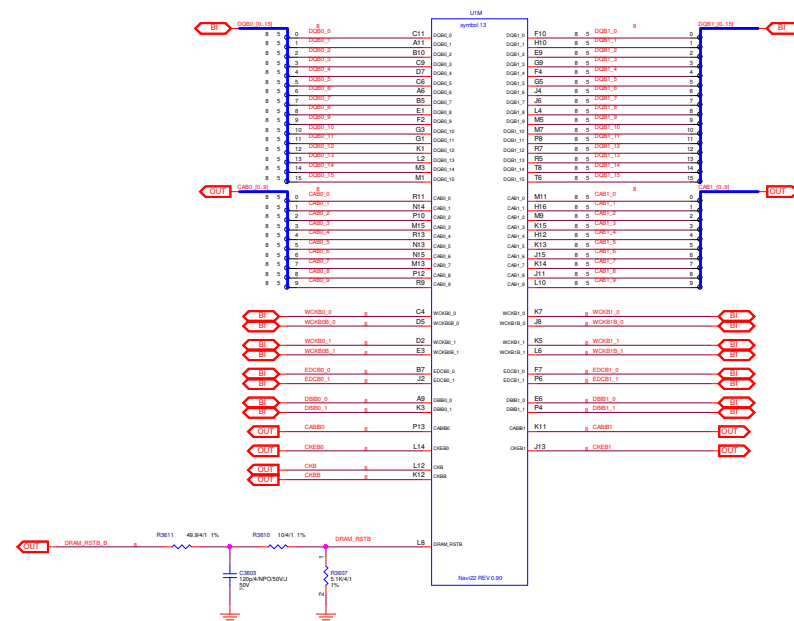
**GIGABYTE™**

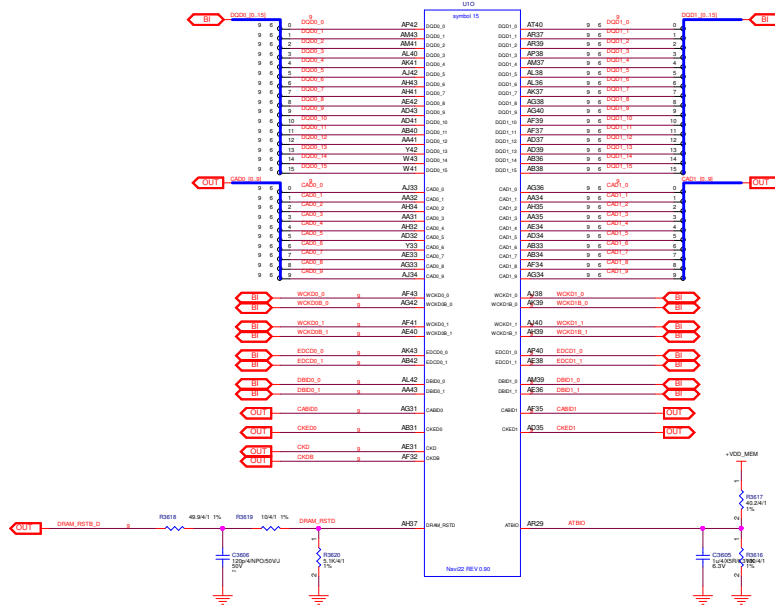


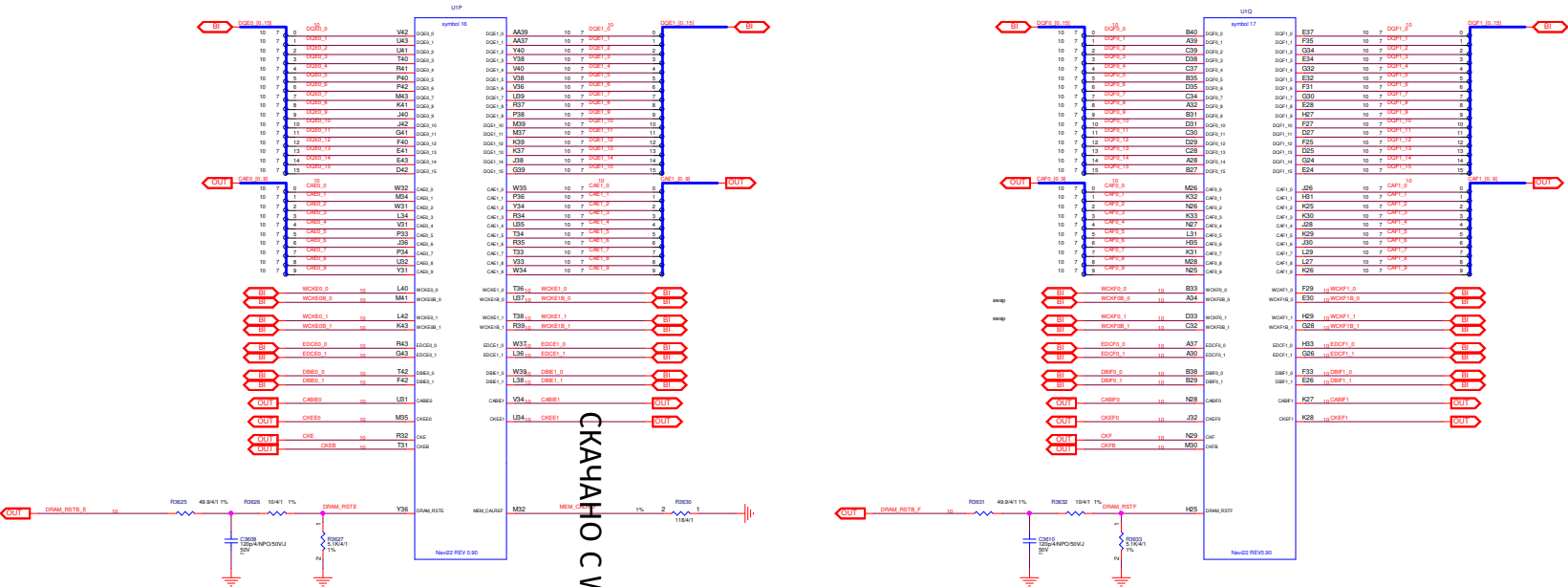
Default OSC\_GAIN is 0x7. Pull-up OSC\_GAIN0 to 3.3V\_SSP  
When 0x7, external clock chip connect to XTALOUT and leave XTALIN unconnected.

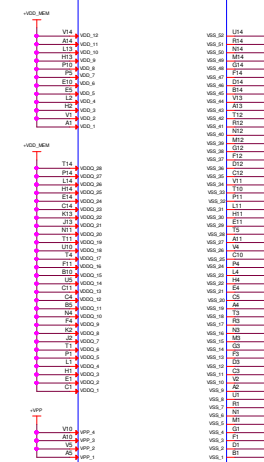
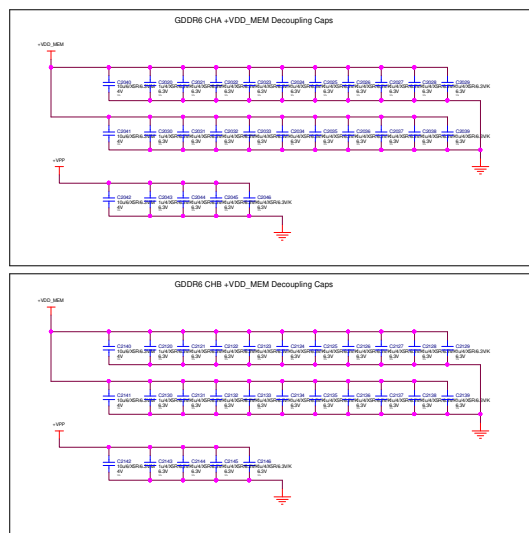
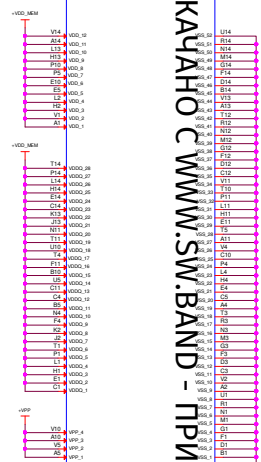
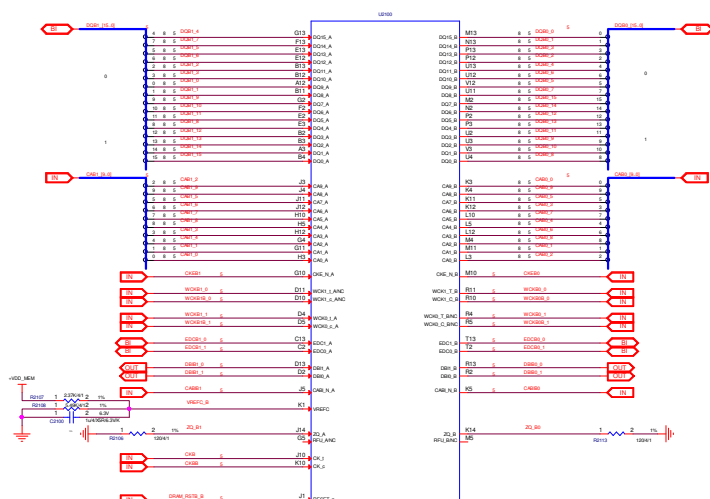
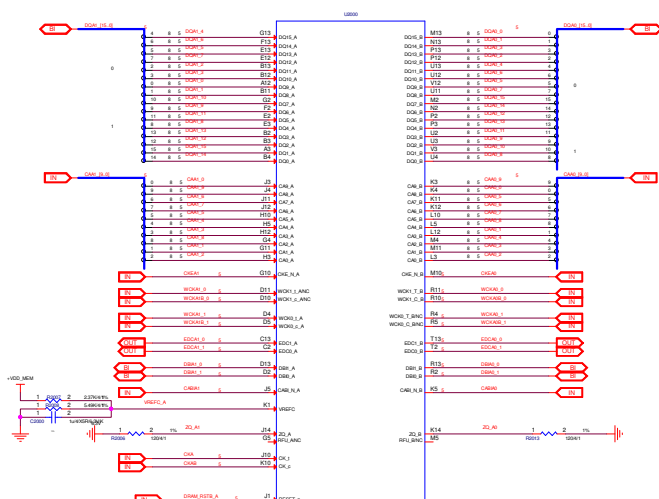
СКАЧАНО С WWW.S.W.BAND - ПРИСОЕДИНЯЯСЯ

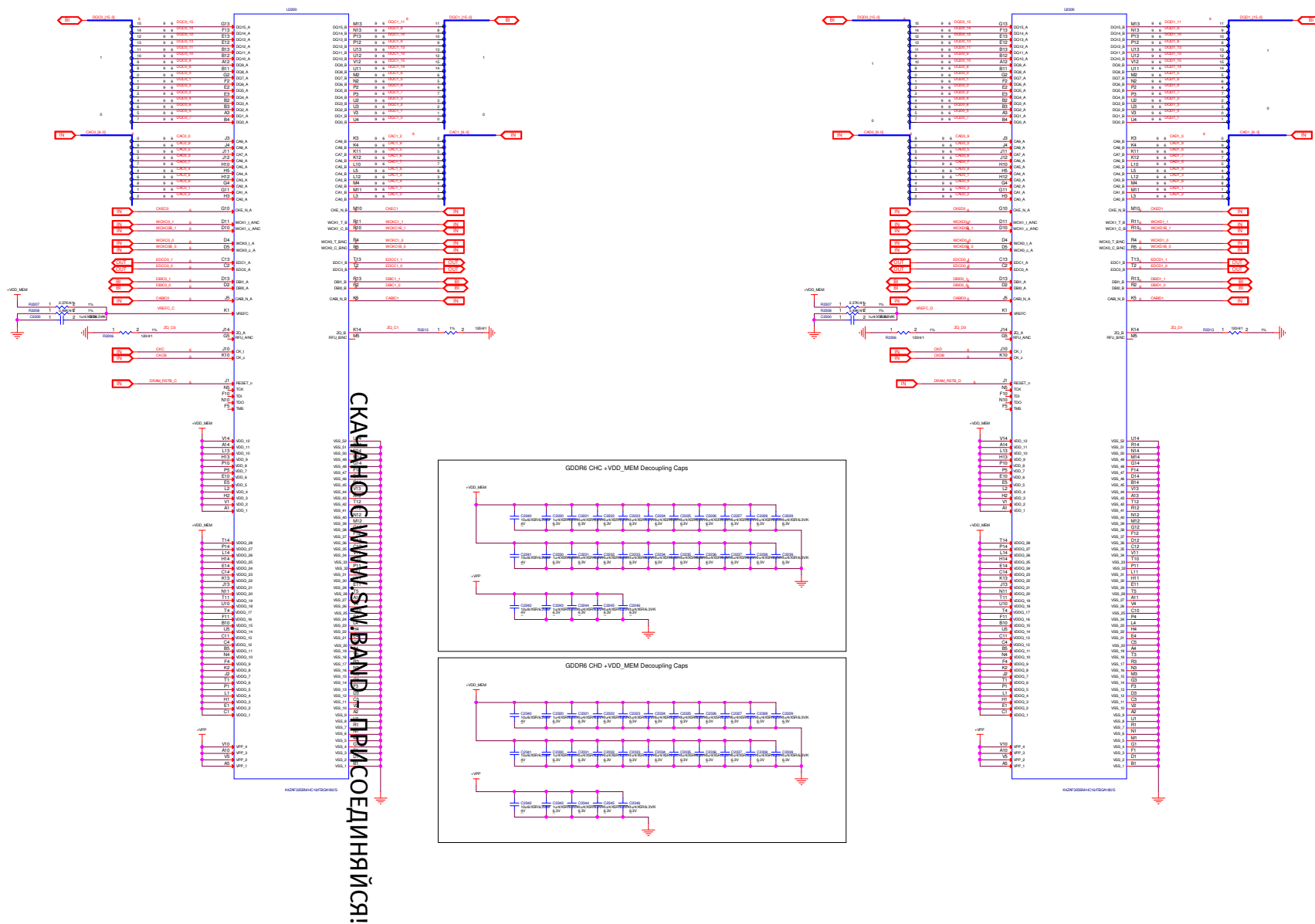


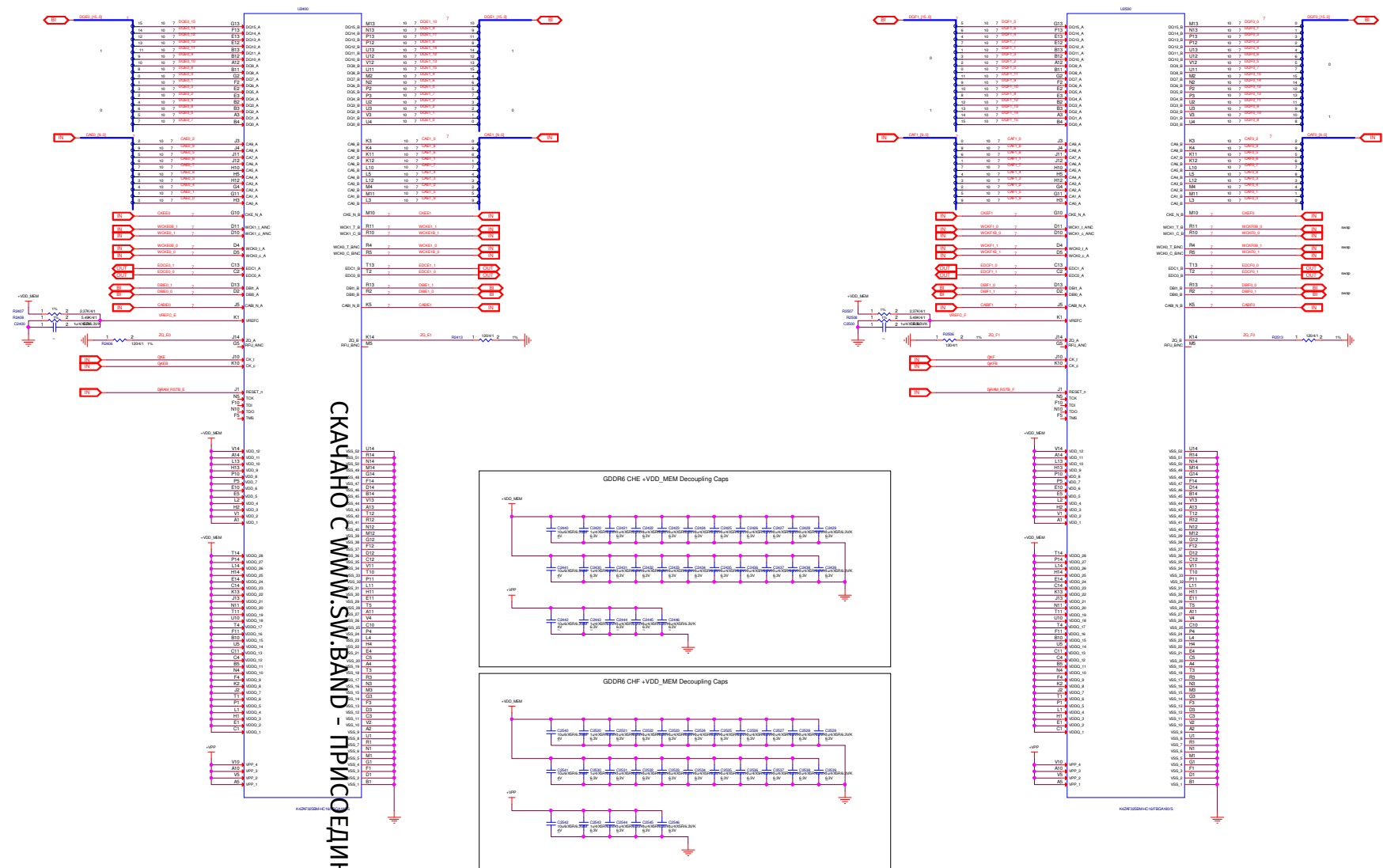




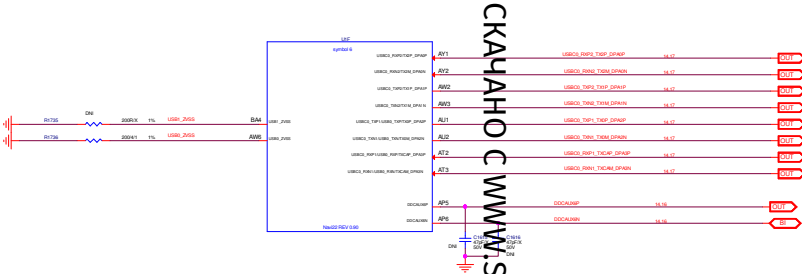
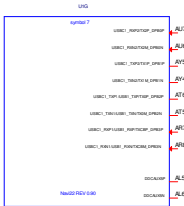






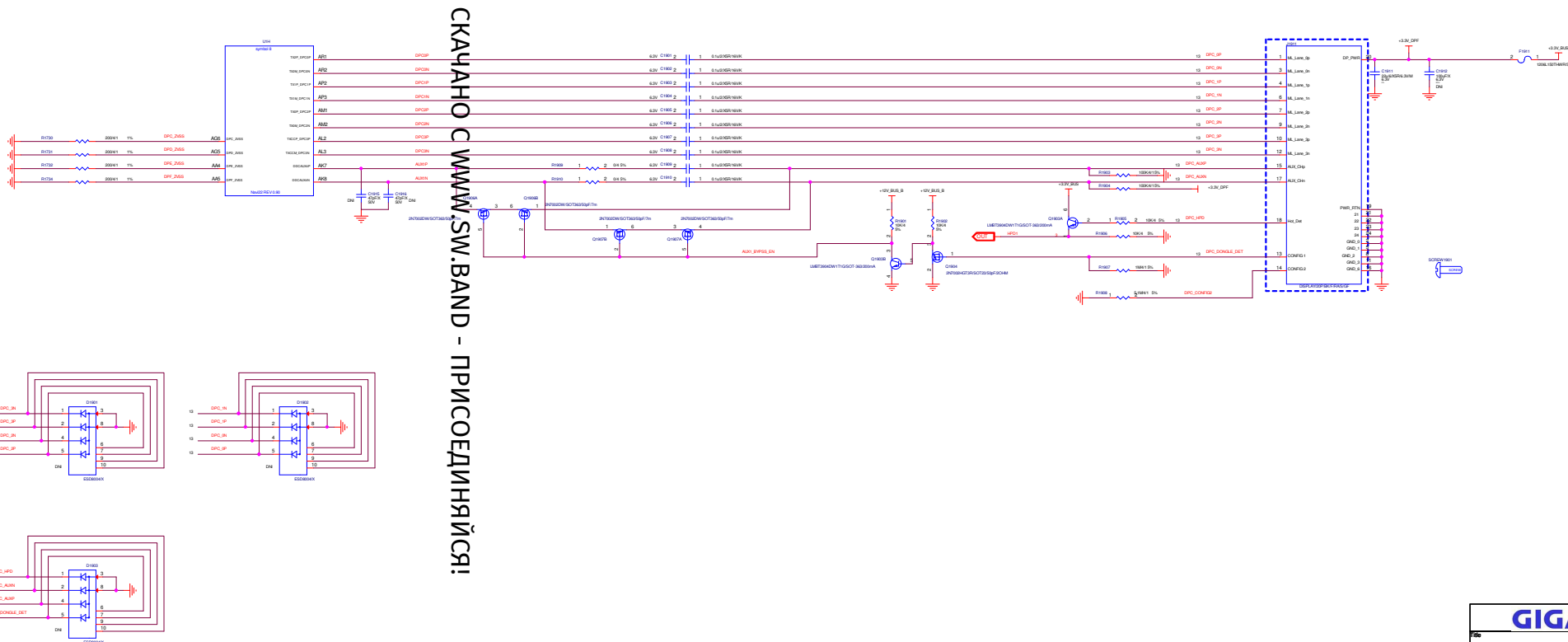


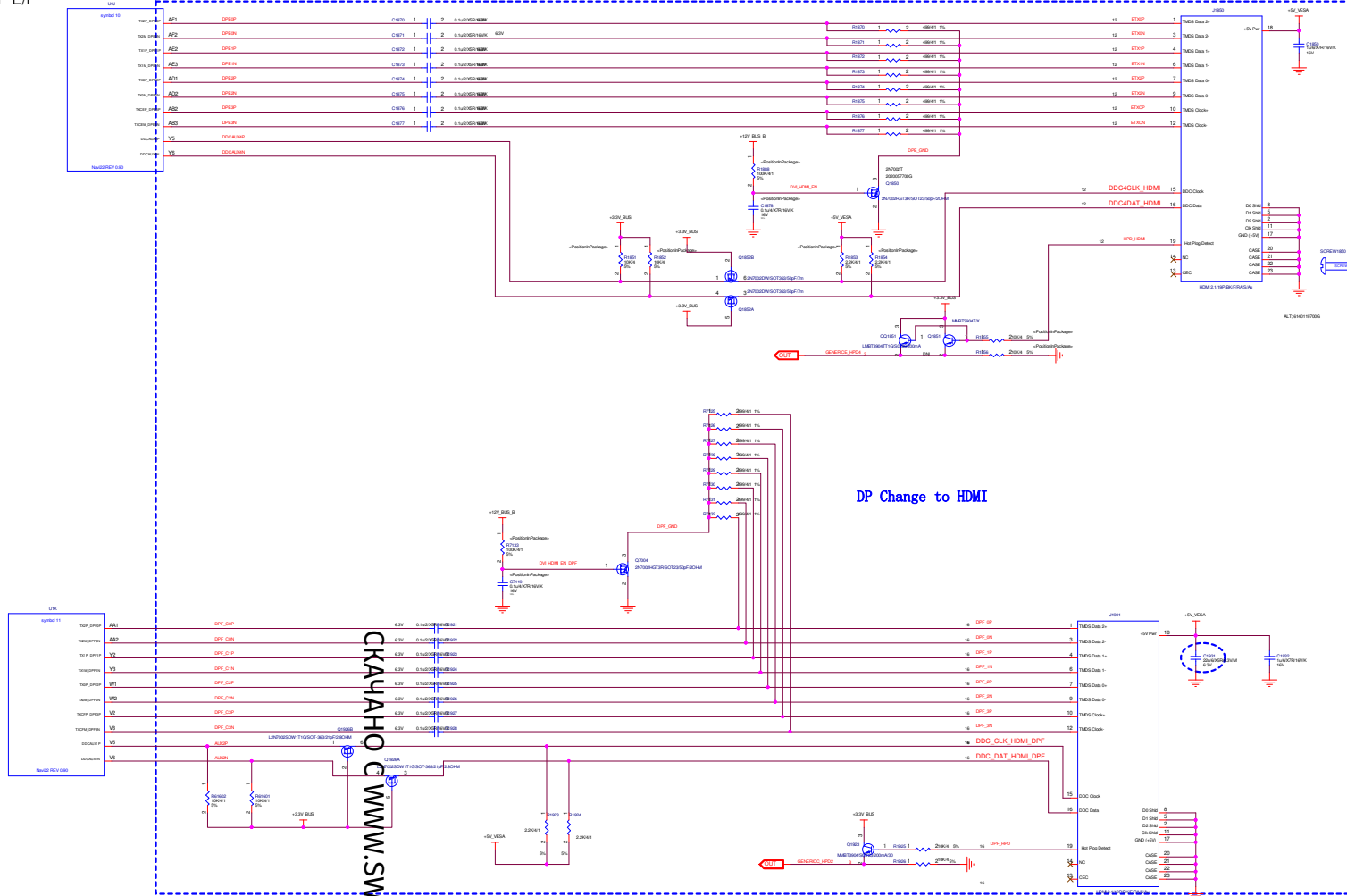
СКАЧАНО С WWW.SV.BAND - ПРИСОЕДИНЯЙСЯ!



СКАЧАНО С WWW.SW.BAND - ПРИСОЕДИНЯЙСЯ!

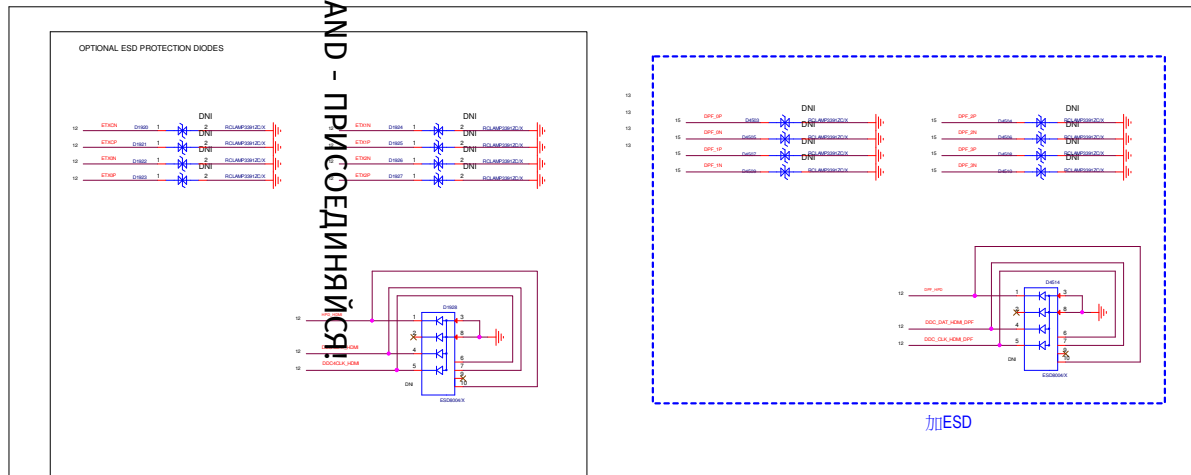
## NAVI22 TMDP C/D



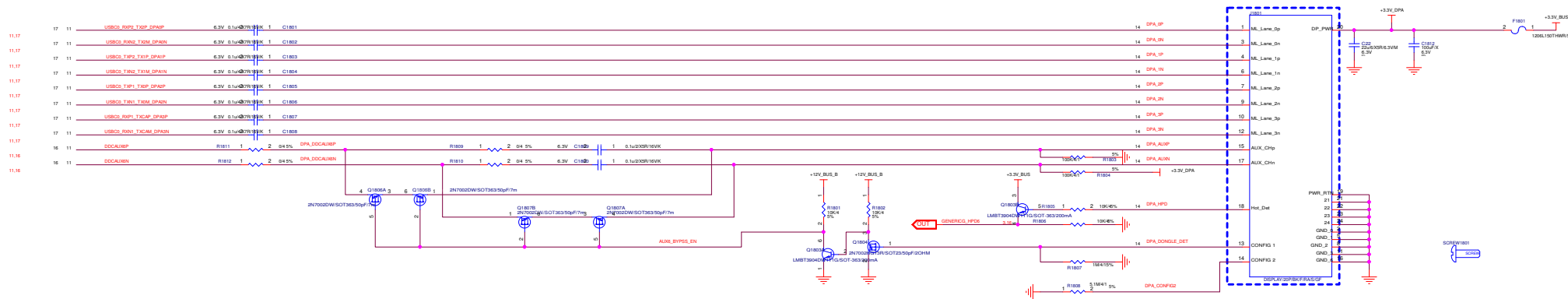


DP Change to HDMI

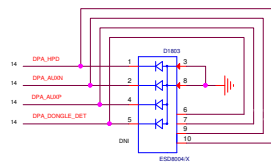
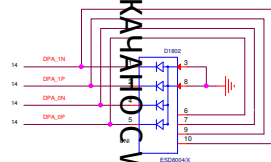
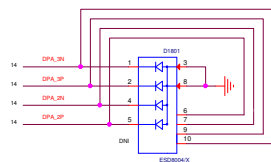
СКАЧАНО С WWW.SW.BAND - ПРИСОЕДИНЯЙСЯ!



加ESD

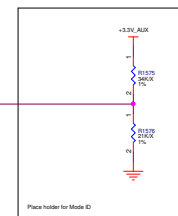
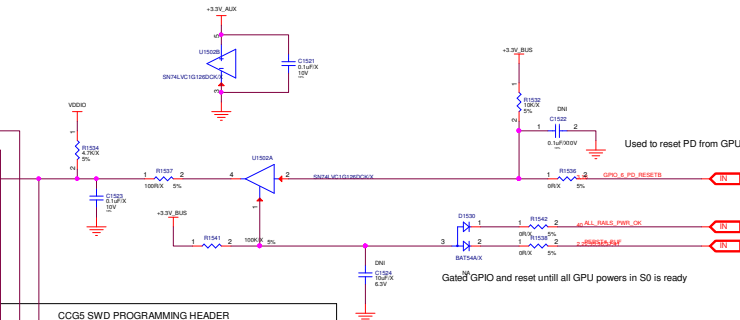
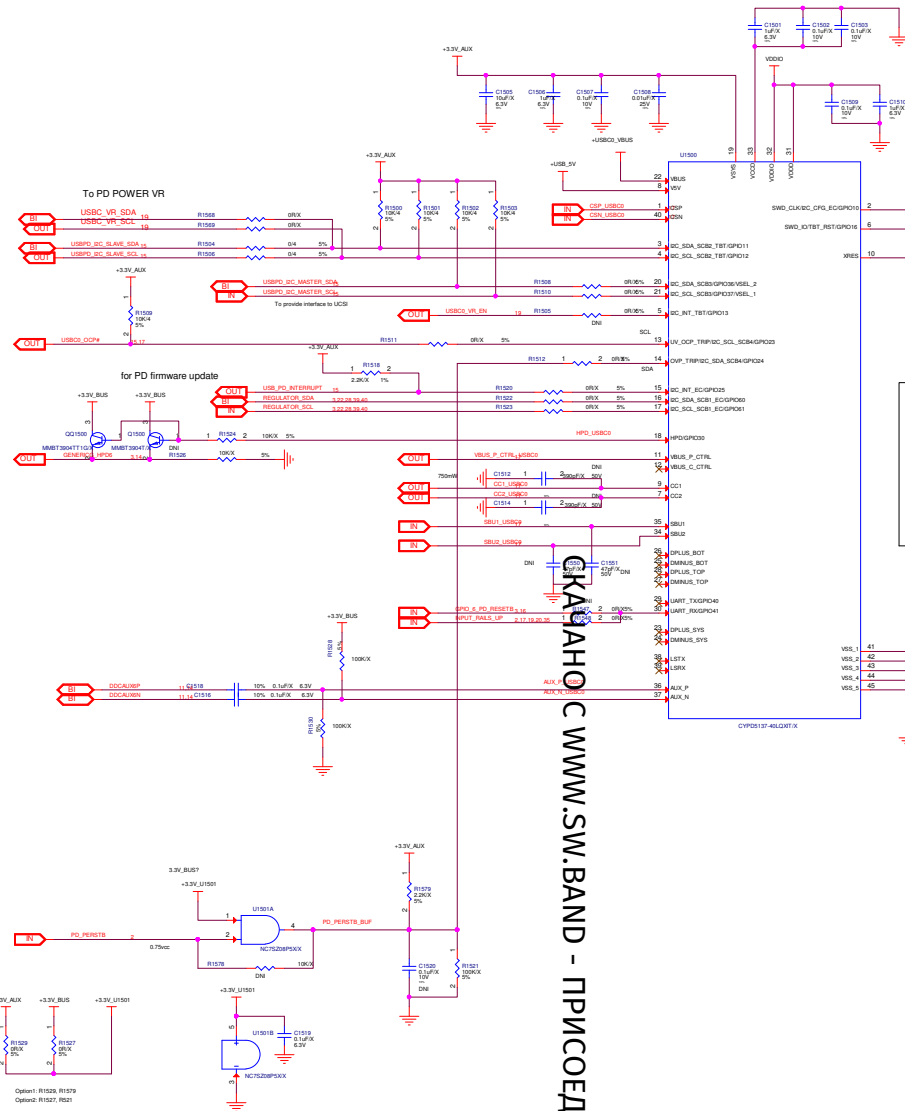


Overlap with USBC



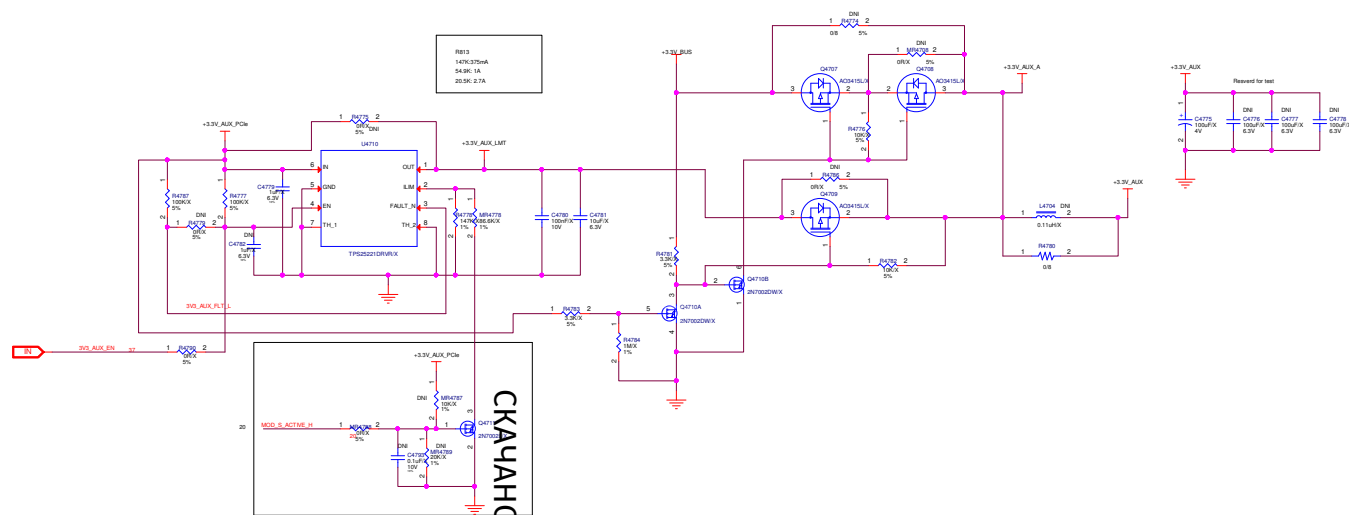
СКАЧАНО С WWW.S.W.BAND - ПРИСОЕДИНЯЙСЯ



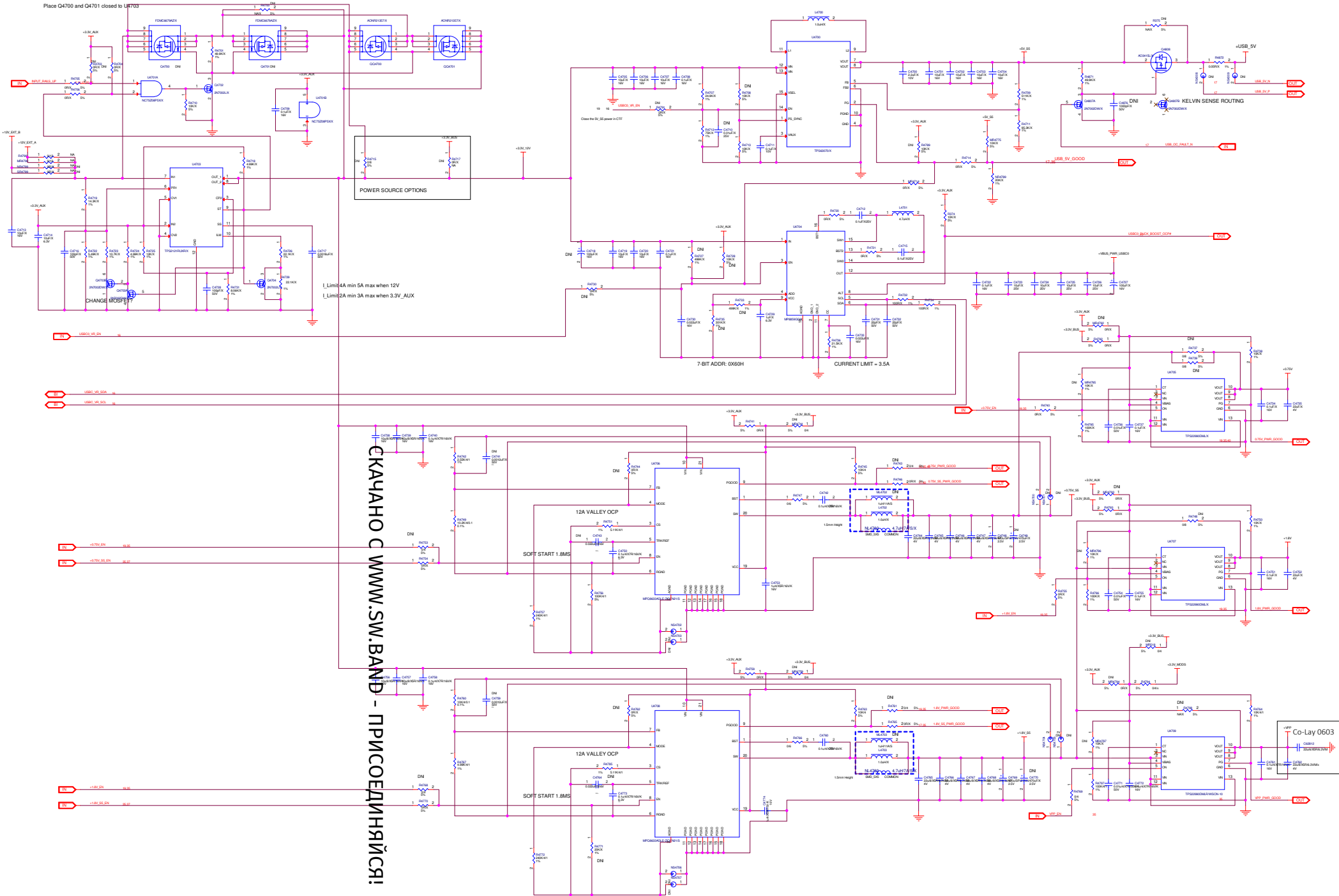


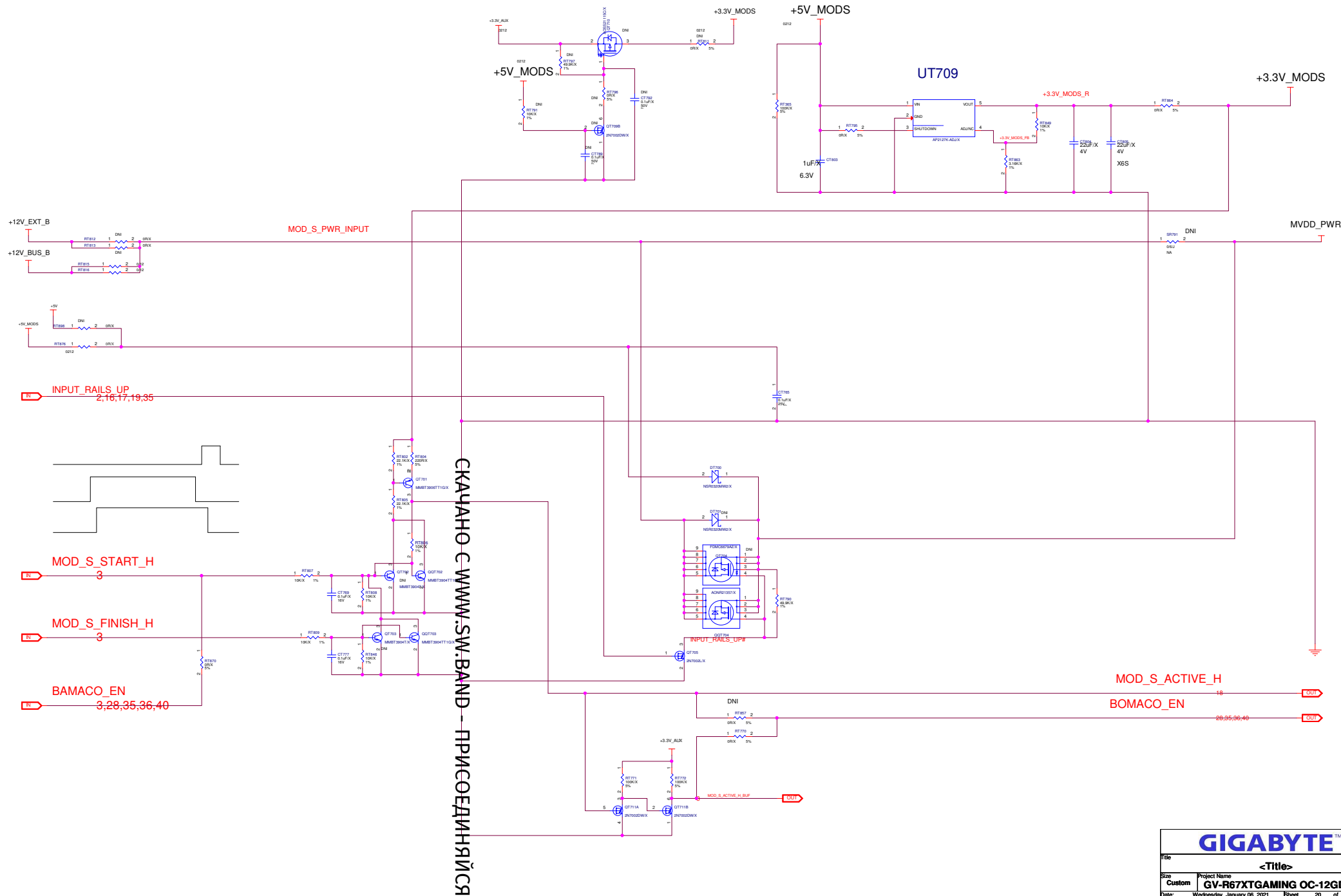
| CG55 | Nav10                                                   | Note                           |
|------|---------------------------------------------------------|--------------------------------|
| SCB1 | SDA/SCL<br><small>sdapcb_uart_0_0_page2840-1049</small> | Firmware update/SMU            |
| SCB2 | USBDP_I2C_SLAVE_SDA/SCL<br>USBC_VR_SDA/SCL              | Nav10 MUX/PD_Regulator/re-driv |
| SCB3 | USBDP_I2C_MASTER_SDA/SCL                                | UCSI                           |

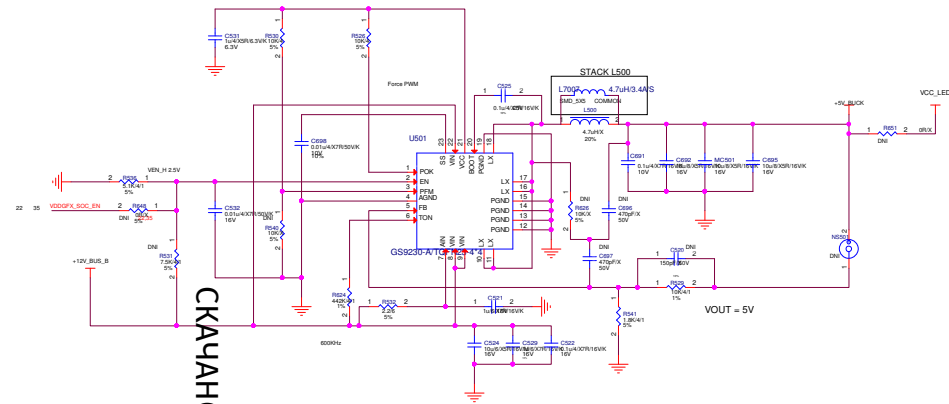




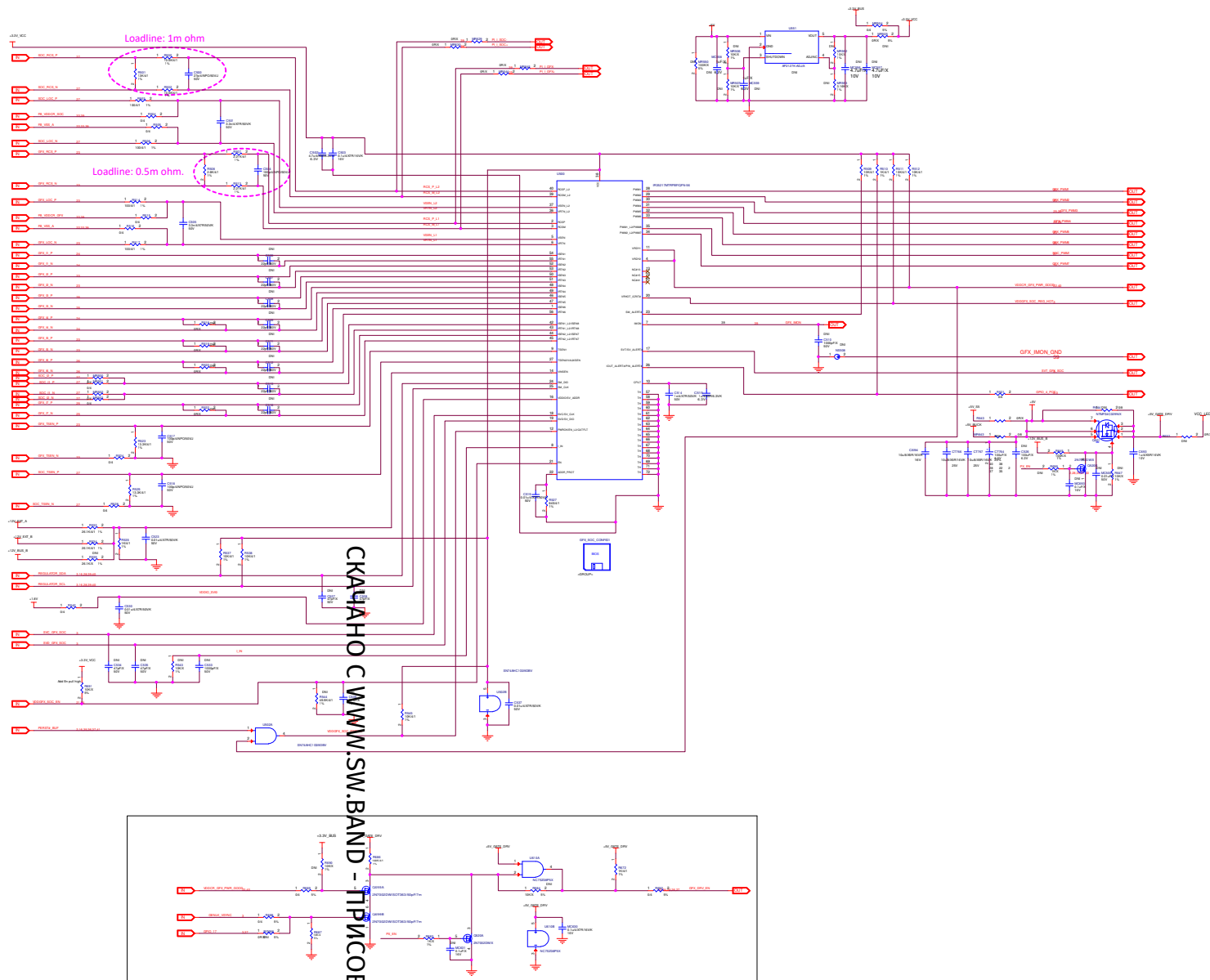
Place Q4700 and Q4701 closed to U1703



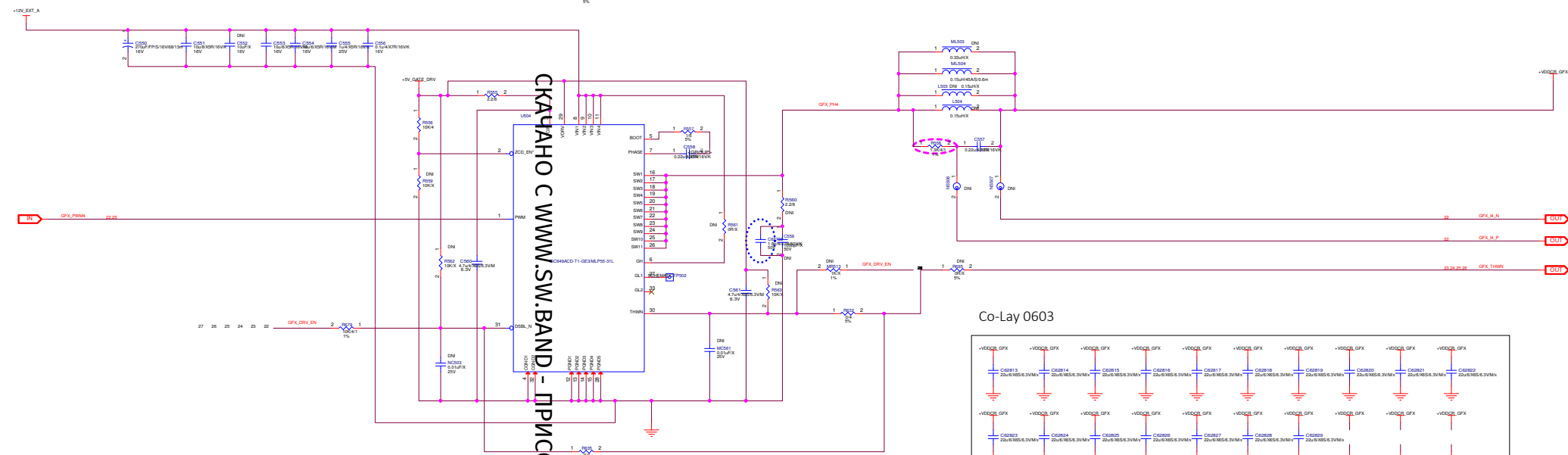
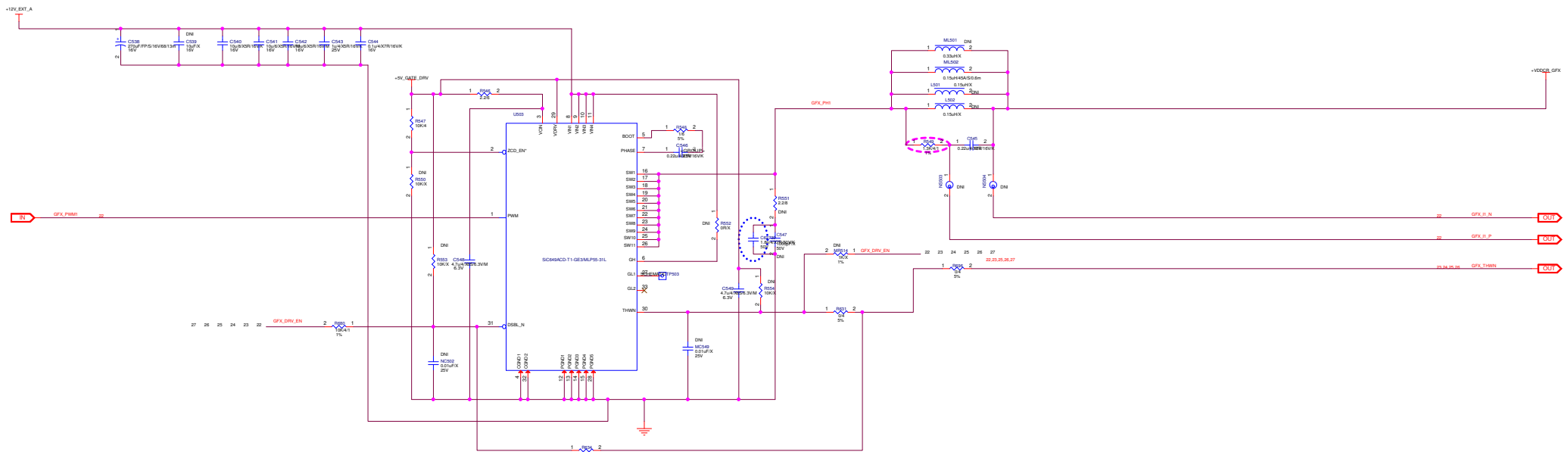




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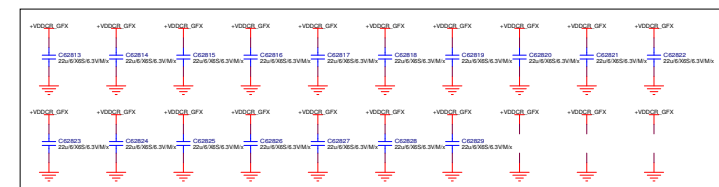






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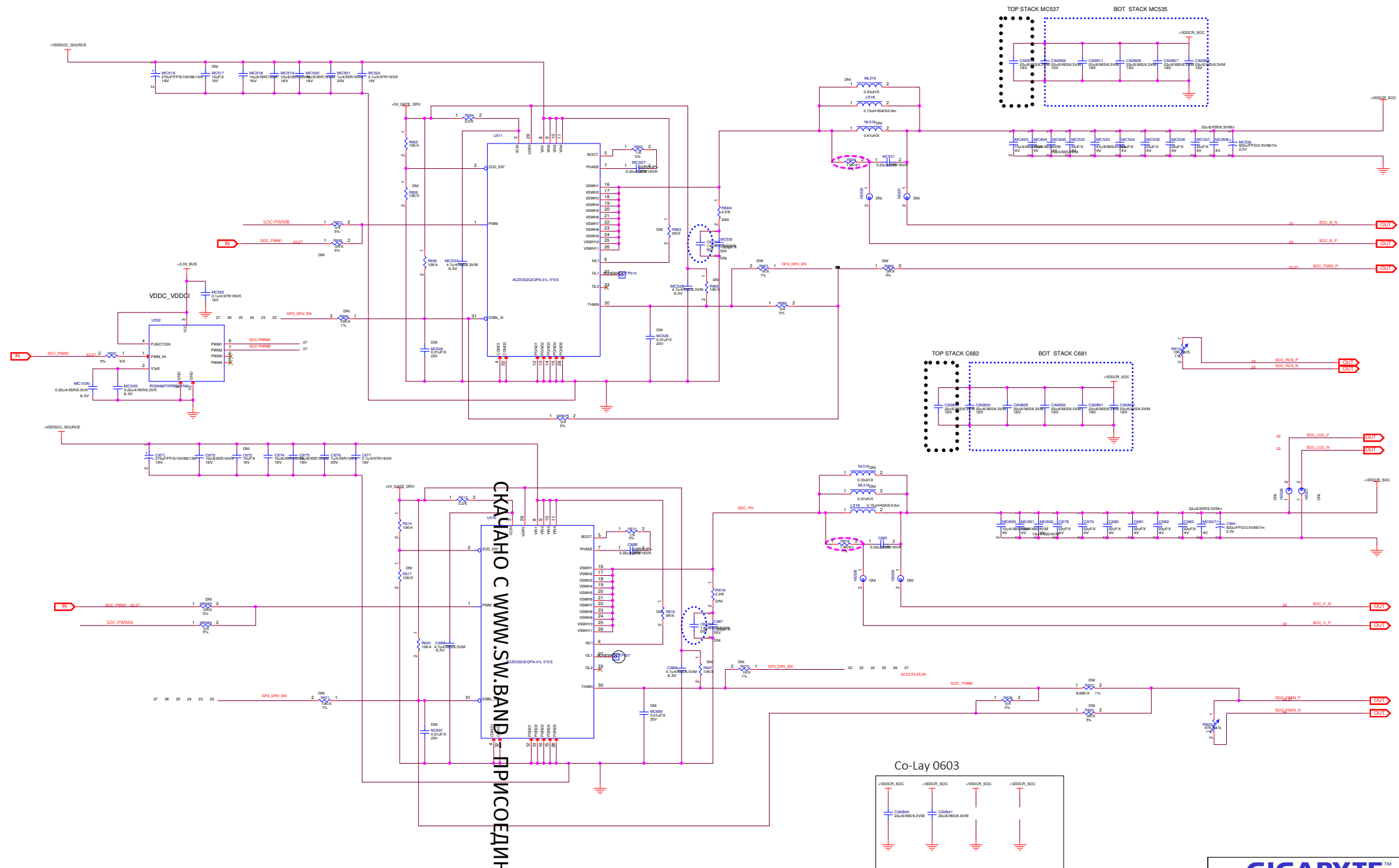
Co-Lay 0603



**GIGABYTE™**

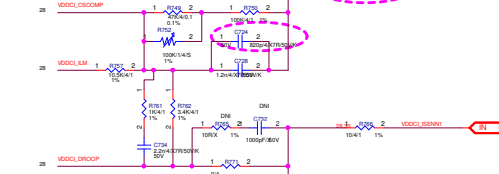
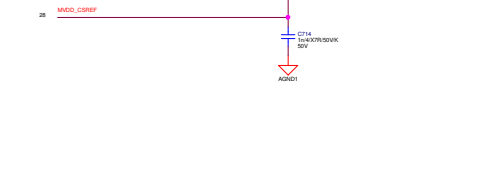
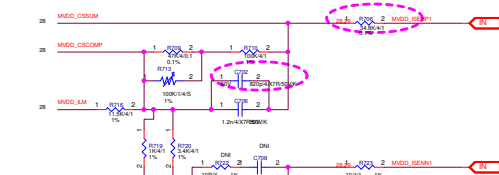
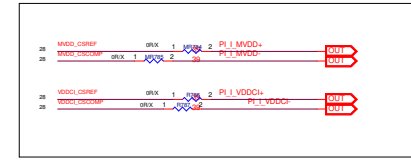
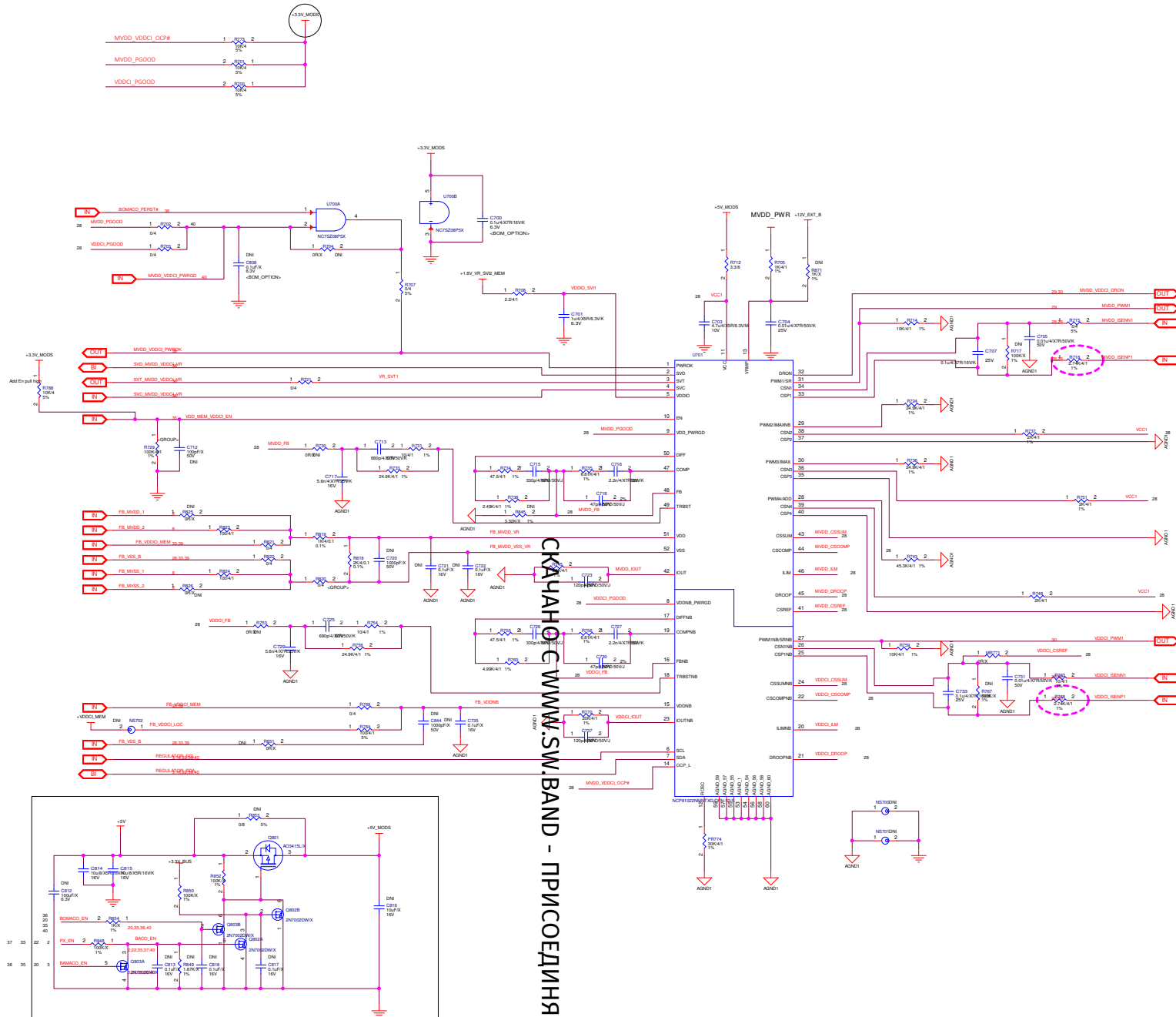




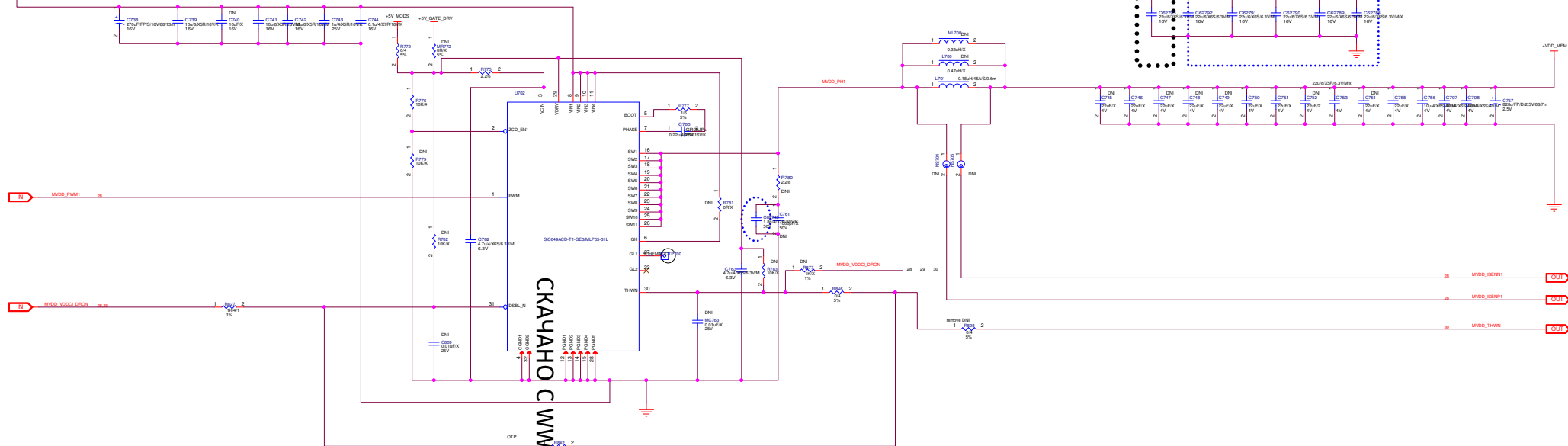


**GIGABYTE™**

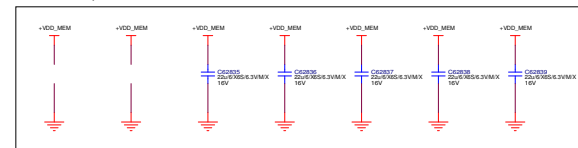
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MVDD\_PWR

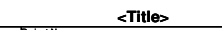
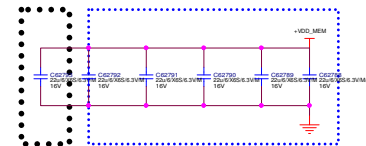


Co-Lay 0603



TOP STACK C753

BOT STACK C754

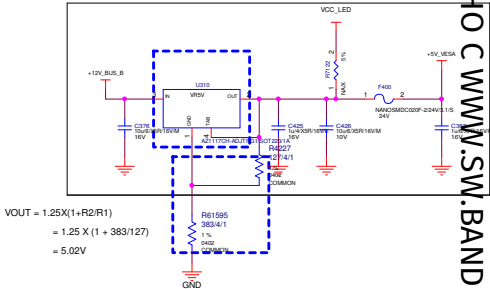
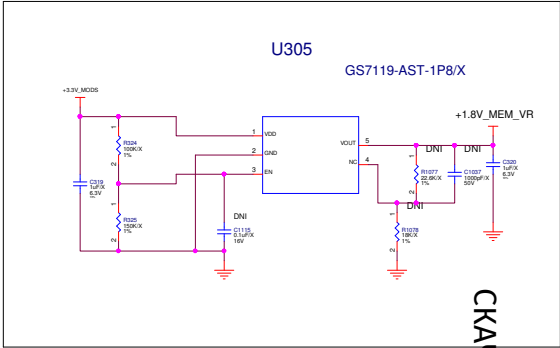


СКАЧАНО С WWW.S.W.BAND - ПРИСОЕДИНЯЙСЯ

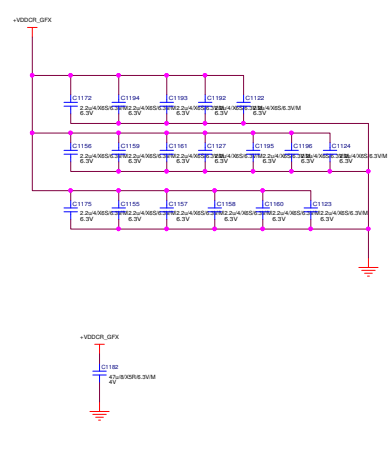
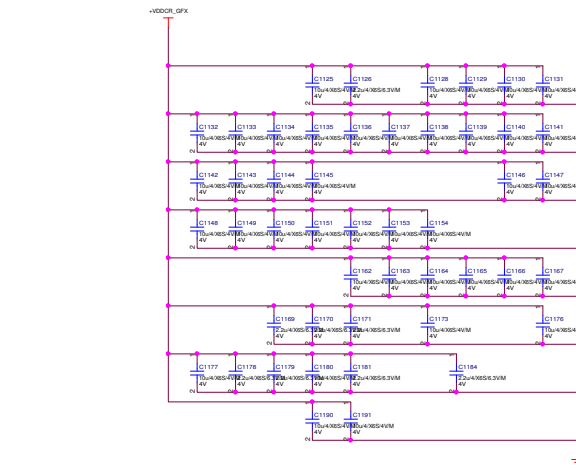
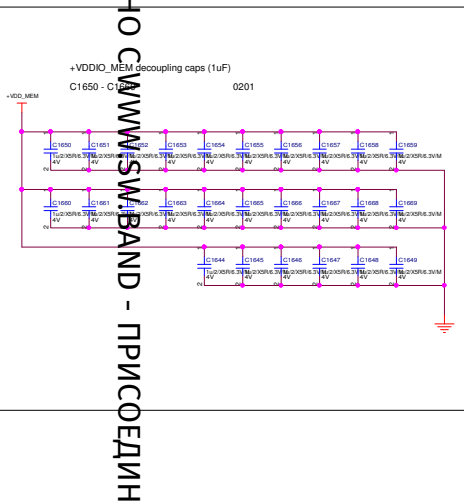
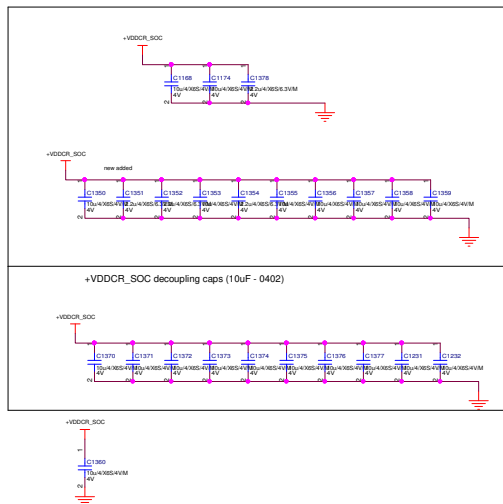
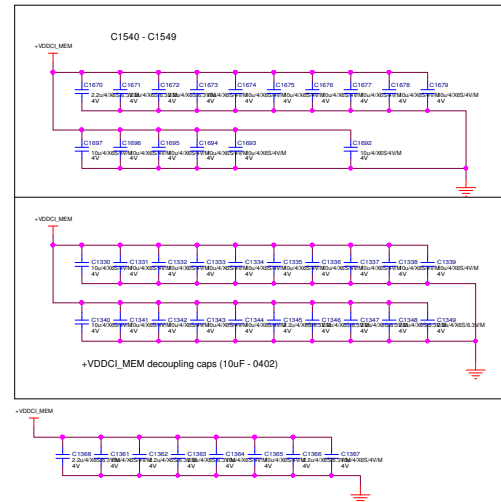
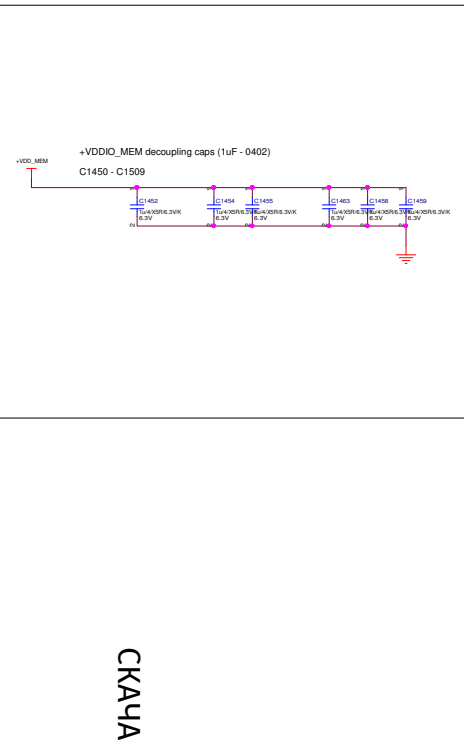
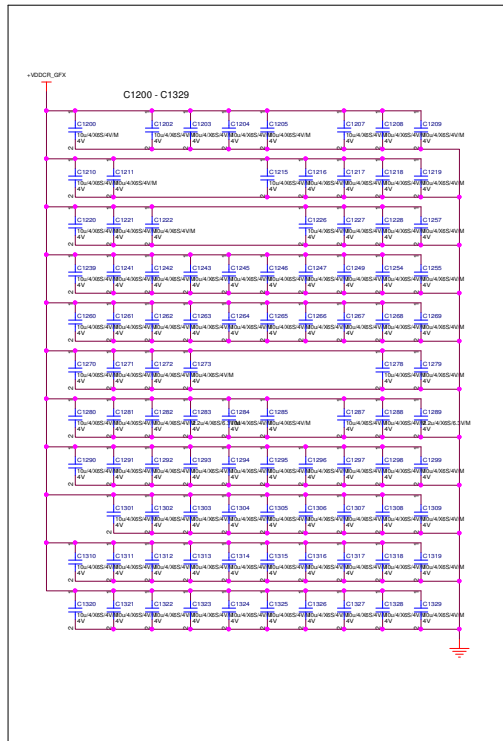
GIGABYTE™



+1.8V FOR BOMACO

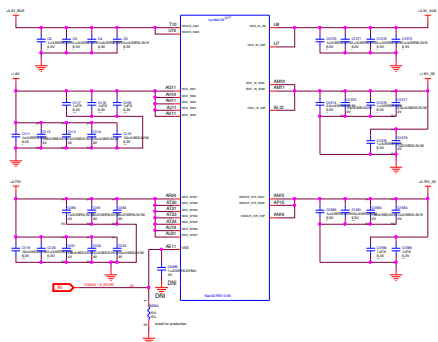
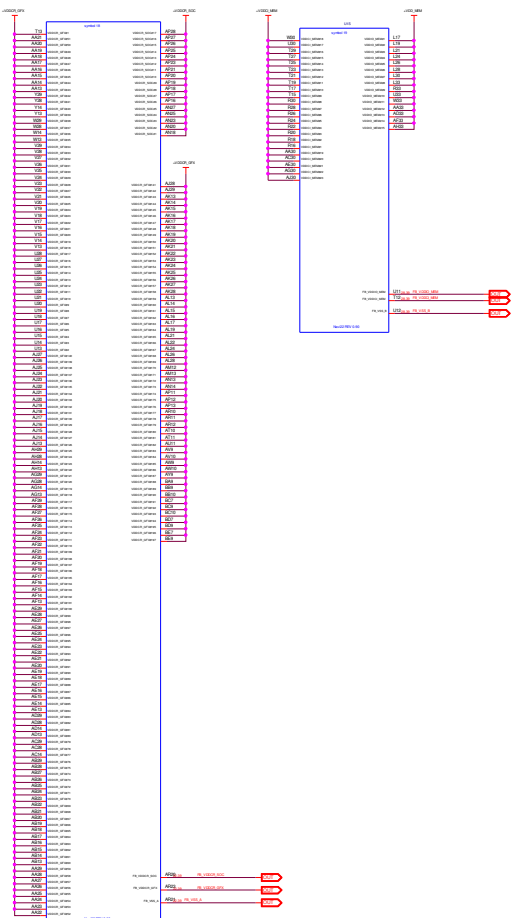


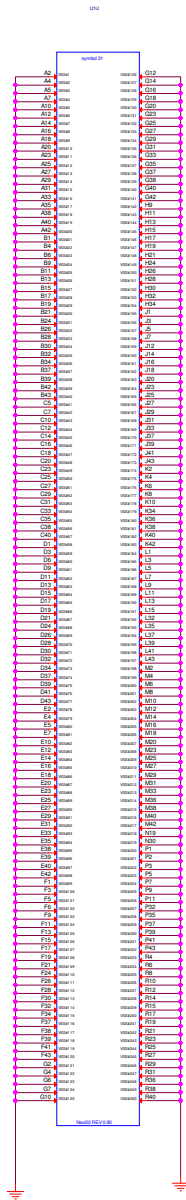
СКАЧАНО С WWW.SM.BAND - ПРИСОЕДИНЯЙСЯ



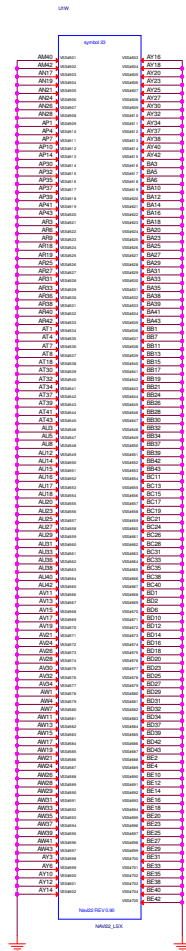
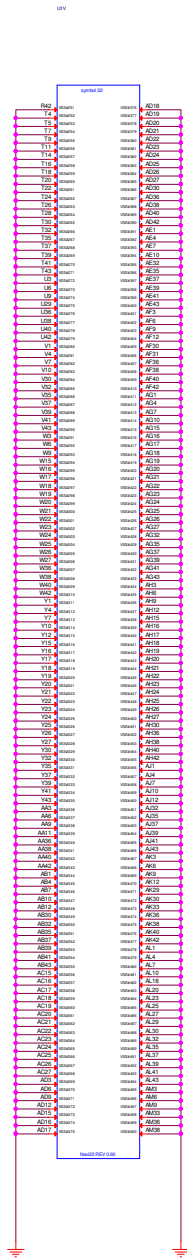
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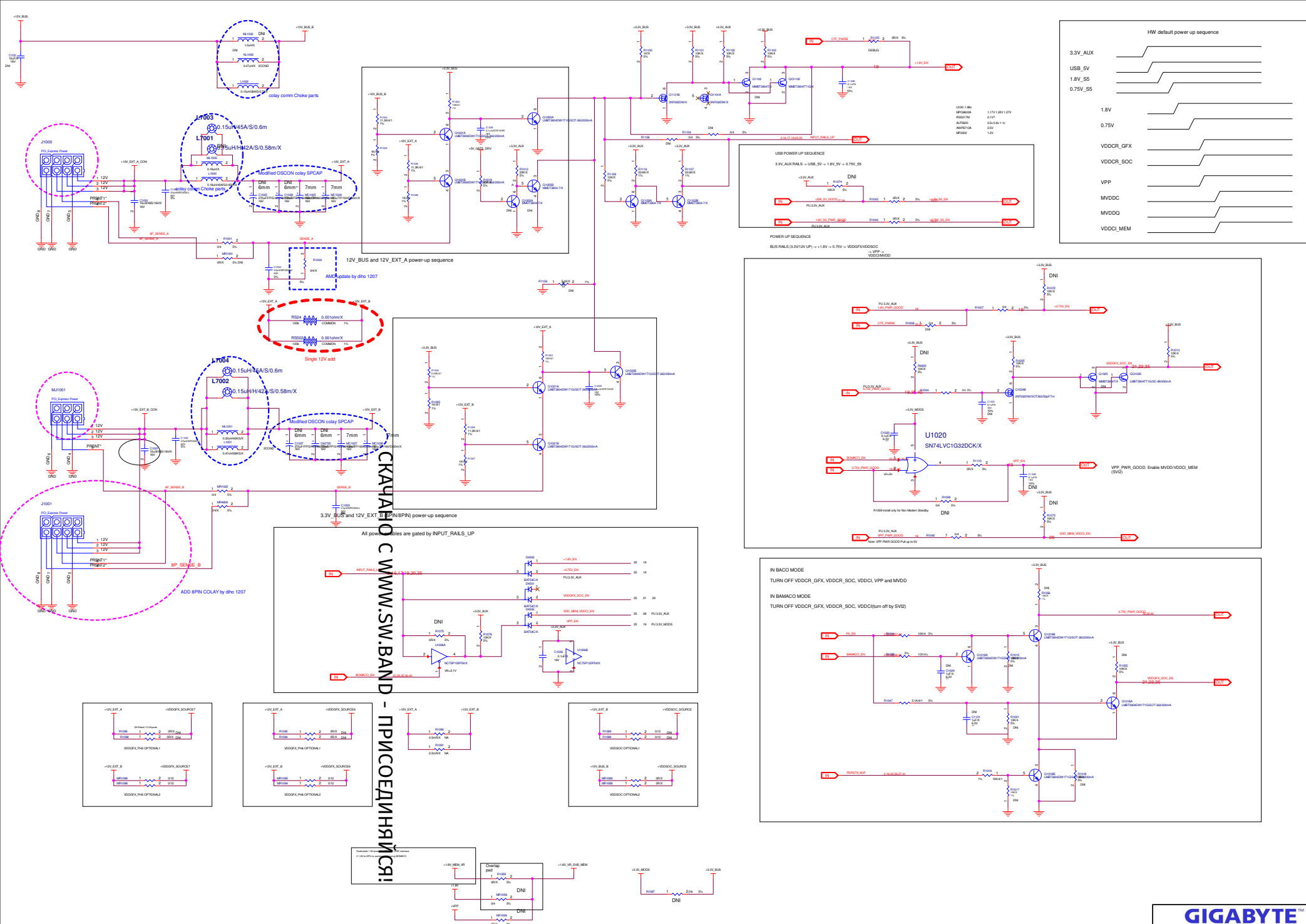
СКАЧАНО С WWW.SW.BAND - ПРИСОЕДИНЯЙСЯ!





СКАЧАНО С WWW.SW.BAND - ПРИСОЕДИНЯЙСЯ!





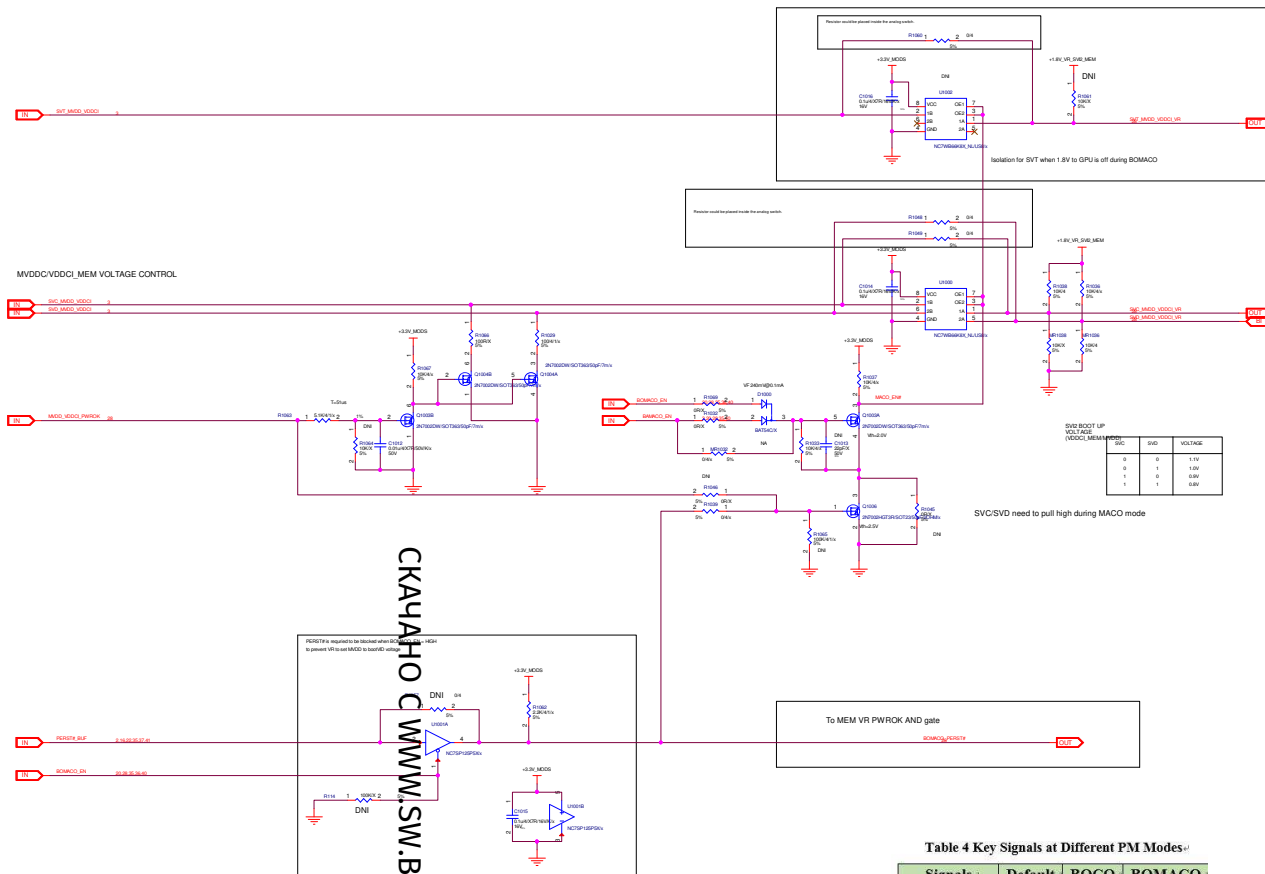


Table 4 Key Signals at Different PM Modes<sup>o</sup>

| Signals <sup>o</sup>   | Default <sup>o</sup> | BOCO <sup>o</sup>    | BOMACO <sup>o</sup>  |
|------------------------|----------------------|----------------------|----------------------|
| PX_EN <sup>o</sup>     | LOW <sup>o</sup>     | N/A <sup>o</sup>     | N/A <sup>o</sup>     |
| MACO_EN <sup>o</sup>   | N/A <sup>o</sup>     | N/A <sup>o</sup>     | N/A <sup>o</sup>     |
| PERSTb <sup>o</sup>    | HIGH <sup>o</sup>    | 1->0->1 <sup>o</sup> | 1->0->1 <sup>o</sup> |
| PWR_EN <sup>o</sup>    | HIGH <sup>o</sup>    | LOW <sup>o</sup>     | LOW <sup>o</sup>     |
| BOMACO_EN <sup>o</sup> | LOW <sup>o</sup>     | LOW <sup>o</sup>     | HIGH <sup>o</sup>    |

Table 5 Platform to Support BOMACO<sup>o</sup>

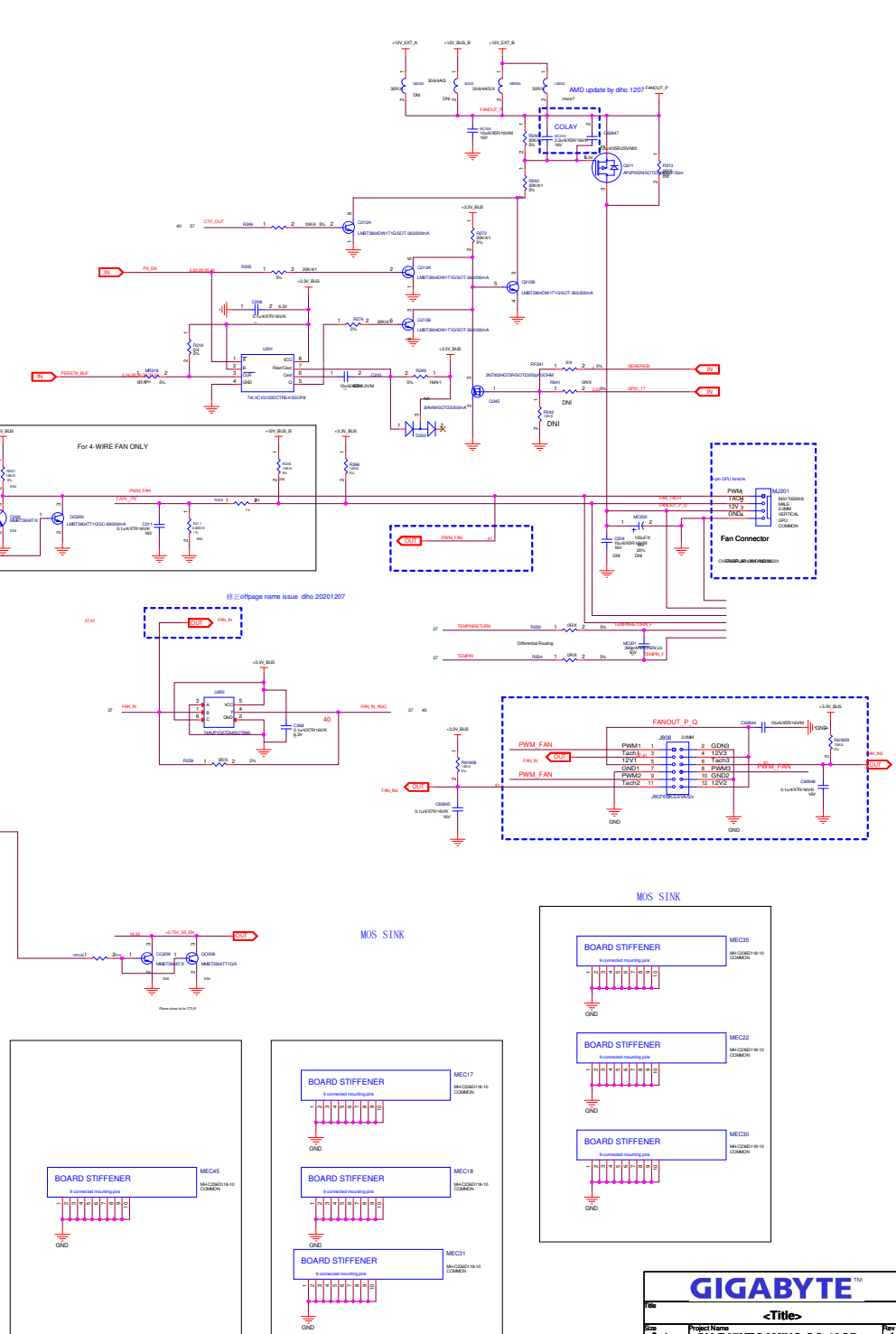
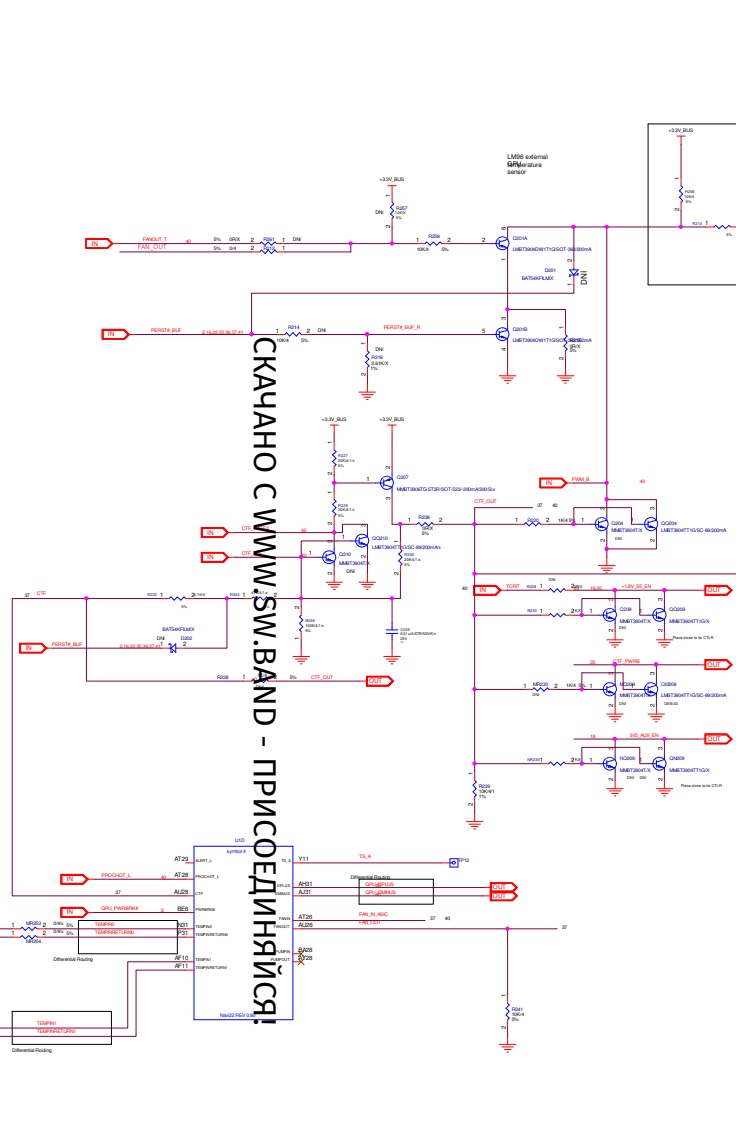
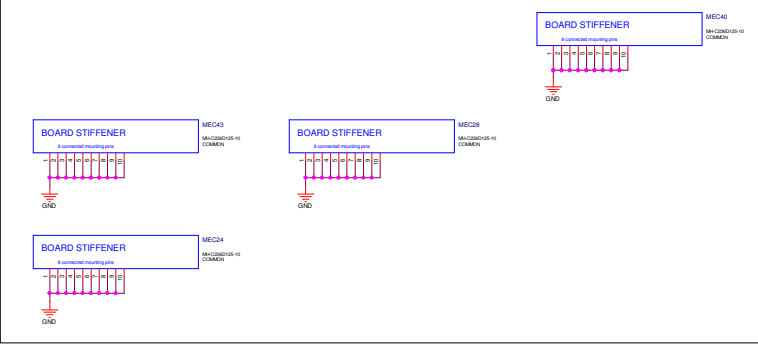
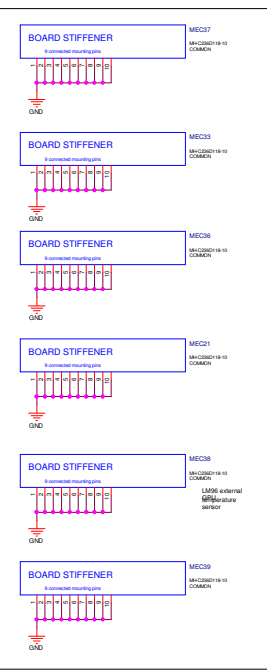
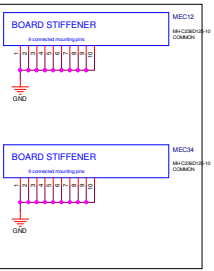
| BOMACO_EN <sup>o</sup> | SVC PU/PD <sup>o</sup> | SVD PU/PD <sup>o</sup> |
|------------------------|------------------------|------------------------|
| HIGH <sup>o</sup>      | PU <sup>o</sup>        | PU <sup>o</sup>        |
| LOW <sup>o</sup>       | bootVID <sup>o</sup>   | bootVID <sup>o</sup>   |

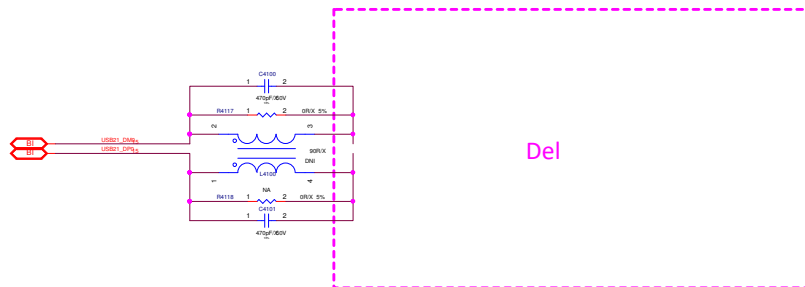
Table 3 Power Rails Status at BAMACO Mode<sup>o</sup>

| Power Rail at ASIC <sup>o</sup> | Used logic <sup>o</sup>                 | ON/OFF Status <sup>o</sup> |
|---------------------------------|-----------------------------------------|----------------------------|
| VDDCR_GFX <sup>o</sup>          | GFX IP, SDMA, GFXCLK CLKIP <sup>o</sup> | OFF <sup>o</sup>           |
| VDDCR_SOC <sup>o</sup>          | SYS IP <sup>o</sup>                     | OFF <sup>o</sup>           |
| VDDCI_MEM <sup>o</sup>          | MEM PHY <sup>o</sup>                    | OFF <sup>o</sup>           |
| VDDIO_MEM <sup>o</sup>          | MEM PHY <sup>o</sup>                    | ON <sup>o</sup>            |
| MVDDC/MVDDQ/VPP <sup>o</sup>    | DRAM <sup>o</sup>                       | ON <sup>o</sup>            |
| VDDCR_BACO <sup>o</sup>         | NBIO/THM/MP1/USB <sup>o</sup>           | ON <sup>o</sup>            |
| VDDIO_PCIE <sup>o</sup>         | PCIe PHY <sup>o</sup>                   | ON <sup>o</sup>            |
| VDDAN_C <sup>o</sup>            | PHY <sup>o</sup>                        | ON <sup>o</sup>            |
| VDDAN_18 <sup>o</sup>           | PLL, PHY, etc <sup>o</sup>              | ON <sup>o</sup>            |
| VDDIO_18 <sup>o</sup>           | 1.8V GPIO, I2C, etc <sup>o</sup>        | ON <sup>o</sup>            |
| VDDIO_33 <sup>o</sup>           | 3.3V GPIO <sup>o</sup>                  | ON <sup>o</sup>            |
| VDDAN_* EFUSE <sup>o</sup>      | EFUSE <sup>o</sup>                      | ON <sup>o</sup>            |
| VDDCR_S5* <sup>o</sup>          | USB <sup>o</sup>                        | ON <sup>o</sup>            |

Table 3 Power Rails Status at BOMACO Mode<sup>o</sup>

| Power Rail at ASIC <sup>o</sup> | Used logic <sup>o</sup>                 | ON/OFF Status for BOMACO-A <sup>o</sup> |
|---------------------------------|-----------------------------------------|-----------------------------------------|
| VDDCR_GFX <sup>o</sup>          | GFX IP, SDMA, GFXCLK CLKIP <sup>o</sup> | OFF <sup>o</sup>                        |
| VDDCR_SOC <sup>o</sup>          | SYS IP <sup>o</sup>                     | OFF <sup>o</sup>                        |
| VDDCI_MEM <sup>o</sup>          | MEM PHY <sup>o</sup>                    | OFF <sup>o</sup>                        |
| VDDIO_MEM <sup>o</sup>          | MEM PHY <sup>o</sup>                    | ON <sup>o</sup>                         |
| MVDDC/MVDDQ/VPP <sup>o</sup>    | DRAM <sup>o</sup>                       | ON <sup>o</sup>                         |
| VDDCR_BACO <sup>o</sup>         | NBIO/THM/MP1/USB <sup>o</sup>           | OFF <sup>o</sup>                        |
| VDDIO_PCIE <sup>o</sup>         | PCIe PHY <sup>o</sup>                   | OFF <sup>o</sup>                        |
| VDDAN_C <sup>o</sup>            | PHY <sup>o</sup>                        | OFF <sup>o</sup>                        |
| VDDAN_18 <sup>o</sup>           | PLL, PHY, etc <sup>o</sup>              | OFF <sup>o</sup>                        |
| VDDIO_18 <sup>o</sup>           | 1.8V GPIO, I2C, etc <sup>o</sup>        | OFF <sup>o</sup>                        |
| VDDIO_33 <sup>o</sup>           | 3.3V GPIO <sup>o</sup>                  | OFF <sup>o</sup>                        |
| VDDAN_* EFUSE <sup>o</sup>      | EFUSE <sup>o</sup>                      | OFF <sup>o</sup>                        |
| VDDCR_S5* <sup>o</sup>          | USB <sup>o</sup>                        | ON <sup>o</sup>                         |



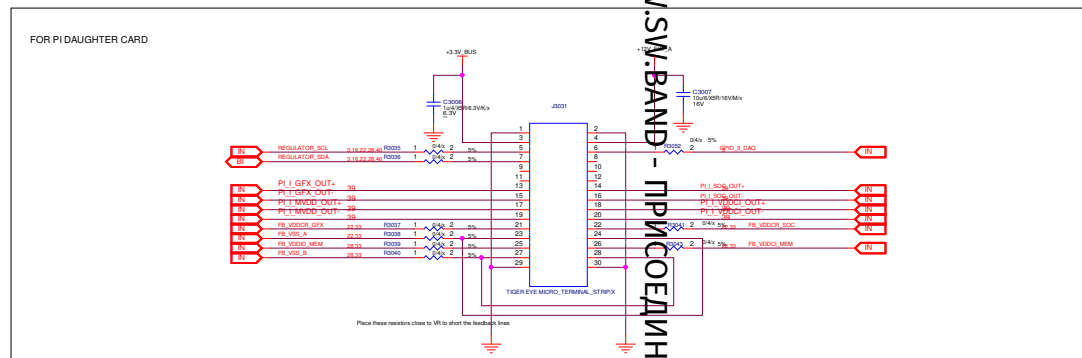
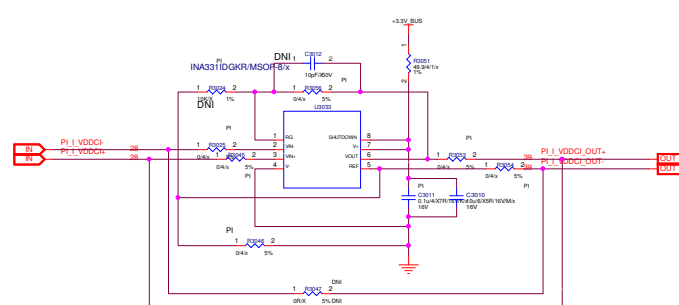
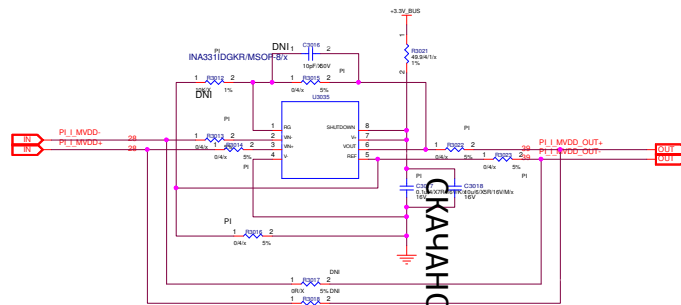
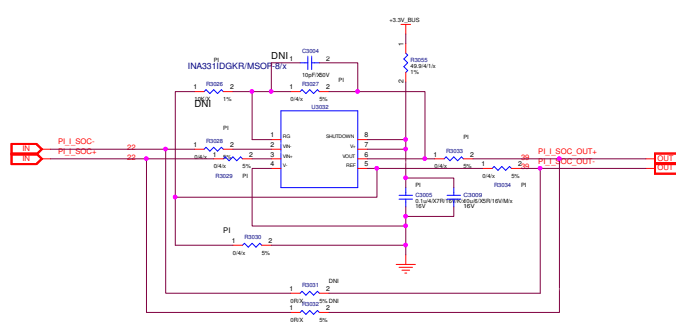
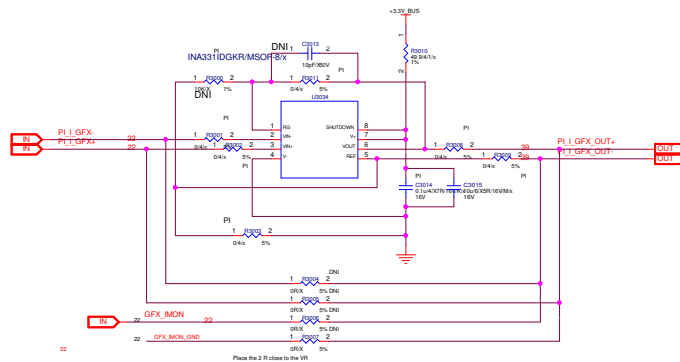


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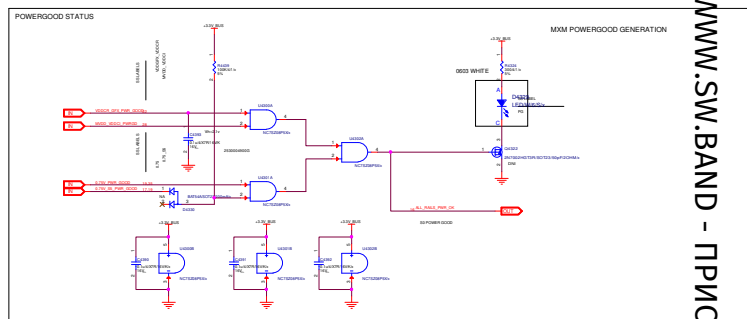
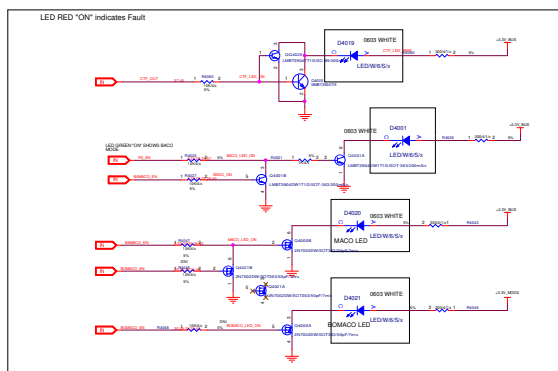
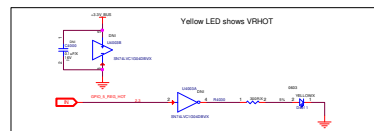
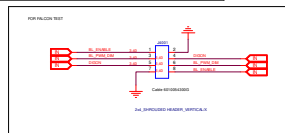
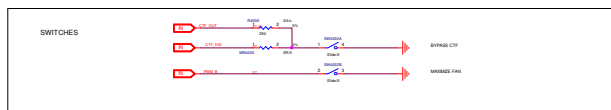
RADEON Lightbar header

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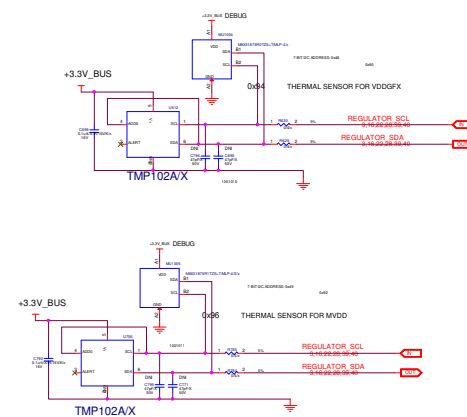
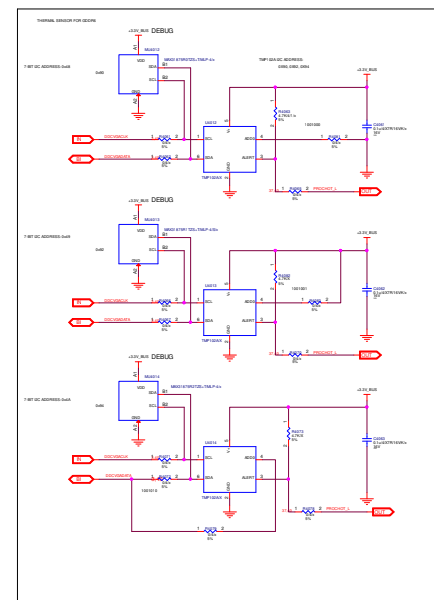
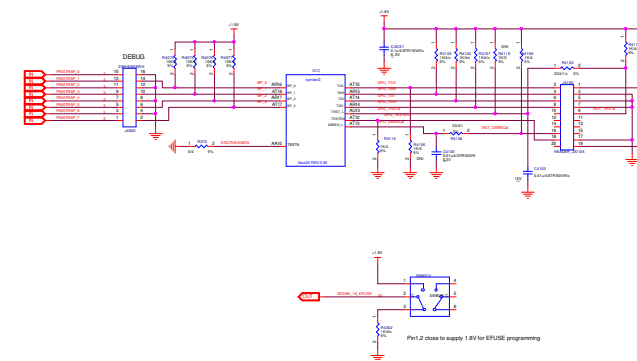
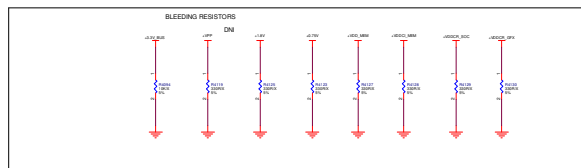
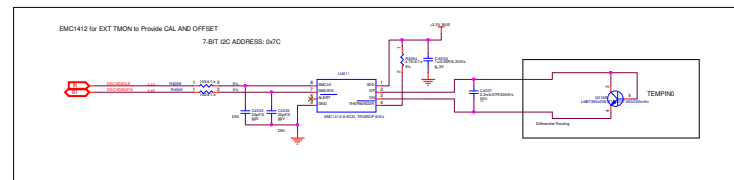
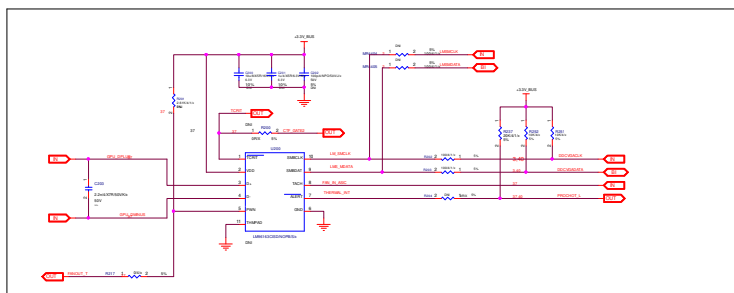
СКАЧАНО С WWW.S.W.BAND - ПРИСОЕДИНЯЙСЯ



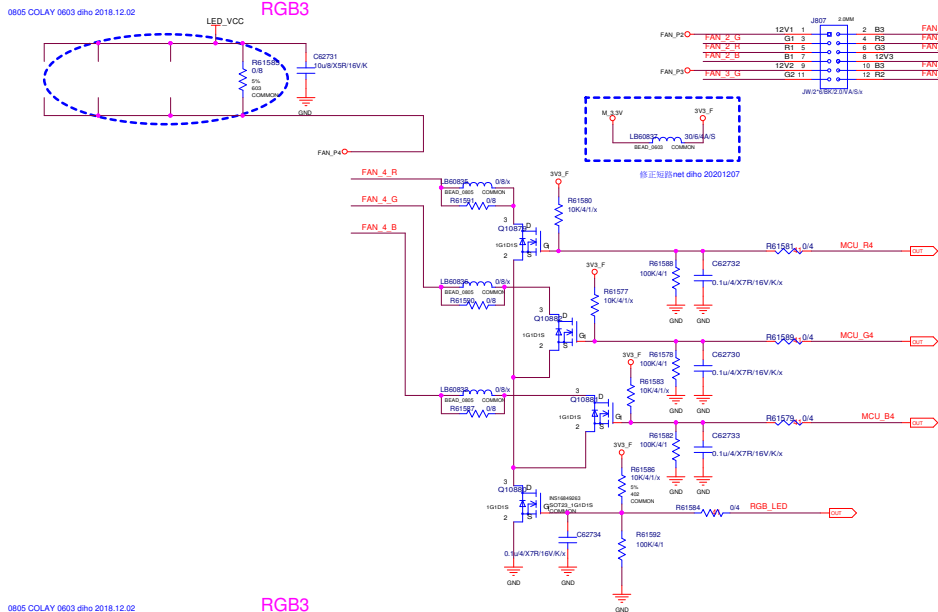
СКАЧАНО С WWW.S.W.BAND - ПРИСОЕДИНЯЙСЯ



СКАЧАНО С WWW.SW.BAND - ПРИСОЕДИНЯЙСЯ





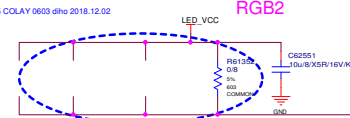


Modified GV-N3060GAMING OC-8GD



RGB1

0805 COLAY 0603 dtho 2018.12.02



0805 COLAY 0603 dtho 2018.12.02

