3/2/1-Phase Synchronous-Rectified Buck Controller for GPU Power Supply

General Description

The uP9529Q is a 3/2/1-phase PWM controller specifically designed to work with 3V ~ 20V input voltage and deliver high quality output voltage for high performance graphic processor power.

The uP9529Q adopts proprietary RCOT™ technology, providing flexible selection of output LC filter and excellent load transient response. The uP9529Q supports NVIDIA Open Voltage Regulator type 3i+ with PWMVID interface. The PWMVID input is buffered and filtered to generate accurate reference voltage and the output voltage is precisely regulated to the reference input.

The uP9529Q is capable of supporting two types of applications, the advanced DrMOS power module with current reporting function, and the inductor DCR current sensing application. The integrated power saving input (PSI) allows for graphic processors to control the operating phase number to obtain high efficiency in light load condition. Other features include adjustable switching frequency, adjustable soft-start time, channel current limit, under voltage protection, over voltage protection and power good indication. The uP9529Q is available in a WQFN3x3-20L package.

Ordering Information

Order Number	Package	Top Marking
uP9529QQKF	WQFN3x3 - 20L	uP9529Q

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

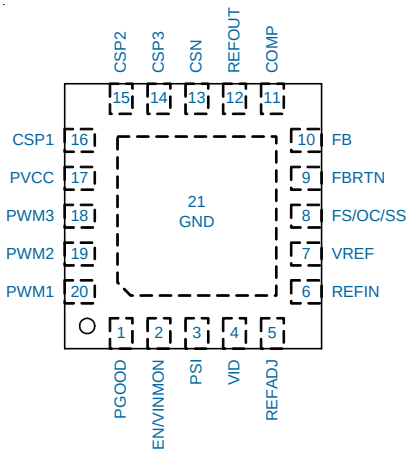
Features

- **Support NVIDIA's Open VReg Type 3i+ with PWMVID Interface**
- **Selectable 3/2/1-Phase Operation by Hardware Setting**
- **Support Up to 1.2MHz Operation Frequency**
- **REFOUT Reference Voltage for Advanced DrMOS Power Module with Current Reporting Function (DrMOS)**
- **Support Inductor DCR Current Sensing Application**
- **Selectable 2-Level Soft-Start Time**
- **Power Saving Input (PSI)**
- **Power Good Indication**
- **Channel Current Limit Protection**
- **Over/Under Voltage Protection**
- **Over Temperature Protection**
- **RoHS Compliant and Halogen Free**

Applications

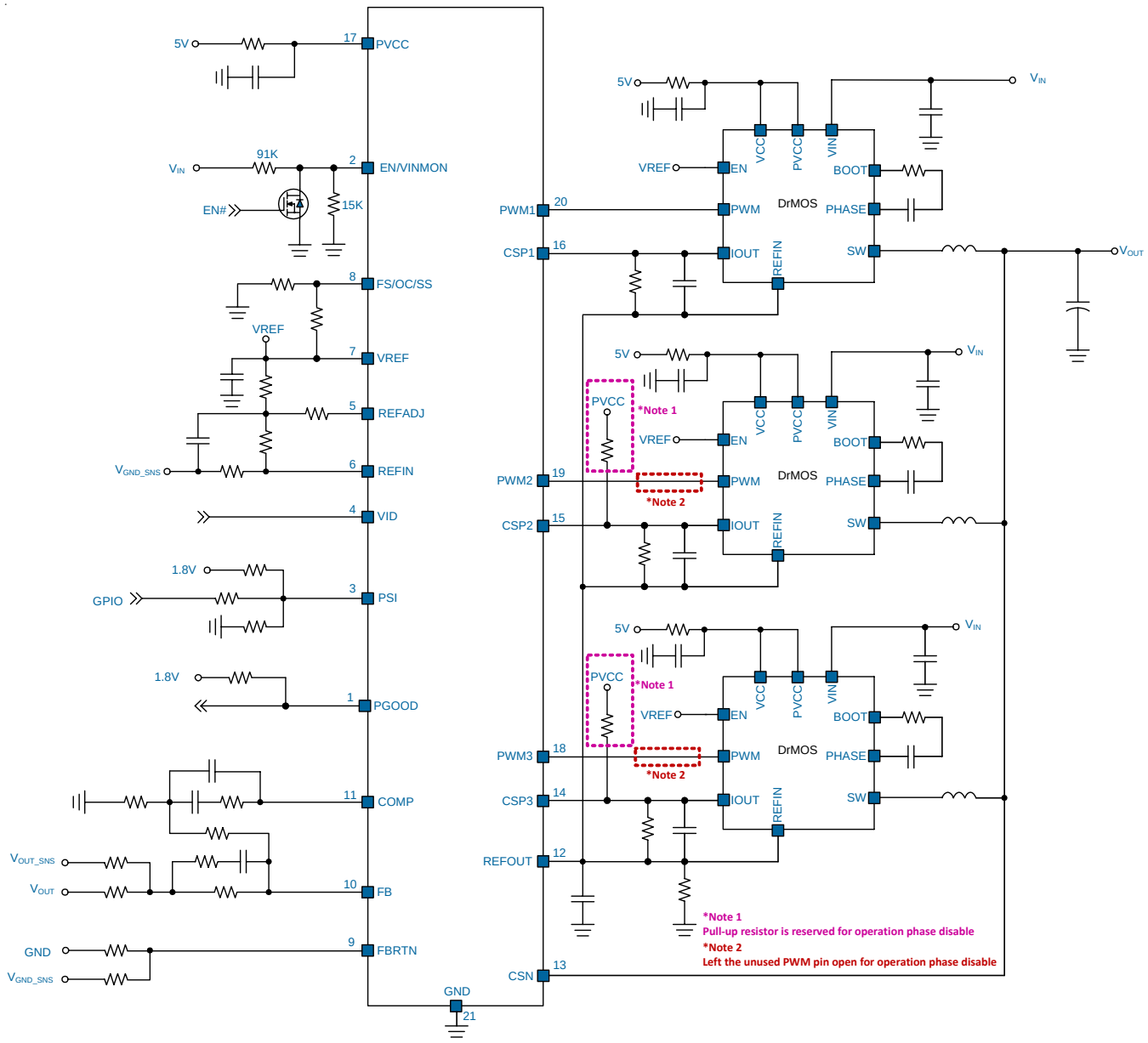
- **Middle-High End GPU Core Power Supplies**

Pin Configuration



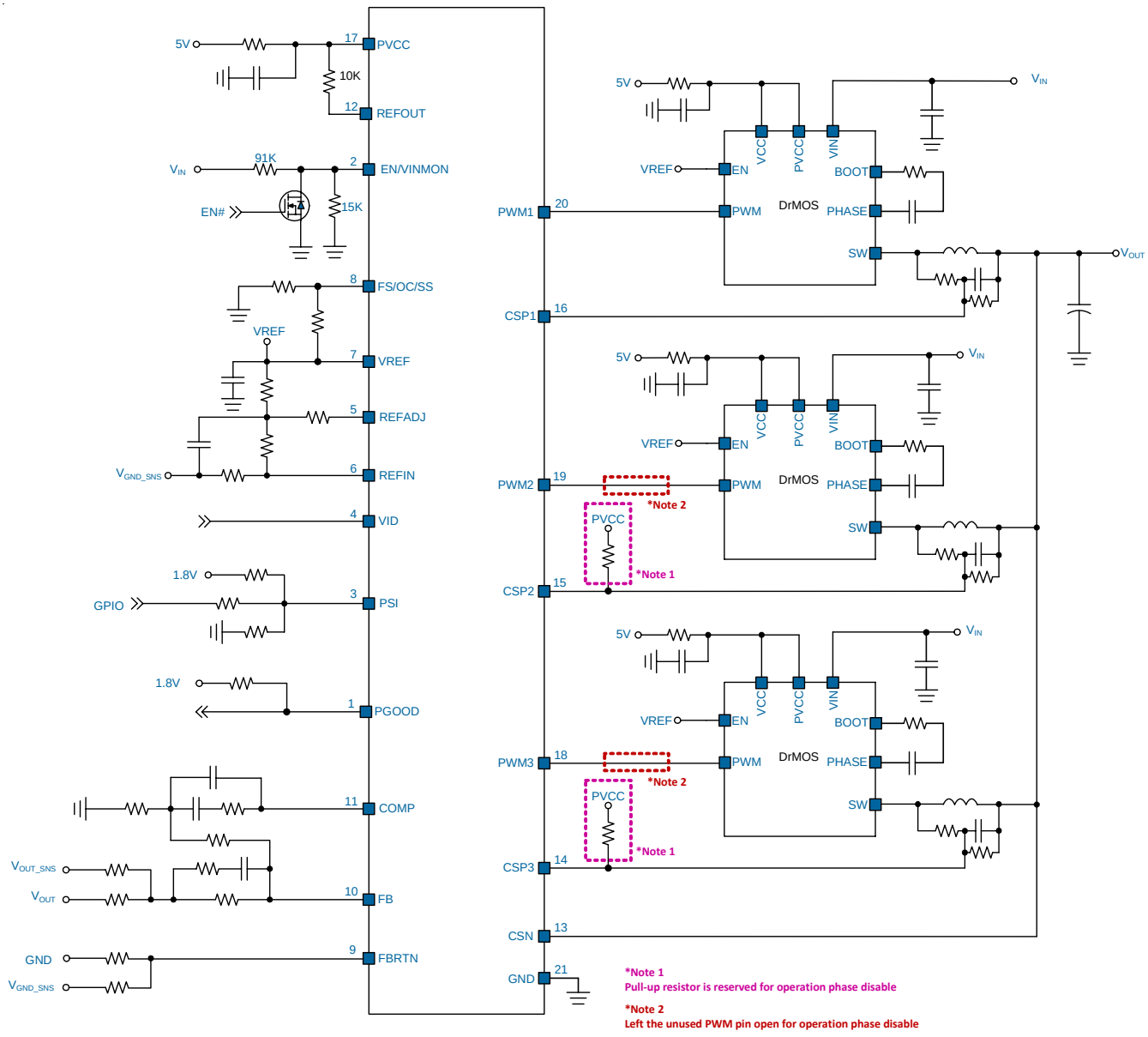
Typical Application Circuit

For Advanced DrMOS Power Module with Current Reporting Function



Typical Application Circuit

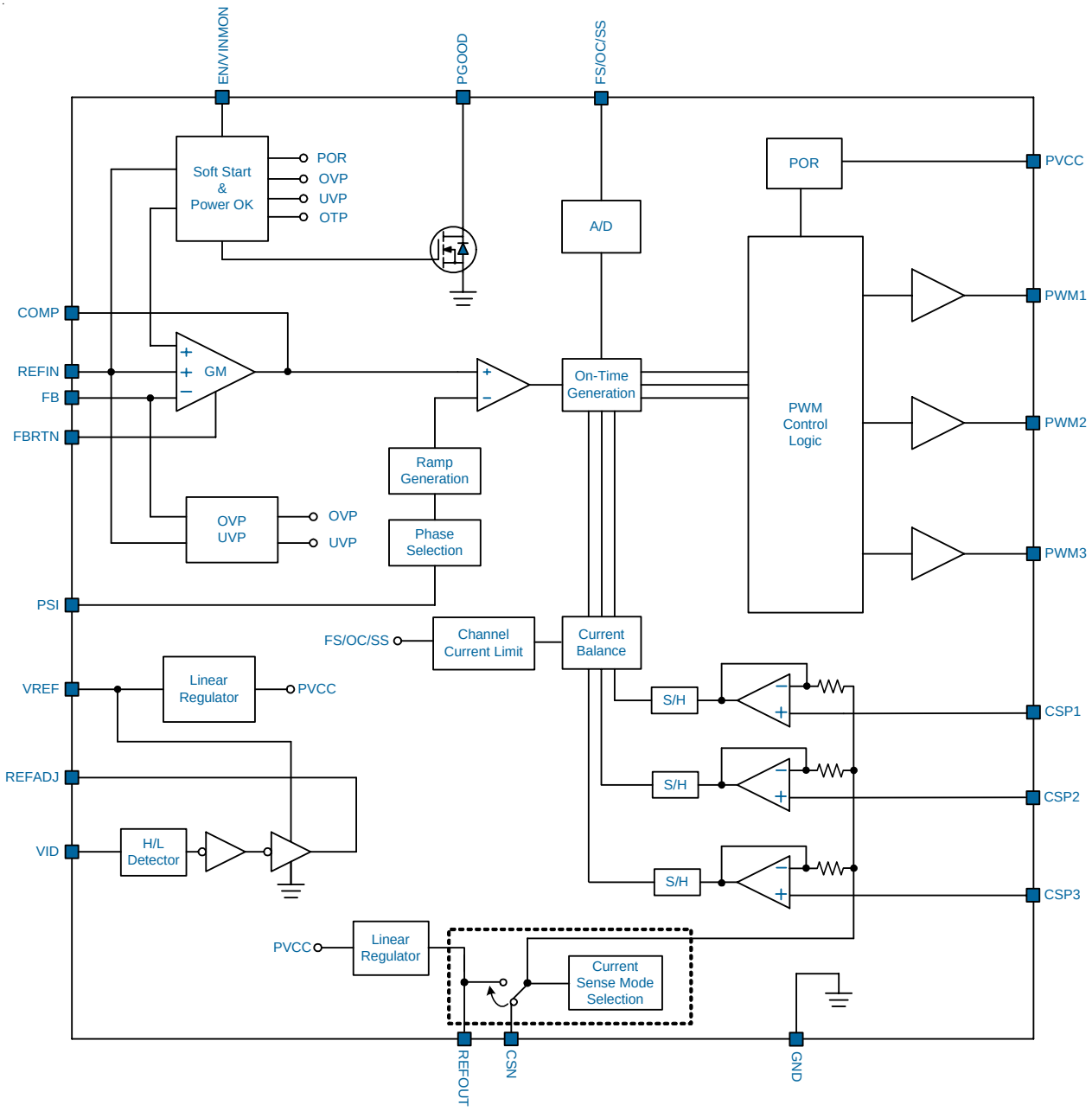
For Inductor DCR Current Sense Application



Functional Pin Description

No.	Name	Pin Function
1	PGOOD	**Power Good Indication.** This pin is an open drain structure and it is active high. Pull this pin up through a proper resistor to a voltage source.
2	EN/VINMON	**Enable Control and Power Stage Input Voltage Monitor.** Connect this pin to the power stage input V_{IN} with a voltage divider. The controller senses the voltage on this pin for power stage input voltage V_{IN} detection and enable the controller. It is recommended to use a resistor divider with 1/7 dividing ratio from V_{IN}. For example, use a 91kΩ / 15 kΩ resistor divider is a good practice. Refer to the typical application circuit, it is recommended to use a MOSFET with its drain connected to EN/VINMON pin without a pull-up resistor for power sequence control. **Do NOT** connect EN/VINMON pin directly to a voltage source for sequence control.
3	PSI	**Power Saving Input.** An input pin receiving power saving control signal from GPU. PSI input voltage determines the controller operating mode. Do not leave this pin open.
4	VID	**VID.** PWMVID input pin.
5	REFADJ	**Reference Adjustment.** PWMVID output pin. Connect this pin with an RC integrator to generate REFIN voltage.
6	REFIN	**Reference Input.** Connect this pin to an external reference voltage through a resistor or connect to the output of the REFADJ circuit.
7	VREF	**Reference Voltage.** 2V LDO voltage output pin. Connect an at least 1 uF decoupling capacitor between this pin and GND. This pin is also used to enable/disable DrMOS (or MOSFET driver) for power sequence control.
8	FS/OC/SS	**Function Setting Pin.** Connect this pin to the VREF pin with a resistor voltage divider to set switching frequency, channel current limit threshold and soft-start time.
9	FBRTN	**Output Voltage Feedback Return.** Inverting input to the differential voltage sense amplifier. Connect this pin directly to the GPU output voltage feedback return sense point.
10	FB	**Feedback Pin.** This pin is the inverting input of the error amplifier.
11	COMP	**Compensation Output.** This pin is the output of the error amplifier. Connect an RC network from this pin to GND to compensate the voltage control loop.
12	REFOUT	**Reference Output Voltage.** This pin provides a reference voltage for DrMOS. Connect this pin to the REFIN pin of DrMOS. Depends on application, a resistor from this pin to GND is allowed to help sink the current from DrMOS. When this pin is pulled up to PVCC via a resistor 10kΩ, the controller operate in DCR current sensing mode.
13	CSN	**Inverting Input of Total Current Sense Amplifier.**
14	CSP3	**Positive Differential Current Sense Input for Phase 3.**
15	CSP2	**Positive Differential Current Sense Input for Phase 2.**
16	CSP1	**Positive Differential Current Sense Input for Phase 1.**
17	PVCC	**Supply Input for the IC.** Connect this pin to a 5V voltage source with an RC filter. Connect this pin to a 5V supply and decouple with a ceramic capacitor of 1uF minimum.
18	PWM3	**Phase 3 PWM Output.** It outputs a PWM logic signal for external MOSFET driver.
19	PWM2	**Phase 2 PWM Output.** It outputs a PWM logic signal for external MOSFET driver.
20	PWM1	**Phase 1 PWM Output.** It outputs a PWM logic signal for external MOSFET driver.
Exposed Pad		**Ground.** The exposed pad is the ground of logic control circuits, it must be soldered to a large PCB and connected to GND.

Functional Block Diagram



Power Input and Power On Reset

The uP9529Q receives supply input from PVCC pin to provide current to internal control circuit. PVCC pin is continuously monitored for power on reset. The POR level is typical 4.1V at its rising edge. Figure 1. shows the power ready detection circuit. When PVCC is ready, the controller waits for EN/VINMON to start up. When EN/VINMON pin is driven above 0.4V, the controller begins its start up sequence. When EN/VINMON pin is driven below 0.1V, the controller will be turned off, and it will clear all fault states to prepare for next soft-start once the controller is re-enabled.

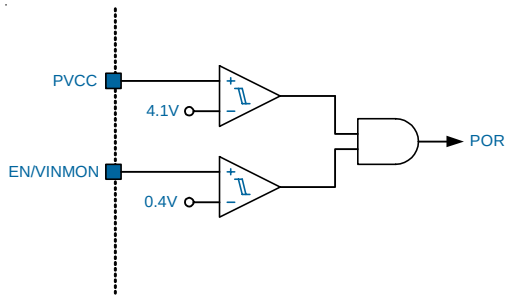


Figure 1. Circuit of Power Ready Detection

Power Input Monitor

EN/VINMON is the power stage input voltage sense pin and is used for on-time calculation. Connect this pin to power stage input voltage (V_{IN}) with a voltage divider and always keep EN/VINMON as 1/7 of power stage input voltage.

Enable Control

The EN/VINMON pin is also used to control the enable and disable state of this device. It is recommended to use a small MOSFET with its drain connected to EN/VINMON pin without pull up resistor for power sequence control as shown in Figure 2. Do NOT connect EN/VINMON pin directly to any sequencing circuit of the system. Make sure the slew rate of the gate signal (EN#) of Q1 is fast and not affected by any additional circuit.

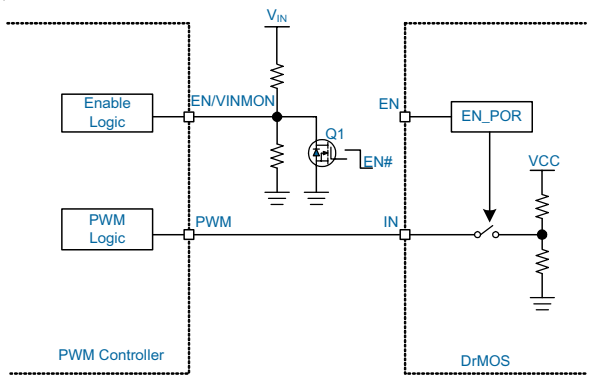


Figure 2. Enable Sequence Control

Power Up Sequence and Power Good

A built-in soft-start function is used to prevent surge current from power supply input during power on. Controller starts the soft-start process right on EN/VINMON pin enable. The following graph shows the soft-start sequence of the uP9529Q.

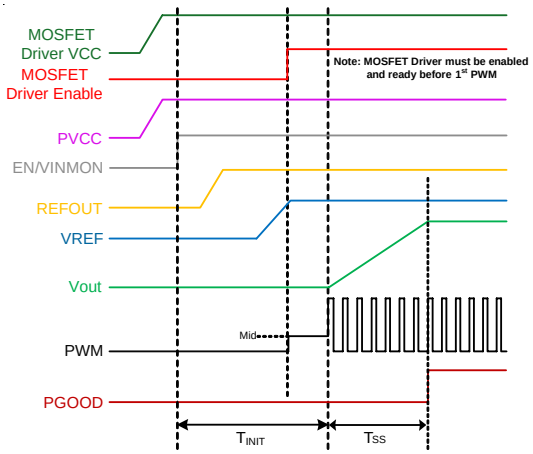


Figure 3. Power Up Sequence

Soft Start Time and Switching Frequency Setting

Figure 4 shows the FS/OC/SS pin connection for soft start time setting, operation frequency selection and per phase over current limit (OCL) threshold setting. After PVCC POR, switch S1 and S2 are turned on. An internal current source I_{source}=4uA flows out to FS/OC/SS pin to generate a voltage V_{FS1}. Then, S2 switch turns off, the FS/OC/SS pin voltage V_{FS2} is determined by the external voltage divider. Controller samples/holds the V_{FS1} and V_{FS2} to calculate the V_{FS} (V_{FS1}-V_{FS2})and determine the controller operation frequency and ramp up time according to the following Table 1.

Table 1. Switching Frequency and Soft-Start Time Selection

V_{FS} (mV)	F_{SW} (kHz)	Ramp Up Time (T_ramp) (us)
60	300	150
120	300	600
180	600	150
260	600	600
380	1200	150
480	1200	600

Functional Description

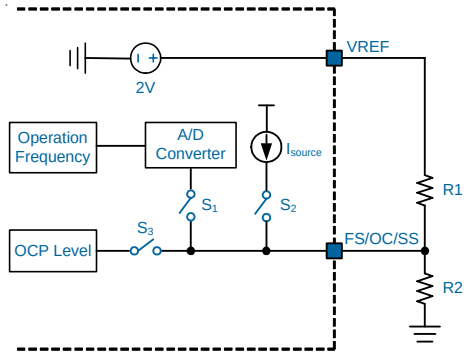


Figure 4. FS/OC/SS Pin for Operation Frequency Selection, Soft Start Time Setting and OCL Threshold Setting

Current Sense Mode Selection

uP9529Q support two current sense modes to maximize the flexibility of applications. One is the current reporting function mode (when applying advanced power module with current reporting function, DrMOS) (IMON mode), and the other is continuous inductor DCR current sensing mode (DCR mode). When REFOUT pin is pulled up to PVCC via a resistor 10kΩ, the controller operate in DCR current sensing mode.

Per Phase Over Current Limit (OCL)

The operation frequency, soft start time and OC level setting are related to the resistance of R1 and R2 as shown in Figure 4. After the operation frequency and soft start time are determined, the S1 and S2 switches are turned off, and switch S3 turns on for OCL setting. When S3 is turned on, the FS/OC/SS pin voltage is determined by the external voltage divider, and the FS/OC/SS pin voltage is connected to the internal OCL circuit for OCL level V_{FSOC} setting. The V_{FSOC} setting range is 600mV~1320mV.

Since uP9529Q supports two different current sense modes, the OCL setting for each mode is described as the following.

ΔV_{CSPx} is the per phase current information from DrMOS in the form of voltage (CSPx to REFOUT) and will limit the phase **valley current** when the controller is operated in **IMON mode**.

When per-phase:

$$V_{FSOC} = 1400mV - \frac{96}{119} \times \Delta V_{CSPx}$$

ΔV_{CSPx} is the differential voltage between CSPx and CSN (V_{OUT}) and will limit the phase **peak current** when the controller is operated in **DCR mode**.

When per-phase:

$$V_{FSOC} = 1400mV - \frac{48}{7} \times \Delta V_{CSPx}$$

Therefore, the proper resistance of R1 and R2 is needed. The following are the equations to calculate the value of R1 and R2.

$$R_1 = \frac{V_{FS} \times V_{VREF}}{I_{source} \times V_{FSOC}}$$

$$R_2 = \frac{V_{FS} \times V_{VREF}}{I_{source} \times (V_{VREF} - V_{FSOC})}$$

Phase Number of Operation (Hardware Setting)

The uP9529Q supports 3/2/1 phase operation. The maximum phase number of operation is determined by checking the CSP2 and CSP3 status when POR. Connect CSP3 pin to PVCC with 100kΩ and left PWM3 floating for maximum 2-phase operation. Connect CSP2 and CSP3 pin to PVCC with 100kΩ resistor, and left PWM3 and PWM2 floating for maximum 1-phase operation. When configured to 1-phase operation, the components of PHASE2/PHASE3 can be unstuffed. Once selected, the maximum phase number of operation is latched and can only be changed at the next POR.

Table 2. Operation Phase Number Setting

Config.	Pin Connection					
	PWM1	PWM2	PWM3	CSP3	CSP2	CSP1
3-PH	--	--	--	--	--	--
2-PH	--	--	Floating	PVCC	--	--
1-PH	--	Floating	Floating	PVCC	PVCC	--

Note 1: "--" denotes normal connection.
Note 2: Use 100kΩ pull-up resistor when pull up to PVCC
Note 3: Strictly follow the table for phase disable. Incorrect pull-up connection may cause catastrophic fault during start-up.

Voltage Control Loop and PWMVID Function

The PWMVID signal from GPU is applied to the VID pin, which is the input pin of the internal buffer. This buffer plays the role of level shifting, and the output of this buffer is injected into the external RC integrator to generate REFIN voltage, which can be calculated as:

$$V_{REFIN} =$$

$$V_{VREF} \times D \times \frac{R2 // (R3+R4+R5)}{R1+R2 // (R3+R4+R5)} \times \frac{R4+R5}{R3+R4+R5} +$$

$$V_{VREF} \times \frac{R1 // (R3+R4+R5)}{R2+R1 // (R3+R4+R5)} \times \frac{R4+R5}{R3+R4+R5}$$

where V_{REFIN} is the DC voltage of REFIN, V_{VREF} is the voltage of VREF (typically 2V), and D is the duty cycle of PWMVID input. The VREF pin is the output of an internal LDO, therefore an output decoupling capacitor is required. Recommend to connect at least a 1uF capacitor from VREF pin to local GND.

Boot Mode and Standby Mode

The PWMVID structure includes two operation modes: boot mode and standby mode. During boot mode, controller ignores the PWMVID signal before PGOOD signal goes high and the REFADJ pin enters high impedance state. The REFIN voltage during boot mode can be calculated as:

$$V_{REFIN,BOOT} = V_{VREF} \times \frac{R4+R5}{R2+R3+R4+R5}$$

During standby mode, other than GPU stopping the PWMVID transaction, an external system standby signal additionally controls the entry of standby mode. An additional external switch should be connected in parallel with the original PWMVID resistors as shown in Figure 5 to generate the standby mode voltage:

$$V_{REFIN,STDBY} =$$

$$V_{VREF} \times \frac{(R3+R4+R5)//R_{STDBY}}{R2+(R3+R4+R5)//R_{STDBY}} \times \frac{R4+R5}{R3+R4+R5}$$

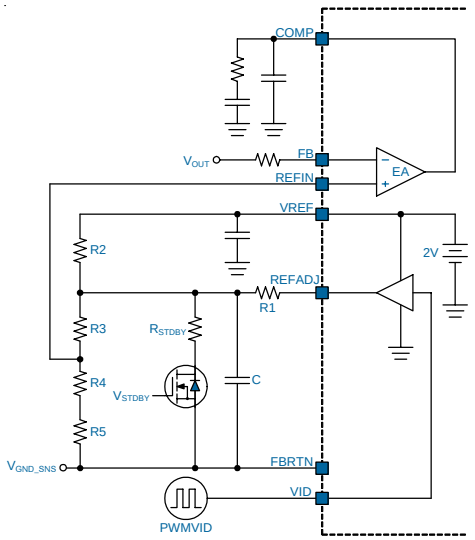


Figure 5. PWMVID Structure

Power Saving Mode

The uP9529Q provides power saving features for platform designers to program platform specific power saving configuration. There are four operation modes: Multi-phase CCM, multi-phase DCM, single-phase CCM, and single phase DCM. The uP9529Q switches between these four operation modes according to the input voltage level of the PSI pin. Figure 6 shows typical PSI application circuit, and Table 3 shows recommended PSI setting voltage level of four operation modes. In single-phase operation, the uP9529Q auto-selects phase 1 to be the operating phase. In DCM, the uP9529Q automatically reduces switching frequency at light load to maintain high efficiency. As the load current decreases, the rectifying MOSFET is turned off when zero inductor current is detected, and the converter runs in discontinuous conduction mode.

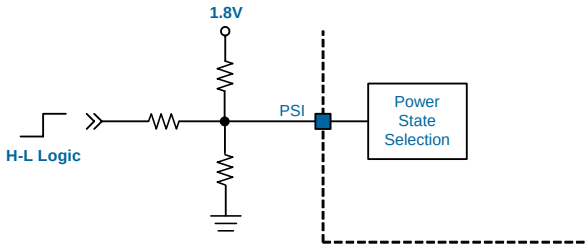


Figure 6. PSI Application Circuit

Table 3. Recommended PSI Setting

Operation Mode	Recommended Voltage Setting at PSI (V)
Multi-Phase CCM	1.8
Multi-Phase DCM	1.2
Single-Phase CCM	0.6
Single-Phase DCM	0

Channel Current Balance

The uP9529Q senses each phase current through CSPx pin for current balancing. The phase current signal is sampled and held when the low-side MOSFETs are turned on. The sensed current I_{SENx} can be determined by the following equation:

$$I_{SENx} = \frac{\Delta V_{CSPx}}{R_{SEN}}$$

Where I_{SENx} is the sampled and held phase current signal. **In IMON mode**, ΔV_{CSPx} is the differential voltage between CSPx and REFOUT, the R_{SEN} is internal sense resistor which is typical 5kΩ as shown in Figure 7. **In DCR mode**, ΔV_{CSPx} is the differential voltage between CSPx and CSN (V_{OUT}), the R_{SEN} is internal sense resistor which is typical 655Ω as shown in Figure 8. The sensed current I_{SENx} is mirrored to the current balance circuit, comparing between each other, and generating current adjusting signals for each phase.

Functional Description

These current adjusting signals are fed to the on-time circuit of the uP9529Q to separately adjust each phase on-time for the purpose of adjusting current balance.

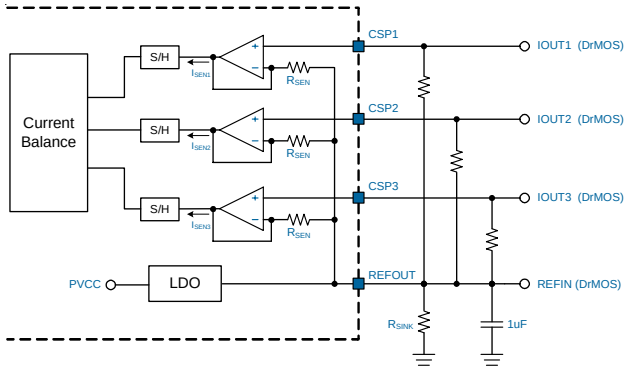


Figure 7. IMON Mode Current Balance Circuit

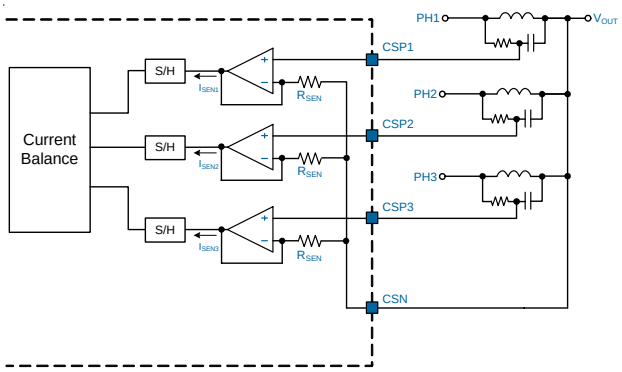


Figure 8. DCR Mode Current Balance Circuit

Over Voltage Protection (OVP)

The OVP is triggered if V_{FB} > 1.55 x V_{REFIN} sustained 6us. When OVP is activated, the uP9529Q turns on all low-side MOSFET and turns off all high-side MOSFET. The over voltage protection is a latch-off function and can only be reset by PVCC re-POR or EN/VINMON restart.

Under Voltage Protection (UVP)

The UVP is triggered, if V_{FB} < 0.45 x V_{REFIN} sustained 9us. When UVP is activated, the uP9529Q turns off all high-side and low-side MOSFET. The under voltage protection is a latch-off function and can only be reset by PVCC re-POR or EN/VINMON restart.

Over Temperature Protection (OTP)

The uP9529Q monitors the temperature of itself. If the temperature exceeds typical 160°C, the uP9529Q is forced into shutdown mode. The over temperature protection is a latch-off function and can only be reset by PVCC re-POR or EN/VINMON restart.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, PVCC ---------- -0.3V to +6V
Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV

Thermal Information

Package Thermal Resistance (Note 3)
WQFN3x3 - 20L θ_{JA} ---------- 68°C/W
WQFN3x3 - 20L θ_{JC} ---------- 6°C/W
Power Dissipation, P_D @ T_A = 25°C
WQFN3x3 - 20L ---------- 1.47W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{PVCC} ---------- 4.5V to 5.5V
Supply Input Voltage, V_{IN} ---------- 3.0V to 20V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(PVCC = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
PVCC POR Threshold	POR_{PVCC}	PVCC rising	3.8	4.1	4.4	V
PVCC POR Hysteresis	HYS_{PVCC_POR}		--	375	--	mV
Quiescent Current	I_Q	EN/VINMON = high , No switching	--	3	--	mA
Shutdown Current	I_{SD}	EN/VINMON = 0V	--	50	--	uA
Enable Control and Power Stage Input Voltage Monitoring (EN/VINMON)						
VINMON Monitoring Range			0.4	--	3.43	V
Logic Low	V_{IL_EN}		--	--	0.1	V
Logic High	V_{IH_EN}		0.4	--	--	V
PWMVID Interface (VREF, VID, REFADJ, REFIN)						
VREF Voltage Accuracy	V_{REF}		1.98	2	2.02	V
VREF Sourcing Current	I_{REF_SRC}	VREF short to GND	10	--	--	mA
REFIN Disable Threshold	V_{REFIN_DSB}		--	0.1	--	V
External Reference Voltage Range	V_{REFIN}		0.2	--	2	V
VID Input Low	V_{IL_VID}		--	--	0.6	V
VID input High	V_{IH_VID}		1.2	--	--	V
VID Tri-state Voltage	V_{TRI_VID}		--	0.9	--	V
VID Tri-state Delay	T_{TRI_VID}	VID from High to Tri-state; VID from Low to Tri-state	--	100	--	ns
REFADJ Source Resistance	R_{BF_SRC}	I_{SRC} = 1mA	--	20	--	Ω
REFADJ Sink Resistance	R_{BF_SNK}	I_{SINK} = 1mA	--	20	--	Ω
Soft-Start						
Output Ramp-up Time	T_ramp	Set to 600us	--	600	--	us
Initialization Time	T_{INIT}	EN/VINMON = high to V_{OUT} start up from 0V	--	550	--	us
On Time						
One Shot Width	T_{ON}	V_{IN}=12V, V_{OUT}=1.2V, F_{SW}=300kHz	--	333	--	ns
Minimum Off Time	T_{OFF_MIN}		--	400	--	ns
Minimum On Time	T_{ON_MIN}	V_{IN} > 15V, guaranteed by design	--	30	--	ns
		9V < V_{IN} ≤ 15V, guaranteed by design	--	60	--	
		9V ≥ V_{IN} , guaranteed by design	--	90	--	
FBRTN						
FBRTN Current	I_{FBRTN}	EN/VINMON = high, normal operation	--	--	100	uA

Electrical Characteristics

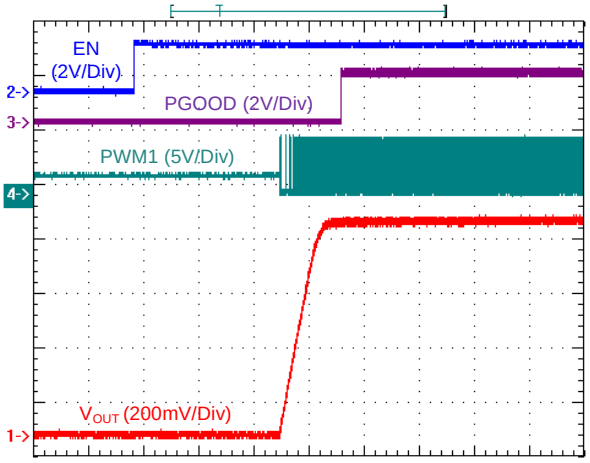
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Error Amplifier						
Offset Voltage	$V_{OS(EA)}$		-1	--	1	mV
Open Loop DC Gain	AO	Guaranteed by Design	--	70	--	dB
Gain-Bandwidth Product	GBW	Guaranteed by Design	--	10	--	MHz
Trans-conductance	GM		--	2020	--	uA / V
COMP Source Current	I_{COMP_SRC}		--	300	--	uA
COMP Sink Current	I_{COMP_SNK}		--	300	--	uA
Current Sense Amplifier (CSP1~CSP3, CSN)						
Input Offset Voltage	V_{OFF_CSA}	Guaranteed by Design	-1	--	1	mV
Max Sourcing Current	I_{SRC_CSA}		100	--	--	uA
REFOUT						
REFOUT Output Voltage	V_{REFOUT}		--	1.2	--	V
REFOUT Sink Resistor	R_{REFOUT}	Guaranteed by Design	--	240	--	kΩ
PWM Output (PWM1 ~ PWM3)						
Output Low Voltage	V_{PWM_L}	I_{SINK} = 4mA	--	--	0.2	V
Output Hight Voltage	V_{PWM_H}	I_{SOURCE} = 4mA	4.7	--	--	V
High Impedance State Leakage		V_{PWM} = 0V	-1	--	0	uA
		V_{PWM} = 5V	0	--	1	uA
Power Saving Input (PSI)						
Power Saving Mode Logic	V_{PSI}	Multi-Phase CCM	1.6	--	--	V
		Multi-Phase DCM	1	--	1.4	
		Single-Phase CCM	0.4	--	0.8	
		Single-Phase DCM	--	--	0.2	
Zero Current Detection Offset Voltage						
Zero Current Detection Offset Voltage	V_{ZC_OFFSET}	DCR Mode,V_{CSP} - V_{OUT}	--	1.6	--	mV
		IMON Mode,V_{CSP} - V_{REFOUT}	--	8	--	
Protection						
Phase Current Limit (OCL) Setting Range	V_{FSOC}	Measure V_{FSOC}	600	--	1320	mV
Under Voltage Protection (UVP) Threshold	V_{UVP}	V_{FB}/V_{REFIN}	--	45	--	%
Under Voltage Protection (UVP) Delay	T_{UVP}		--	9	--	us
Over Voltage Protection (OVP) Threshold	V_{OVP}	V_{FB}/V_{REFIN}	--	155	--	%
Over Voltage Protection (OVP) Delay	T_{OVP}		--	6	--	us
Over Temperature Protection (OTP)	T_{OTP}	Guaranteed by Design	--	160	--	°C

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Good Indicator						
PGOOD Output Low Level	V_{PGOOD}	I_{SINK} = 4mA	--	--	0.3	V
PGOOD Leakage Current	I_{PGOOD_Leak}	V_{PGOOD} = 5V	--	--	0.1	uA

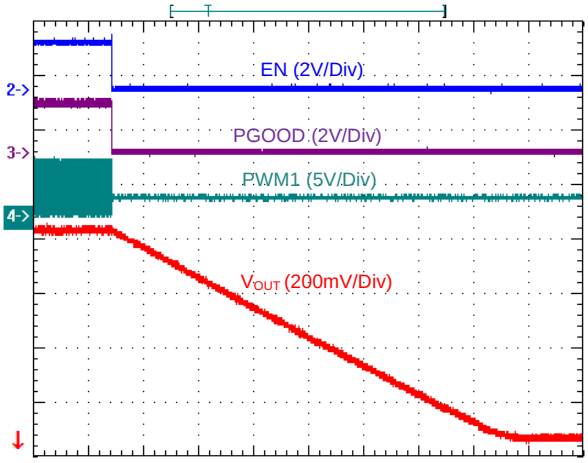
Typical Operation Characteristics

Enable Power On



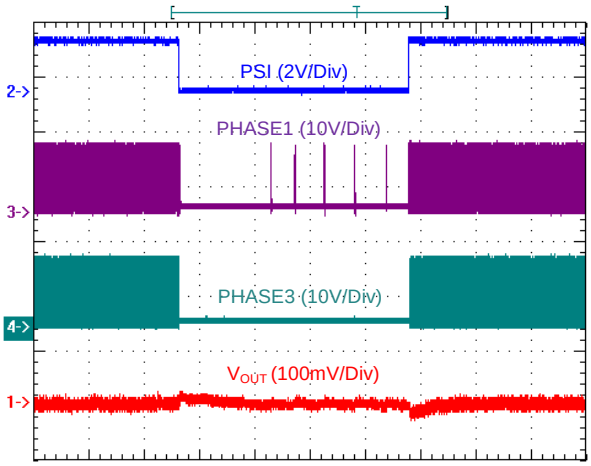
Time：200us/Div
V_{IN} = 12V V_{OUT} = 0.81V, No Load

Enable Power Off



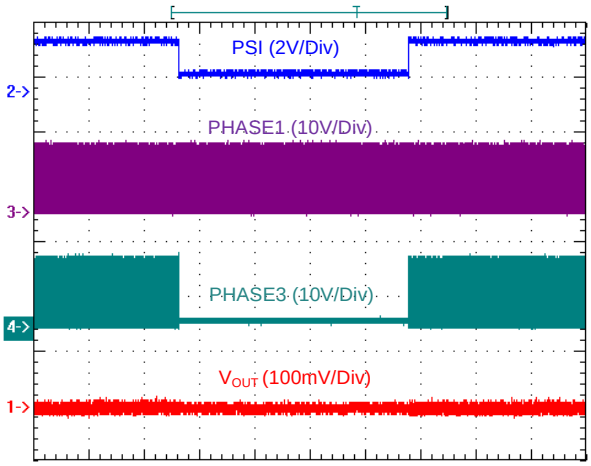
Time：400us/Div
V_{IN} = 12V V_{OUT} = 0.81V, I_{OUT} = 1A

PSI = 1.8V ⇆ 0V



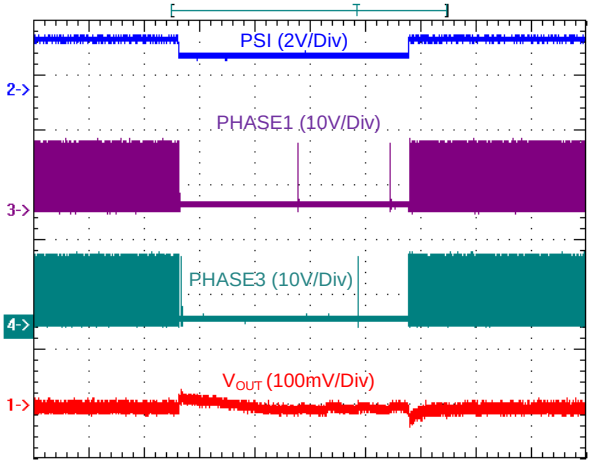
Time：400us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} Offset = 0.81V, I_{OUT} = 0.1A

PSI = 1.8V ⇆ 0.6V



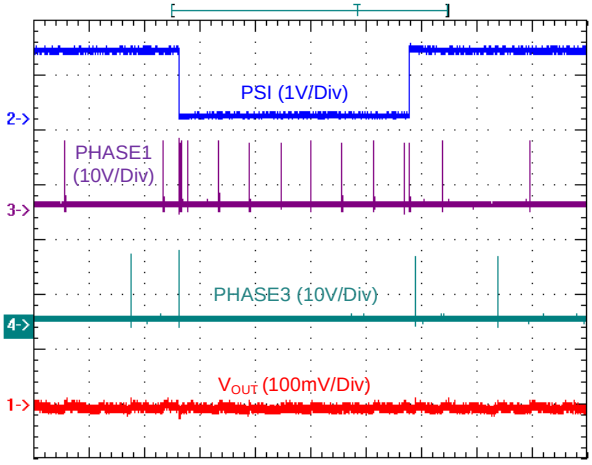
Time：400us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} Offset = 0.81V, I_{OUT} = 0.1A

PSI = 1.8V ⇆ 1.2V



Time：400us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} Offset = 0.81V, I_{OUT} = 0.1A

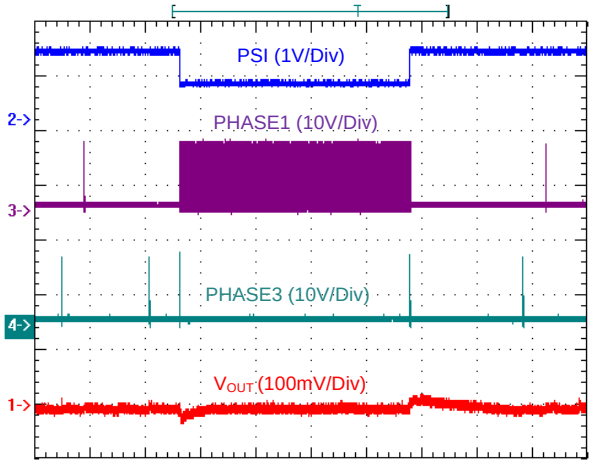
PSI = 1.2V ⇆ 0V



Time：400us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} Offset = 0.81V, I_{OUT} = 0.1A

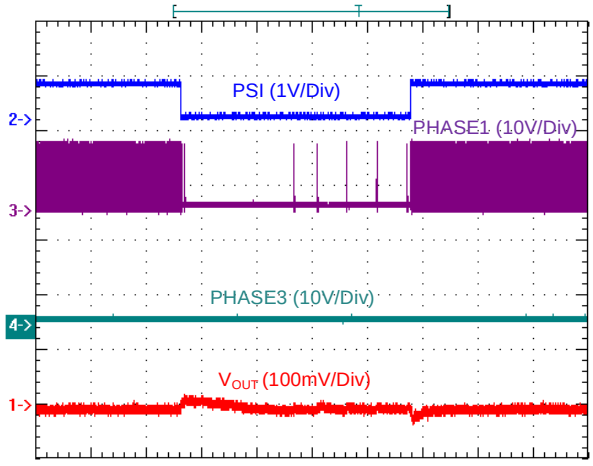
Typical Operation Characteristics

PSI = 1.2V ⇆ 0.6V



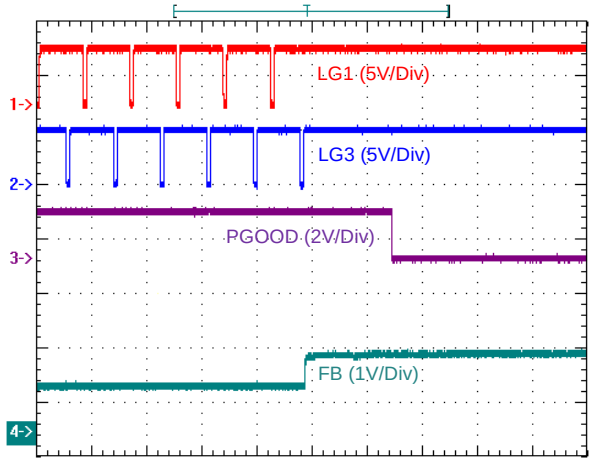
Time：400us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} Offset = 0.81V, I_{OUT} = 0.1A

PSI = 0.6V ⇆ 0V



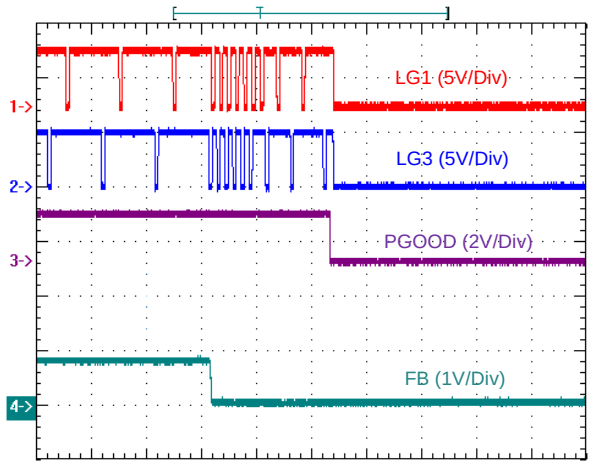
Time：400us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} Offset = 0.81V, I_{OUT} = 0.1A

OVP



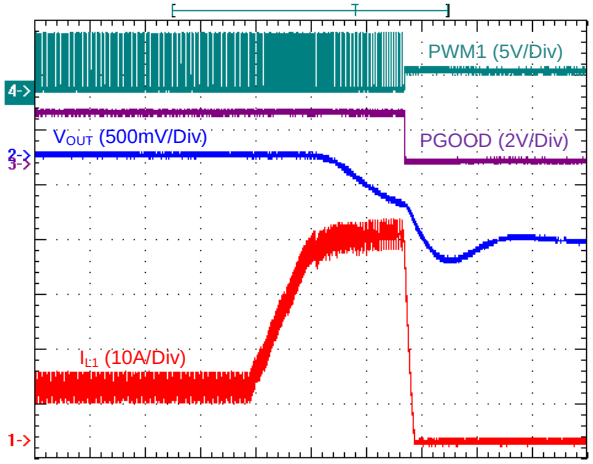
Time：4us/Div
V_{IN} = 12V V_{OUT} = 0.81V, No Load

UVP



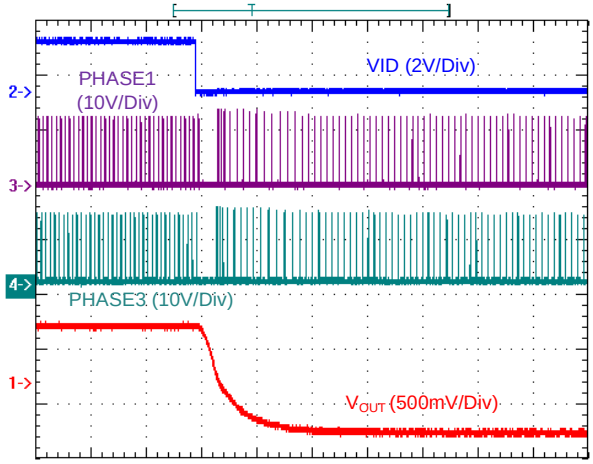
Time：4us/Div
V_{IN} = 12V V_{OUT} = 0.81V, No Load

Over Current Limit



Time：100us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} offset = 0.81V,
I_{OUT} = 10A to 70A

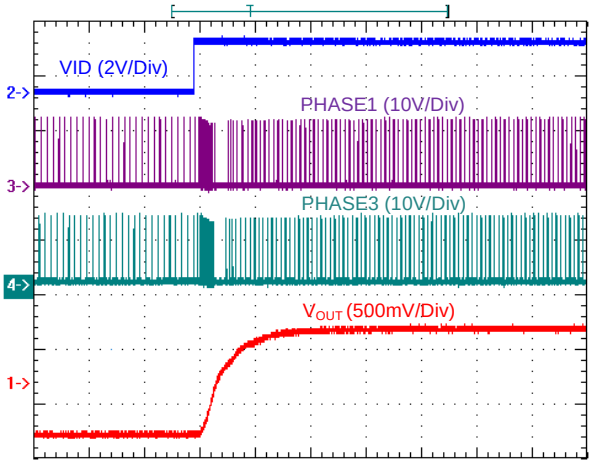
VID Transition: High to Low



Time：40us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} offset = 0.81V, No Load

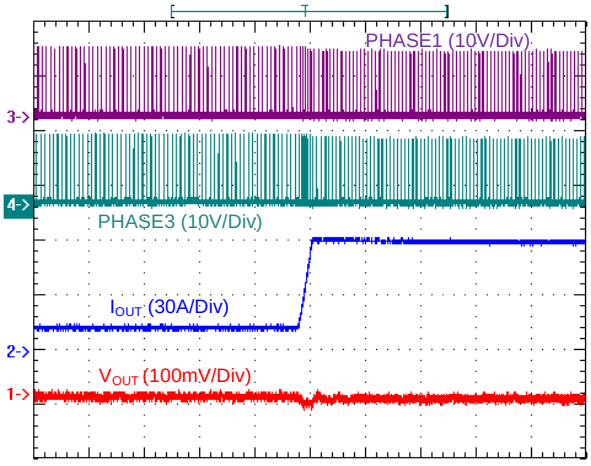
Typical Operation Characteristics

VID Transition: Low to High



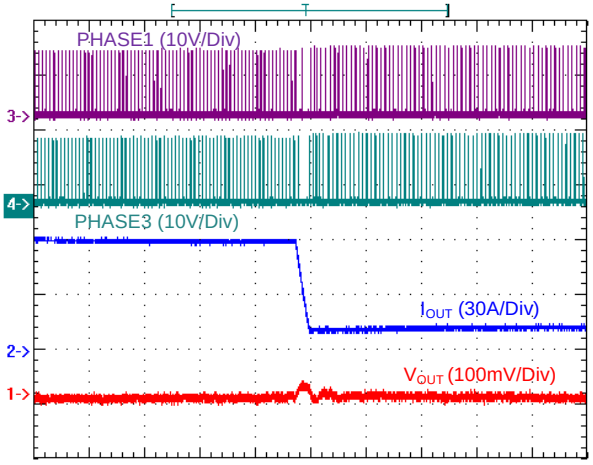
Time：40us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} offset = 0.81V, No Load

Load Transient, Undershoot



Time：40us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} offset = 0.81V,
PSI = 1.8V, I_{OUT} = 14A to 67A

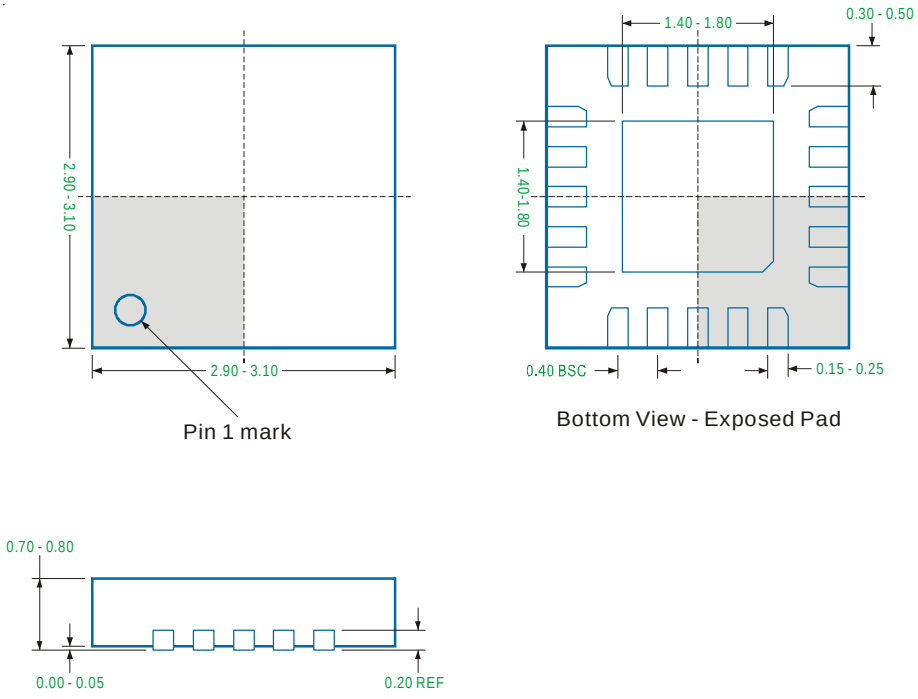
Load Transient, Overshoot



Time：40us/Div
V_{IN} = 12V, V_{OUT} = 0.81V, V_{OUT} offset = 0.81V,
PSI = 1.8V, I_{OUT} = 14A to 67A

Package Information

WQFN3x3 - 20L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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