

PG161-A00

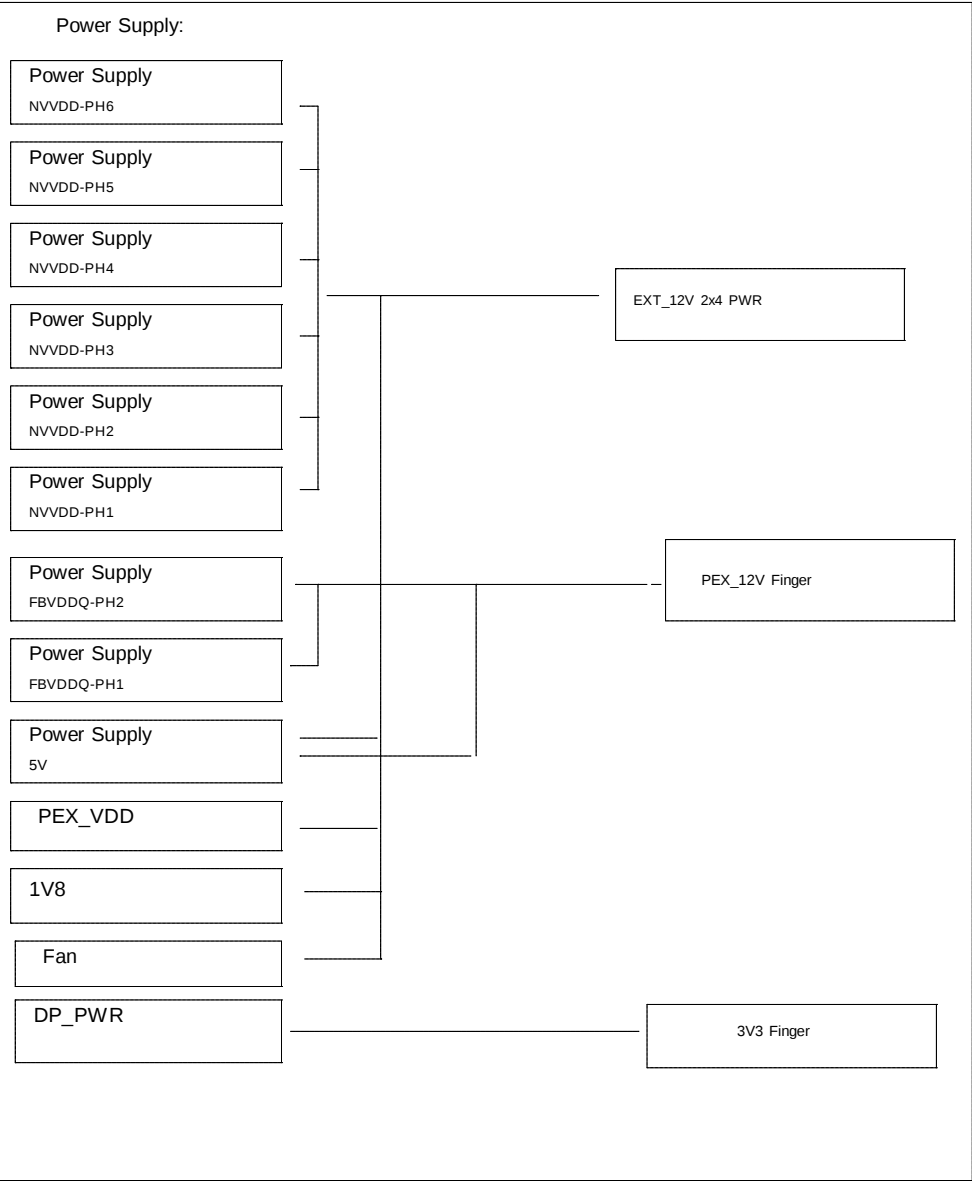
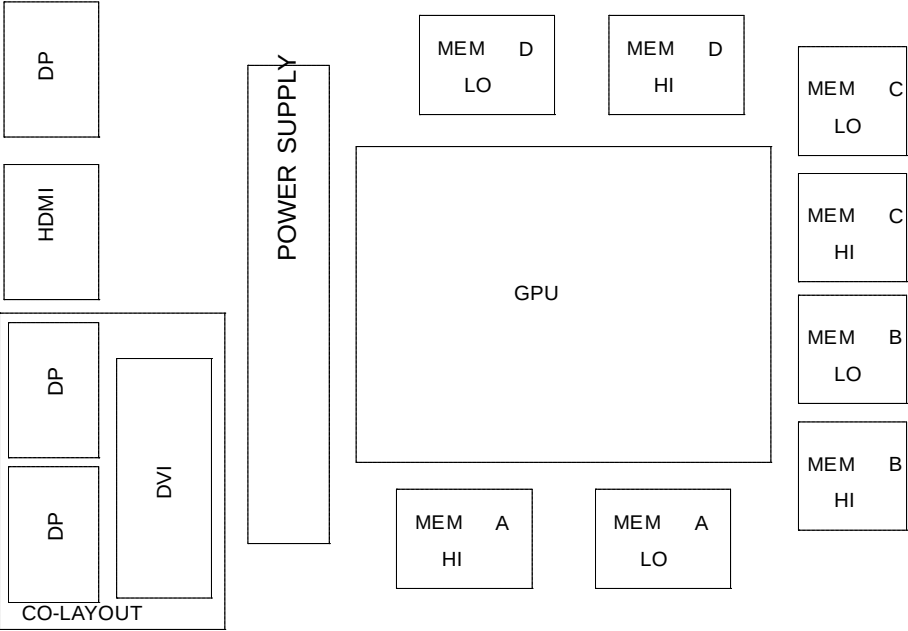
TU106 6GB GDDR6, 192b, X16
DVI-D/DP + DP + HDMI

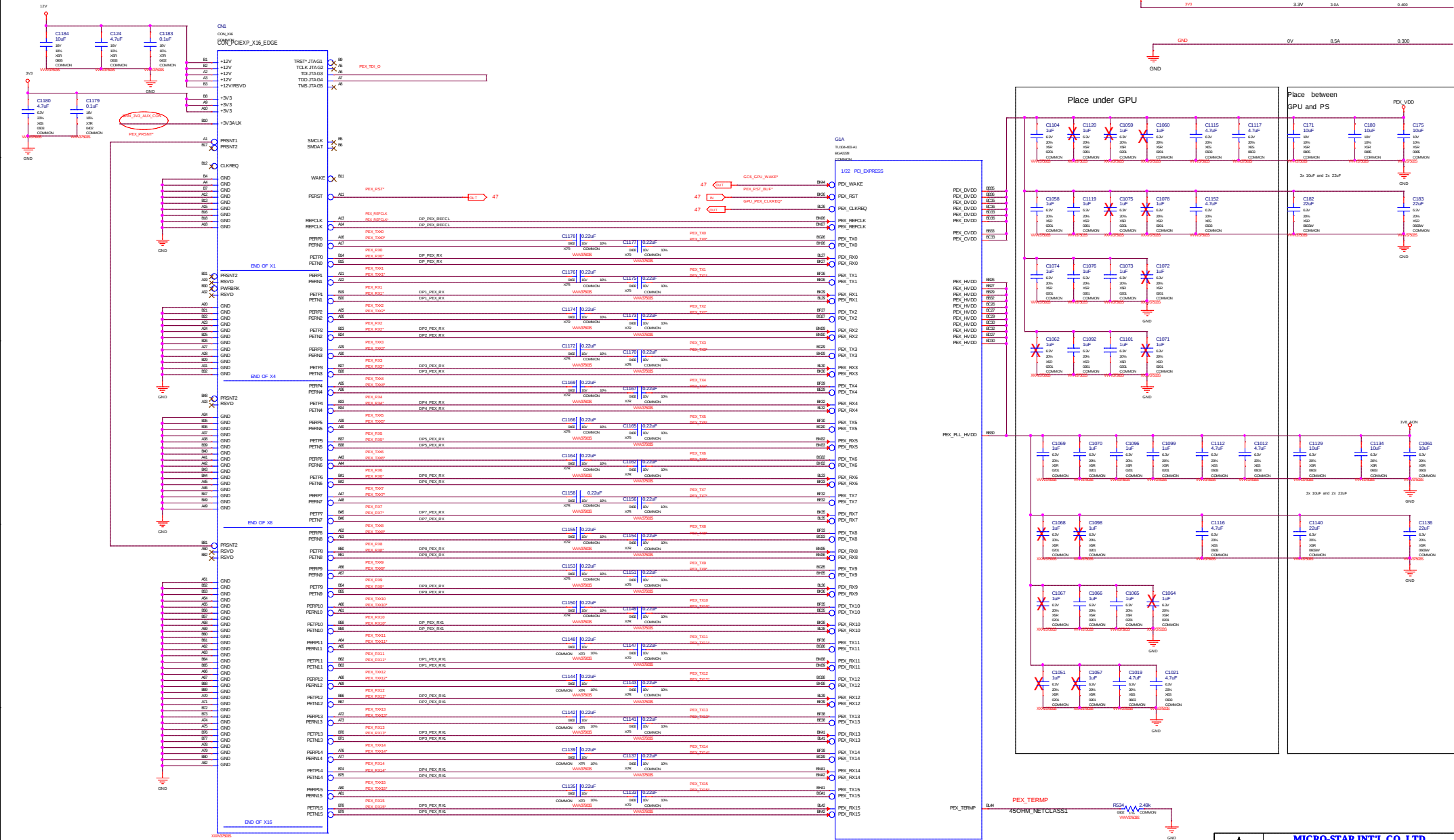
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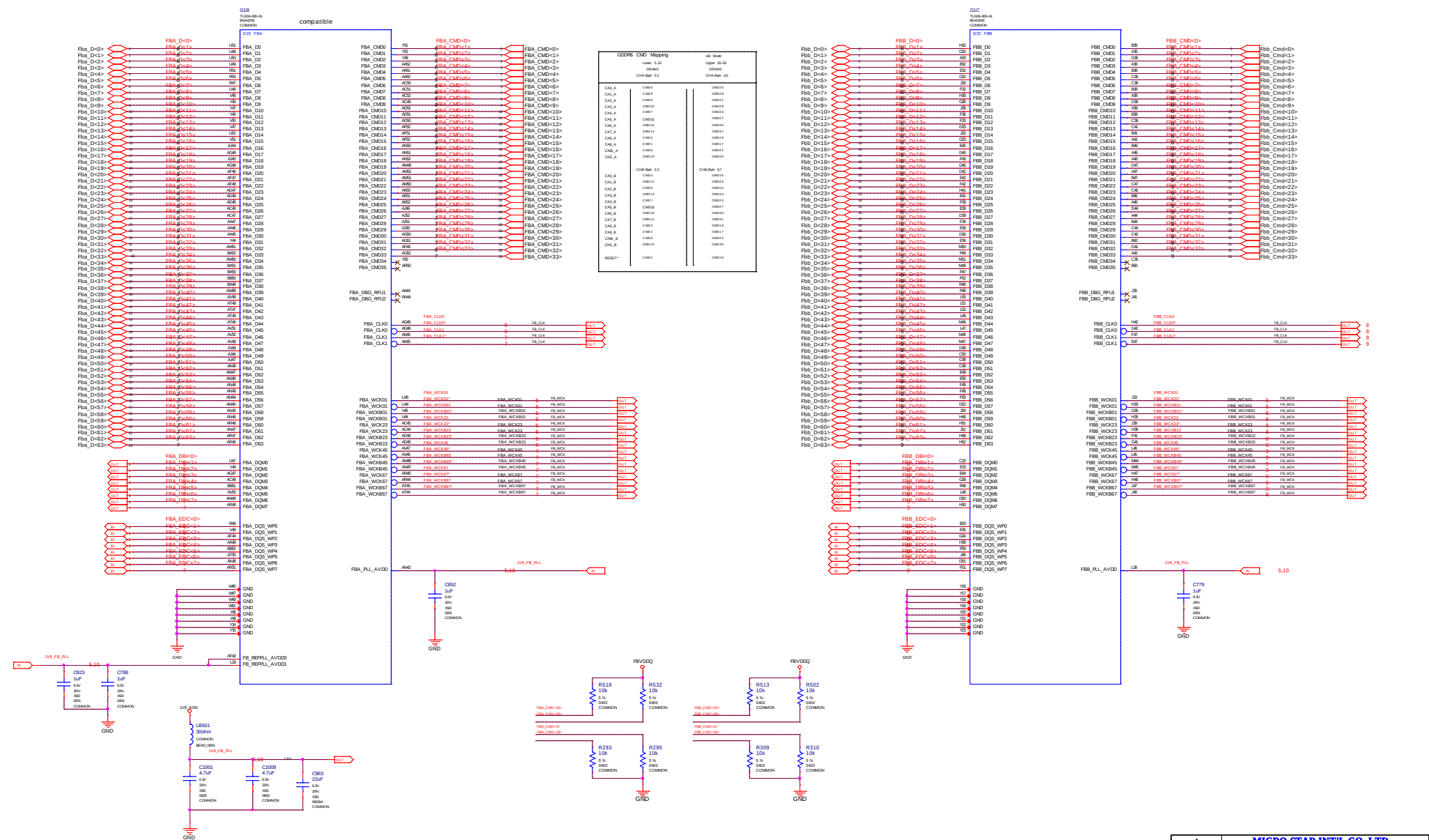
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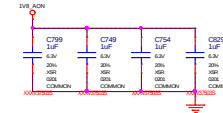
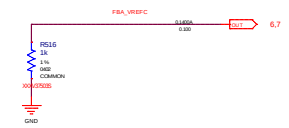
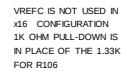
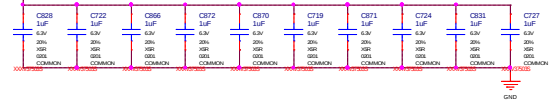
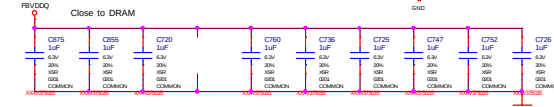
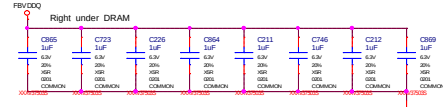
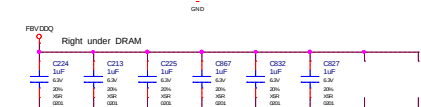
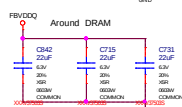
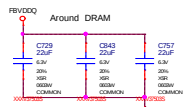
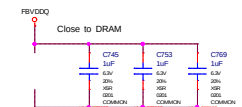
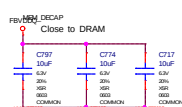
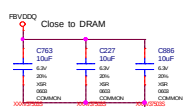
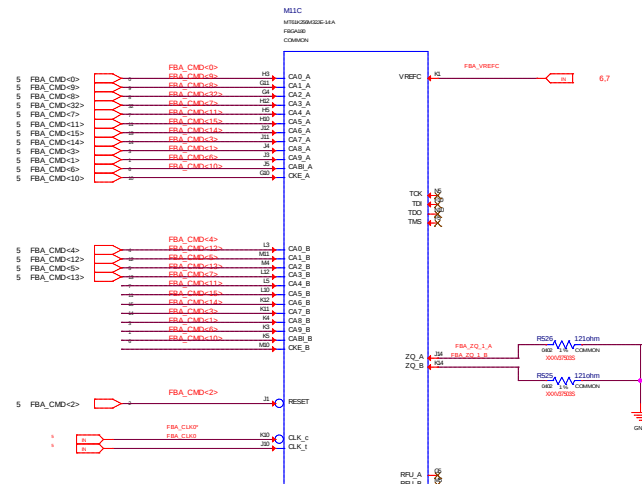
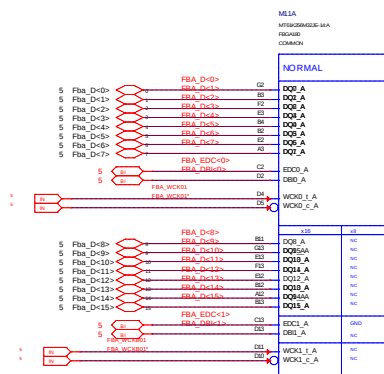
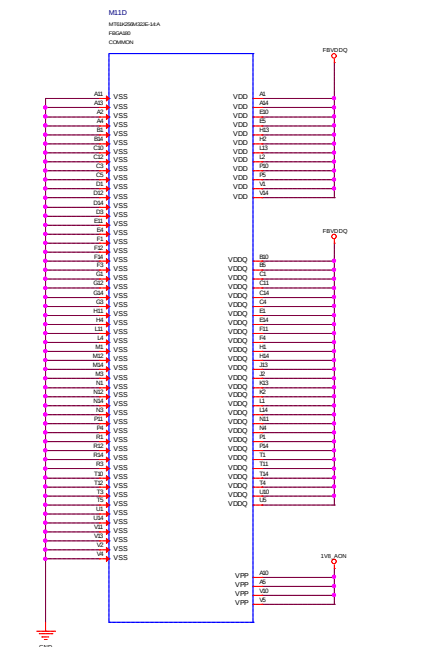
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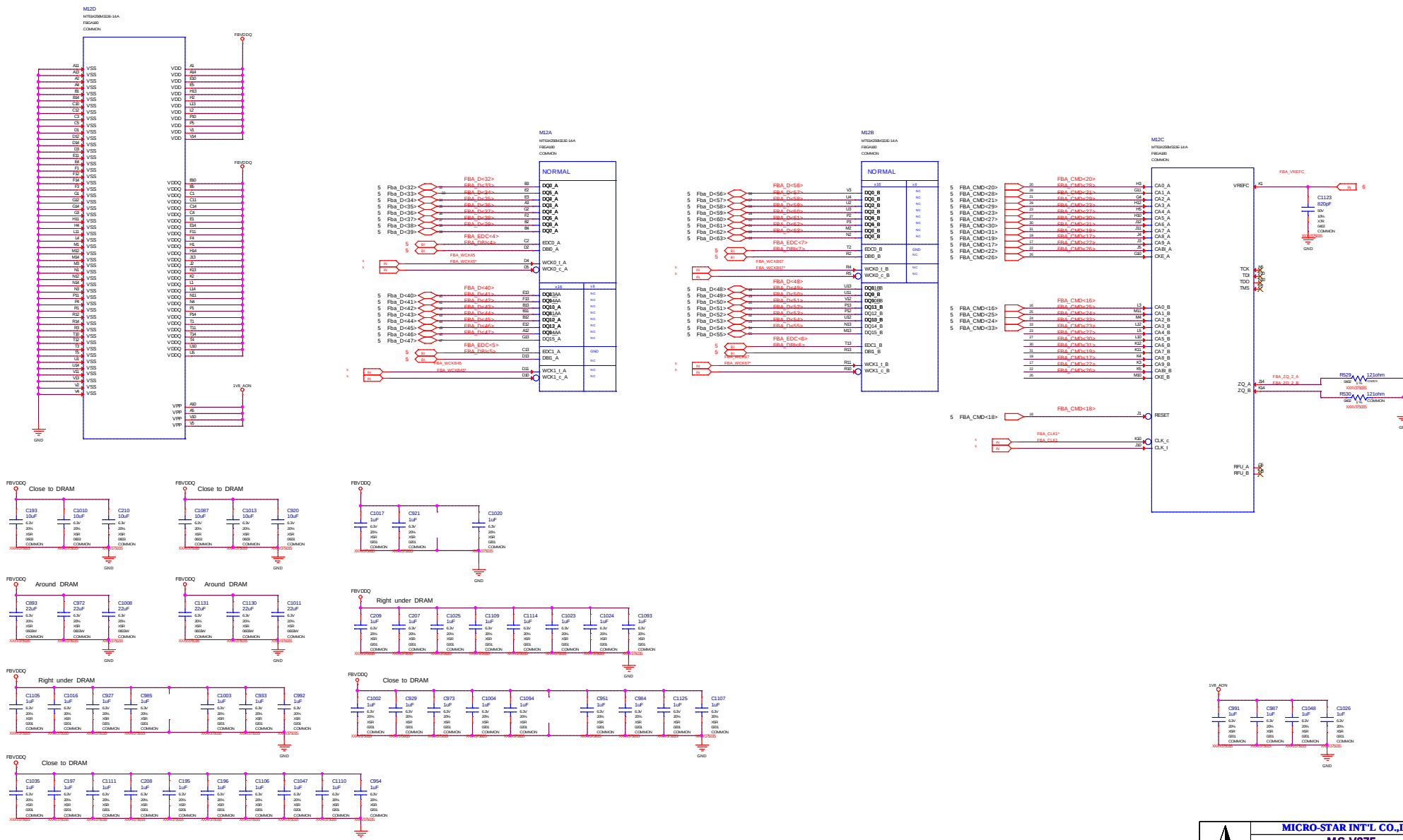


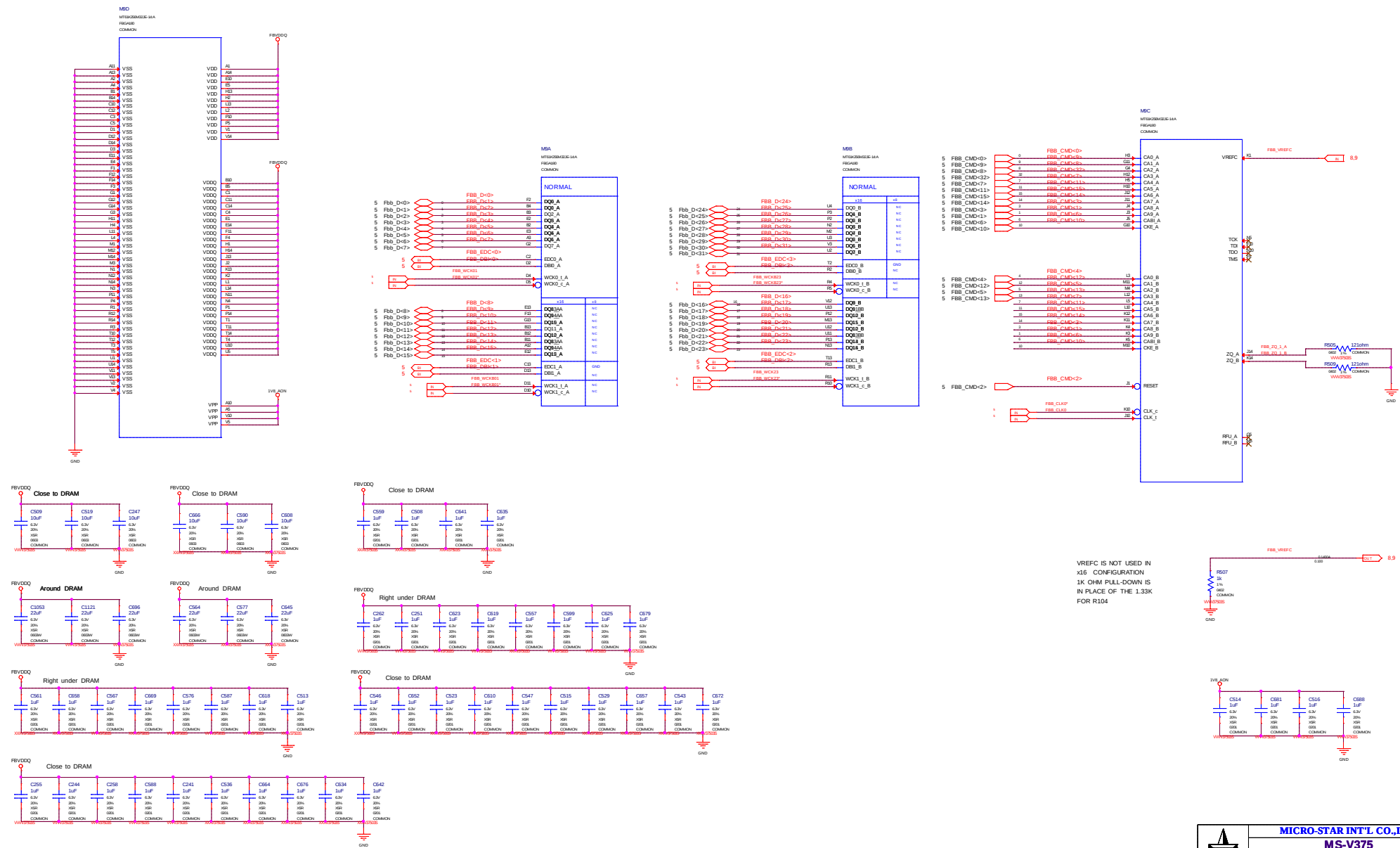


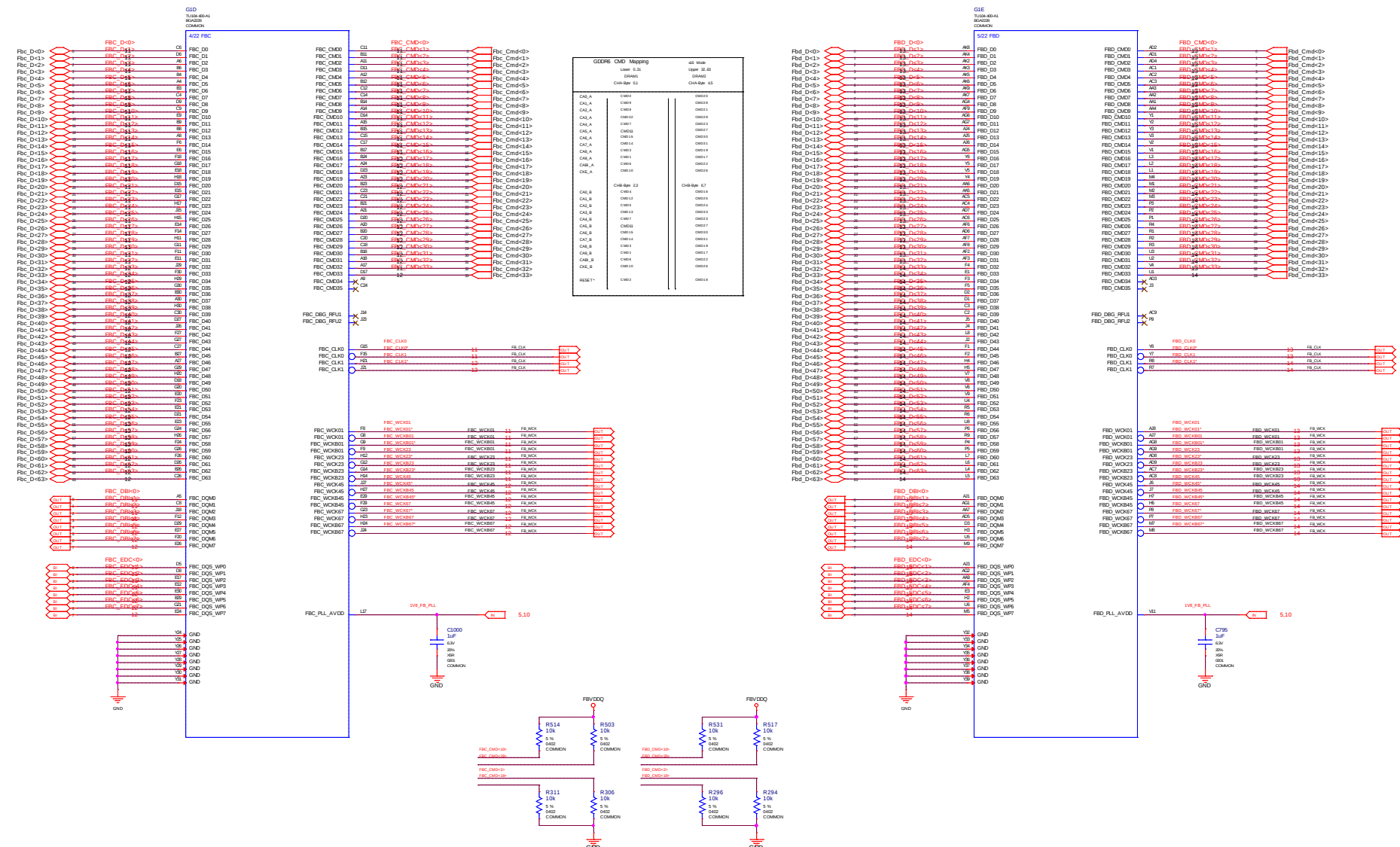
NO PEX GEN4 SUPPORT DELETE RC TERMINATIONS

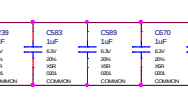
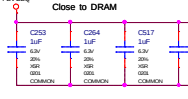
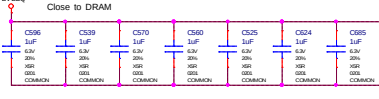
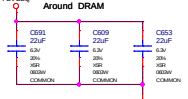
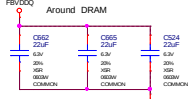
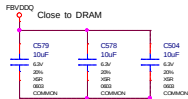
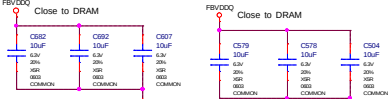
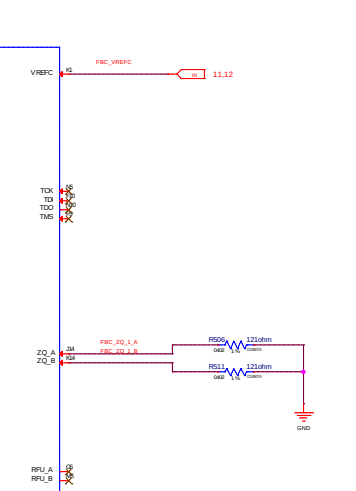
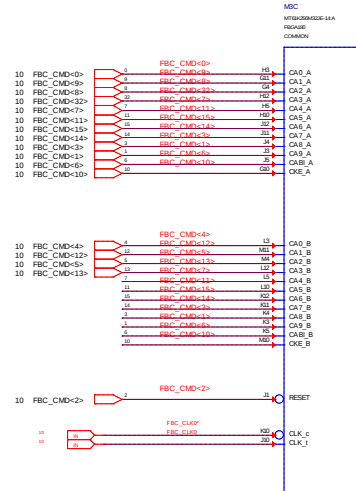
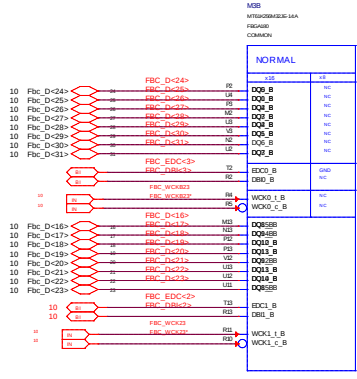
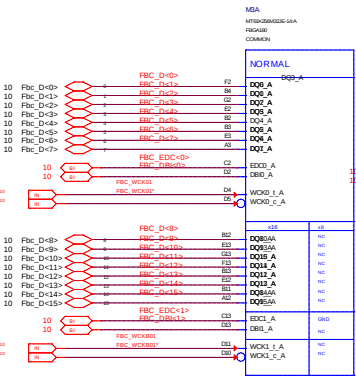
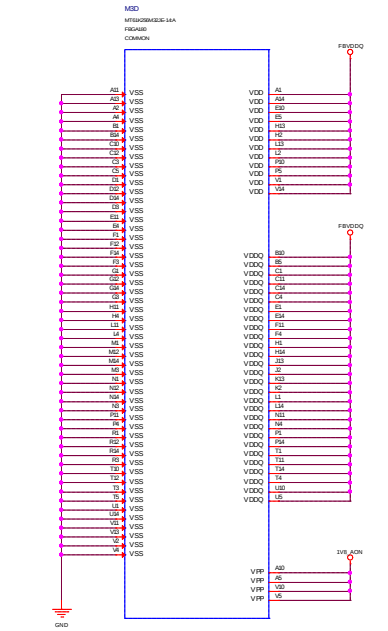




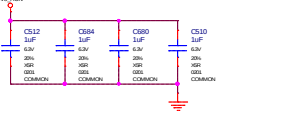


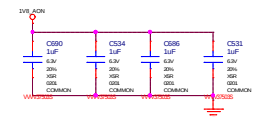
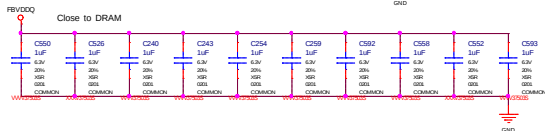
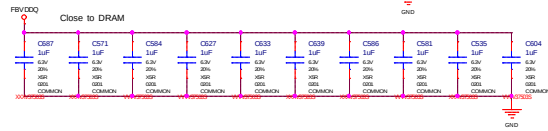
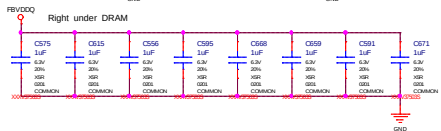
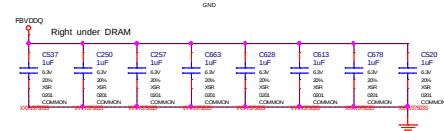
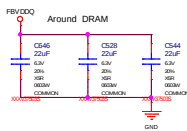
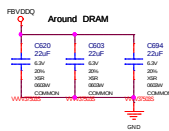
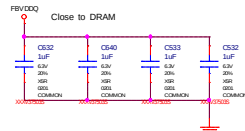
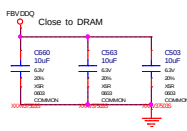
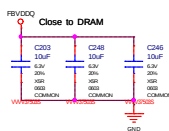
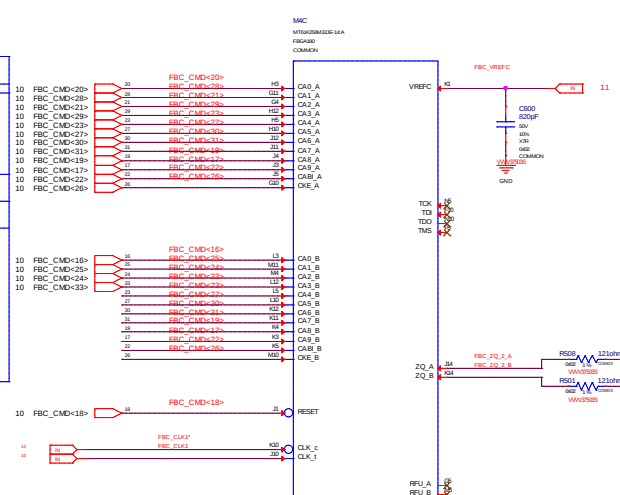
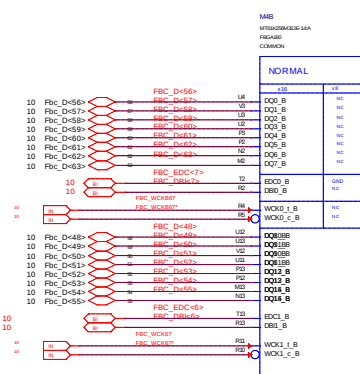
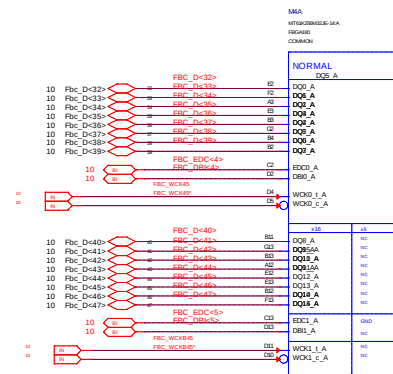


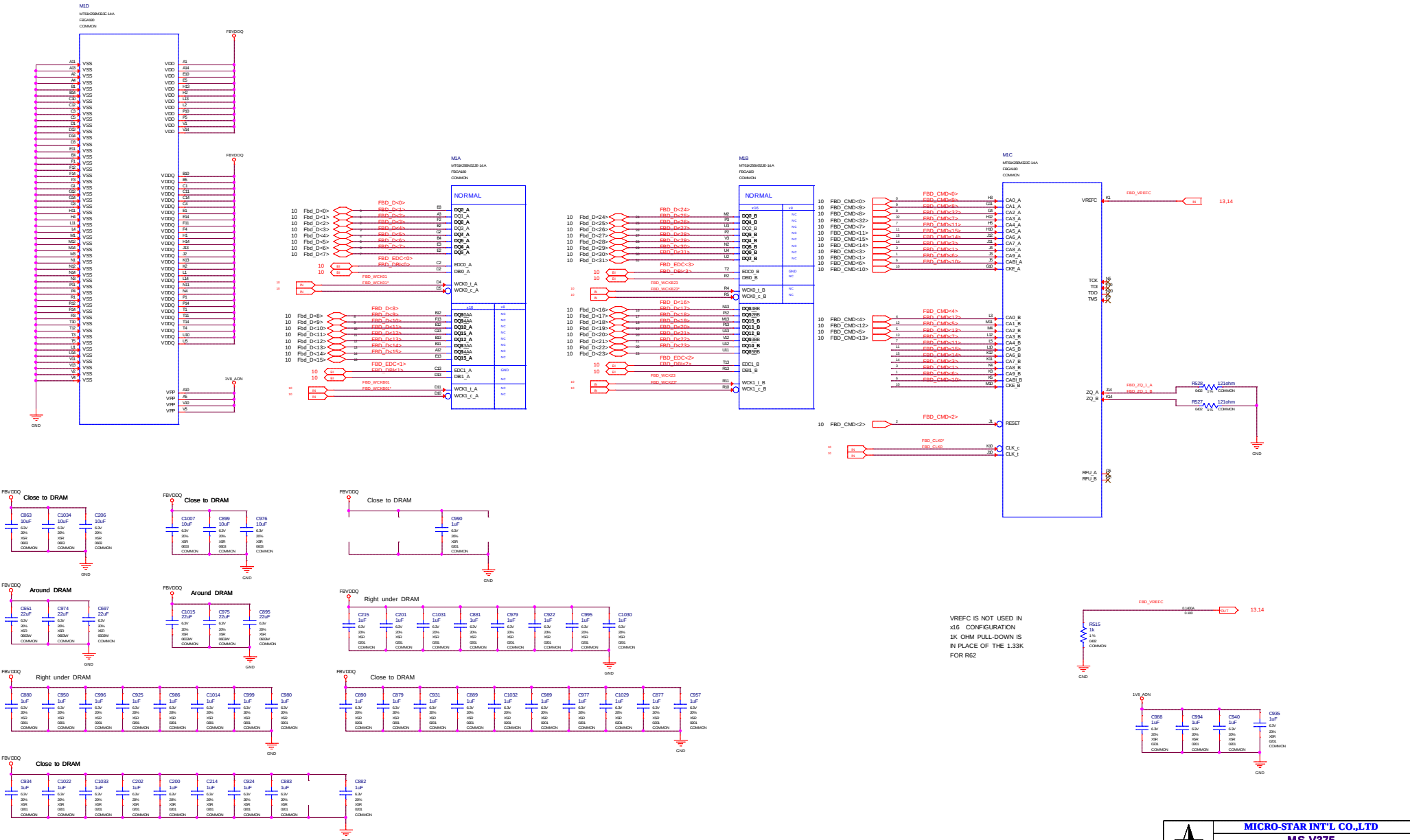


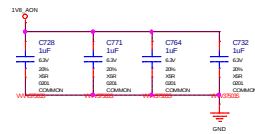
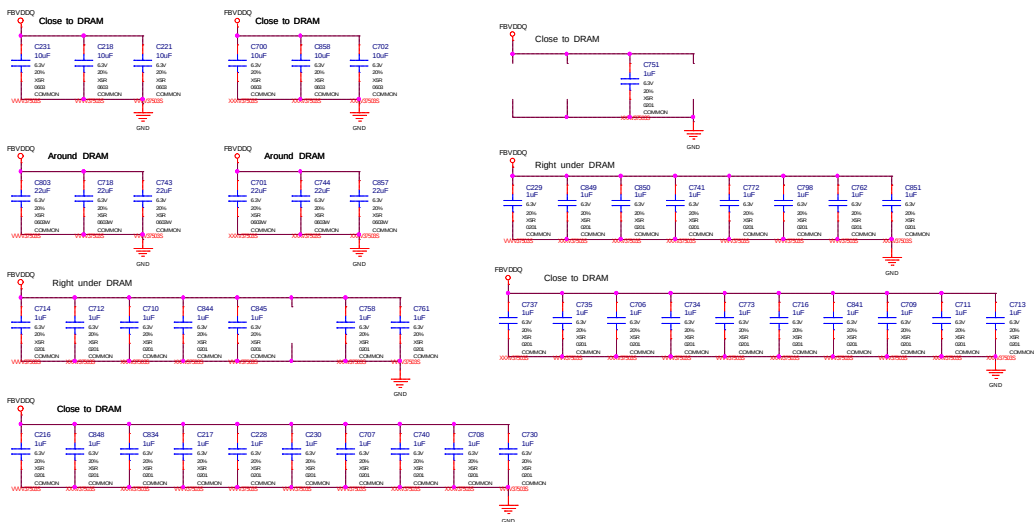
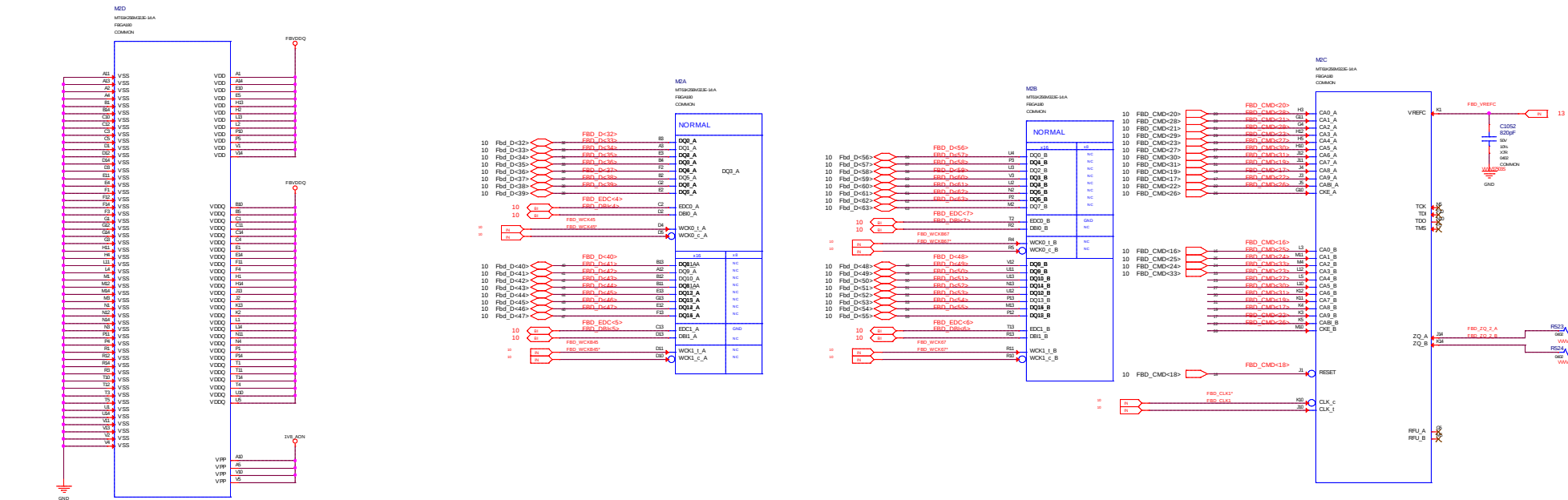


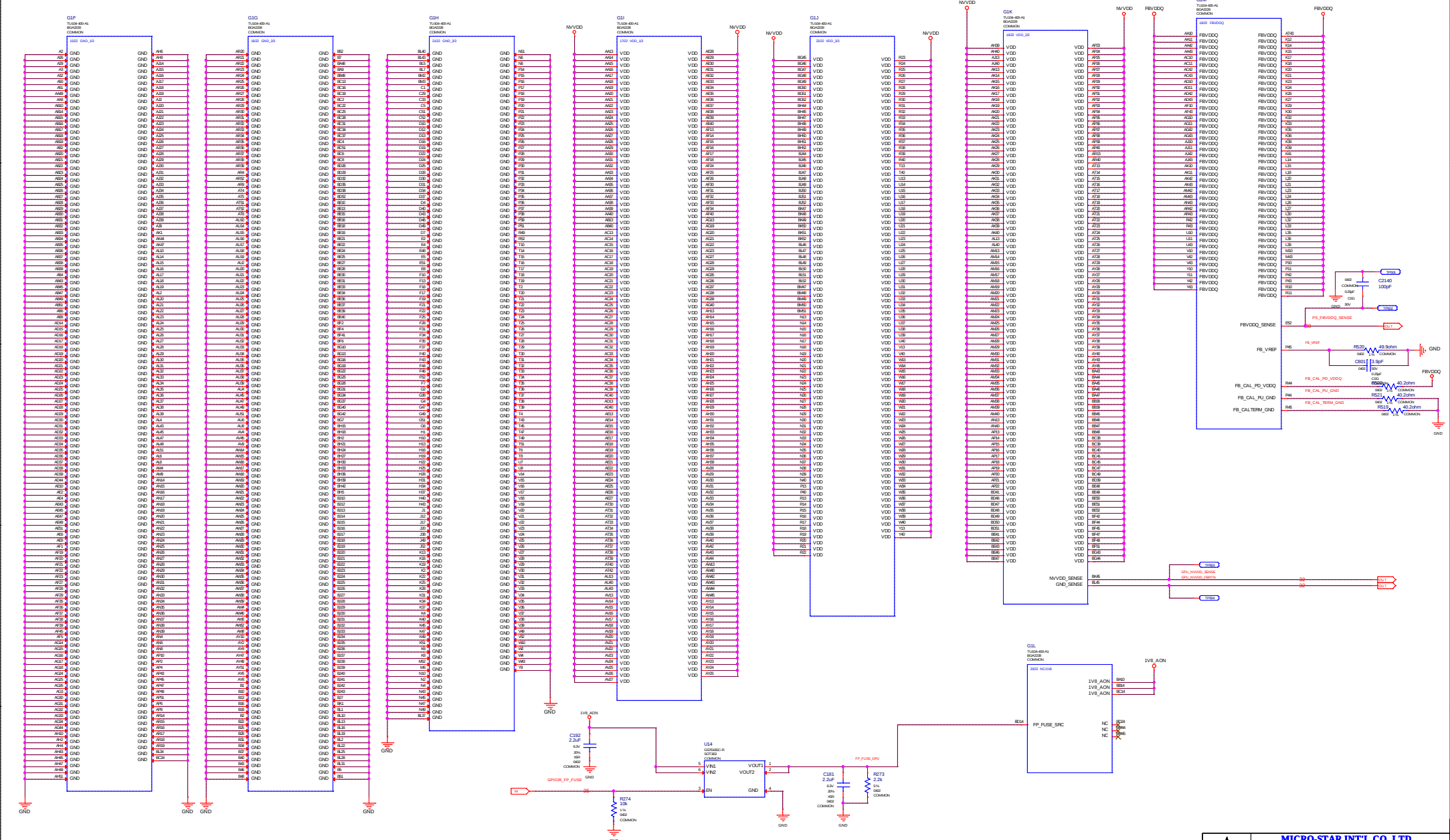
VREFC IS NOT USED IN
X16 CONFIGURATION IS
IN PLACE OF THE 1.33K
FOR R75









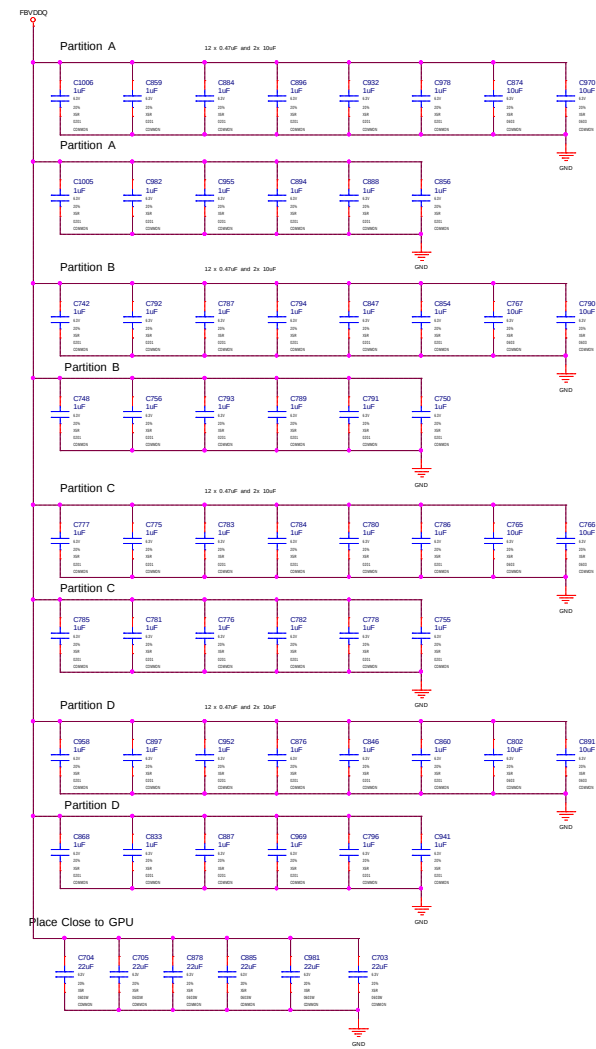


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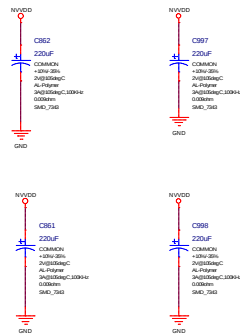
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Rev	Document Description	Rev
0.0	GPU PWR and GND	0.0
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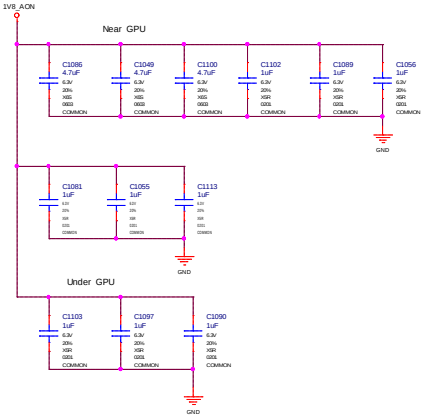
FBVDDQ



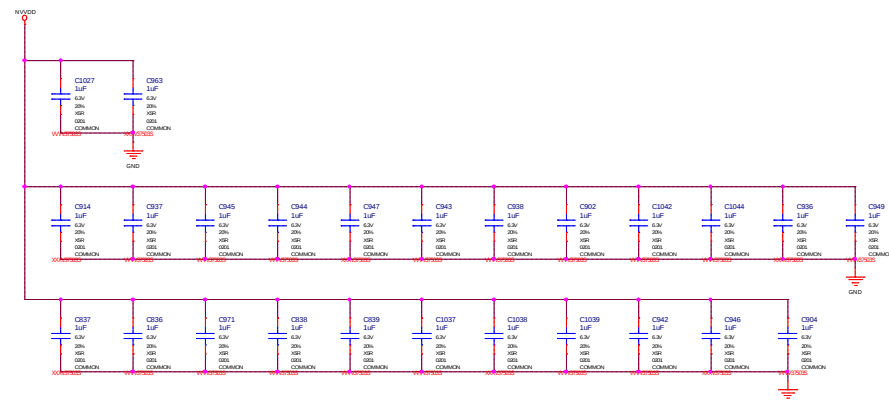
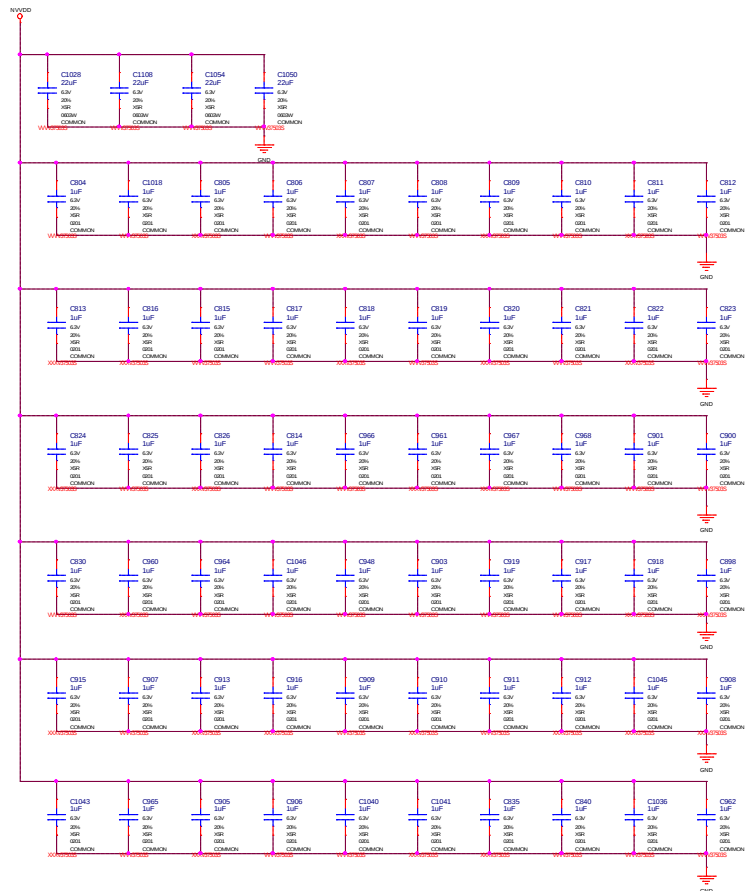
NWDD



1V8_AON



NVVDD

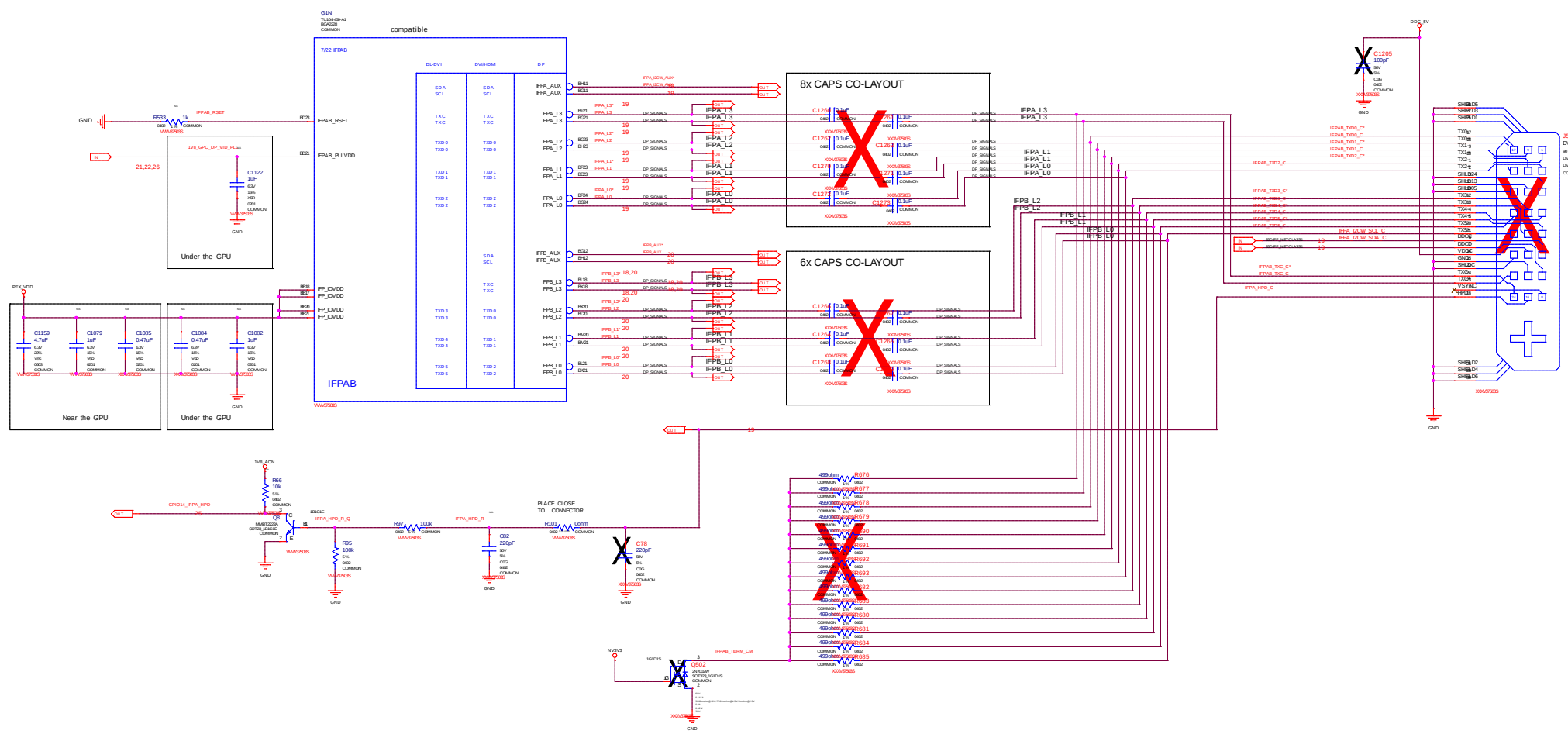


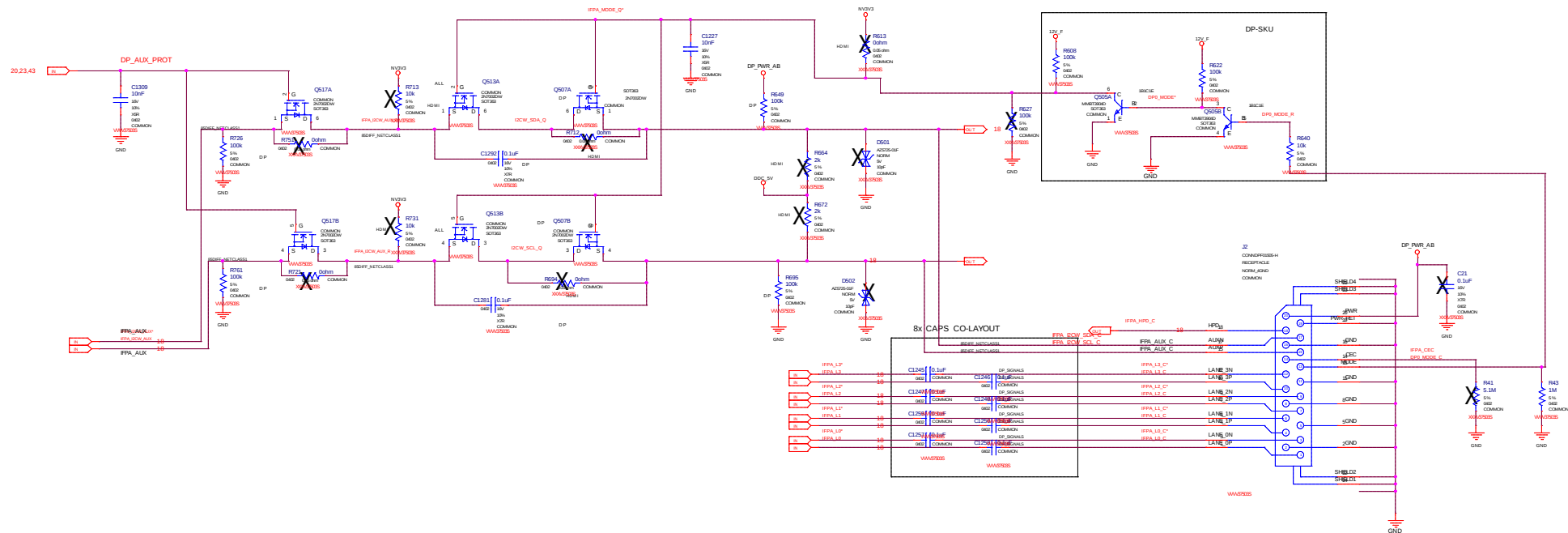
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IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP

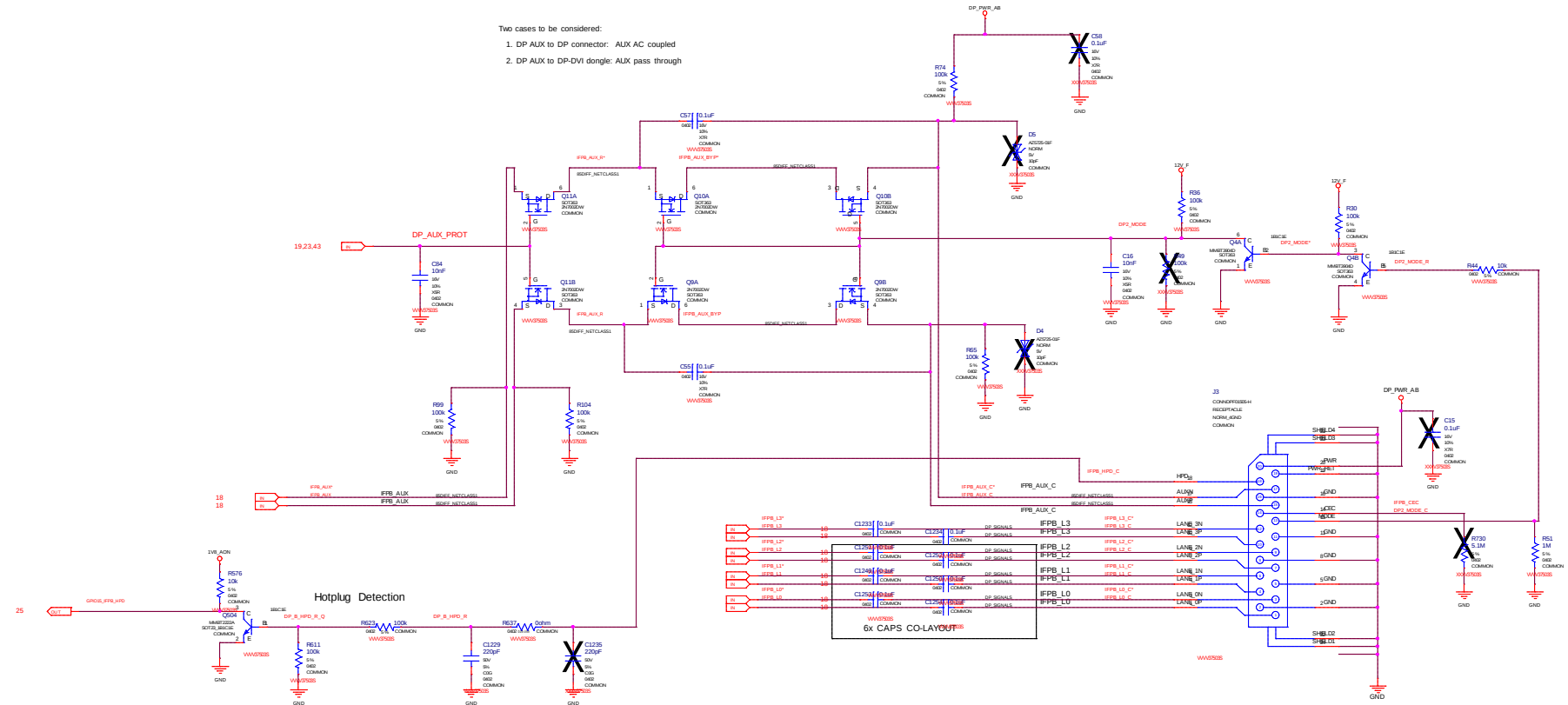




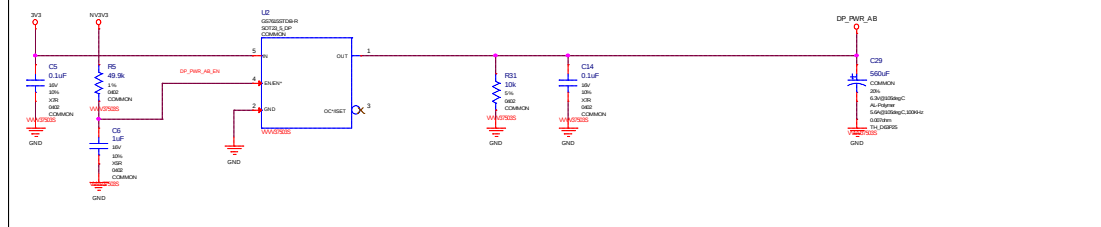
IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



Fused DP_PWR

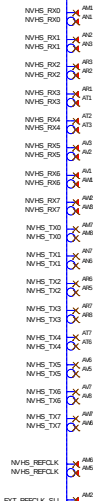


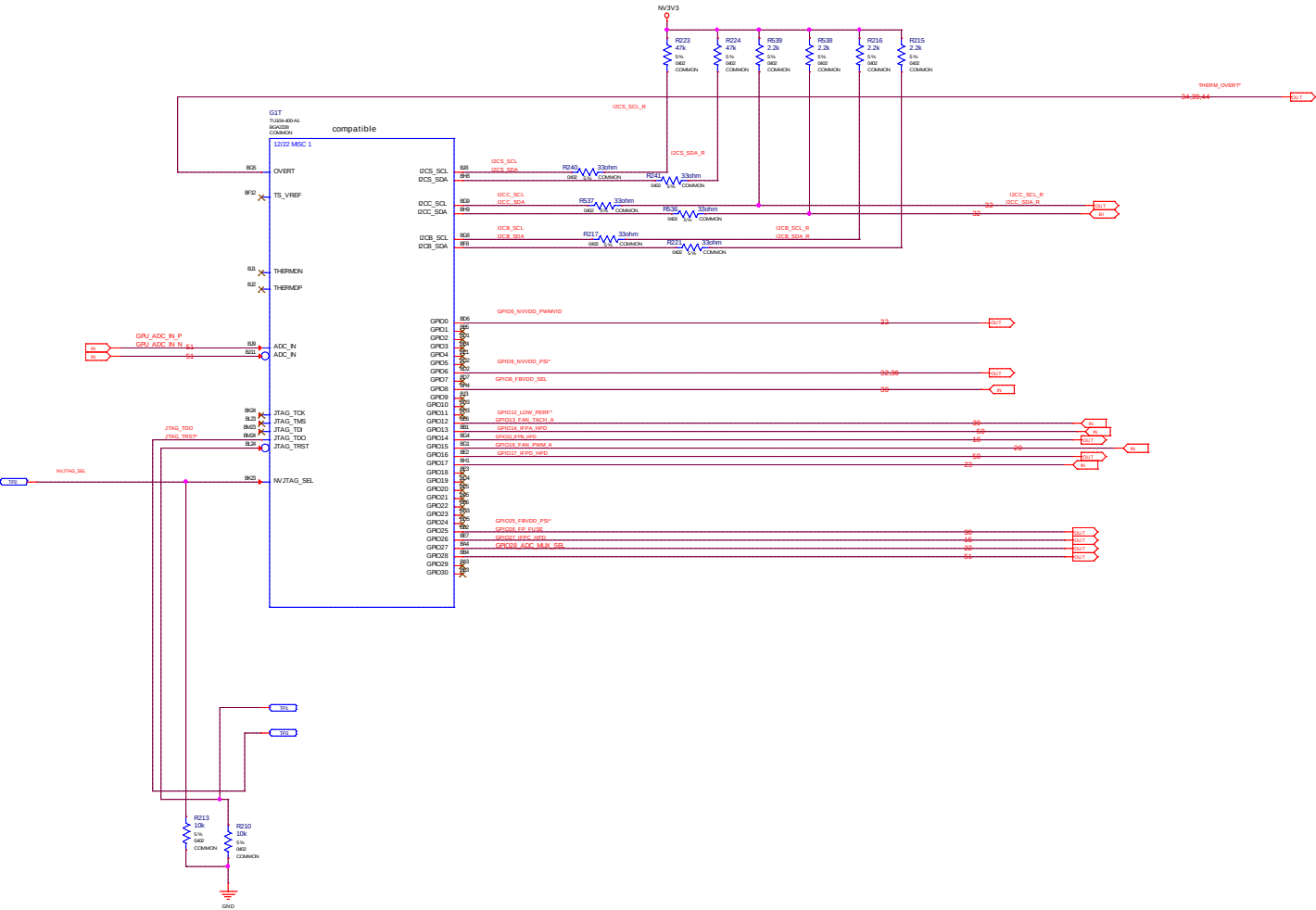
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Custom	MISC1: Fan, Thermal, JTAG, GPIO		2.0
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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00110	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

注意上件的MEM Straps

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]FS_OVERT	1ENABLE 0DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

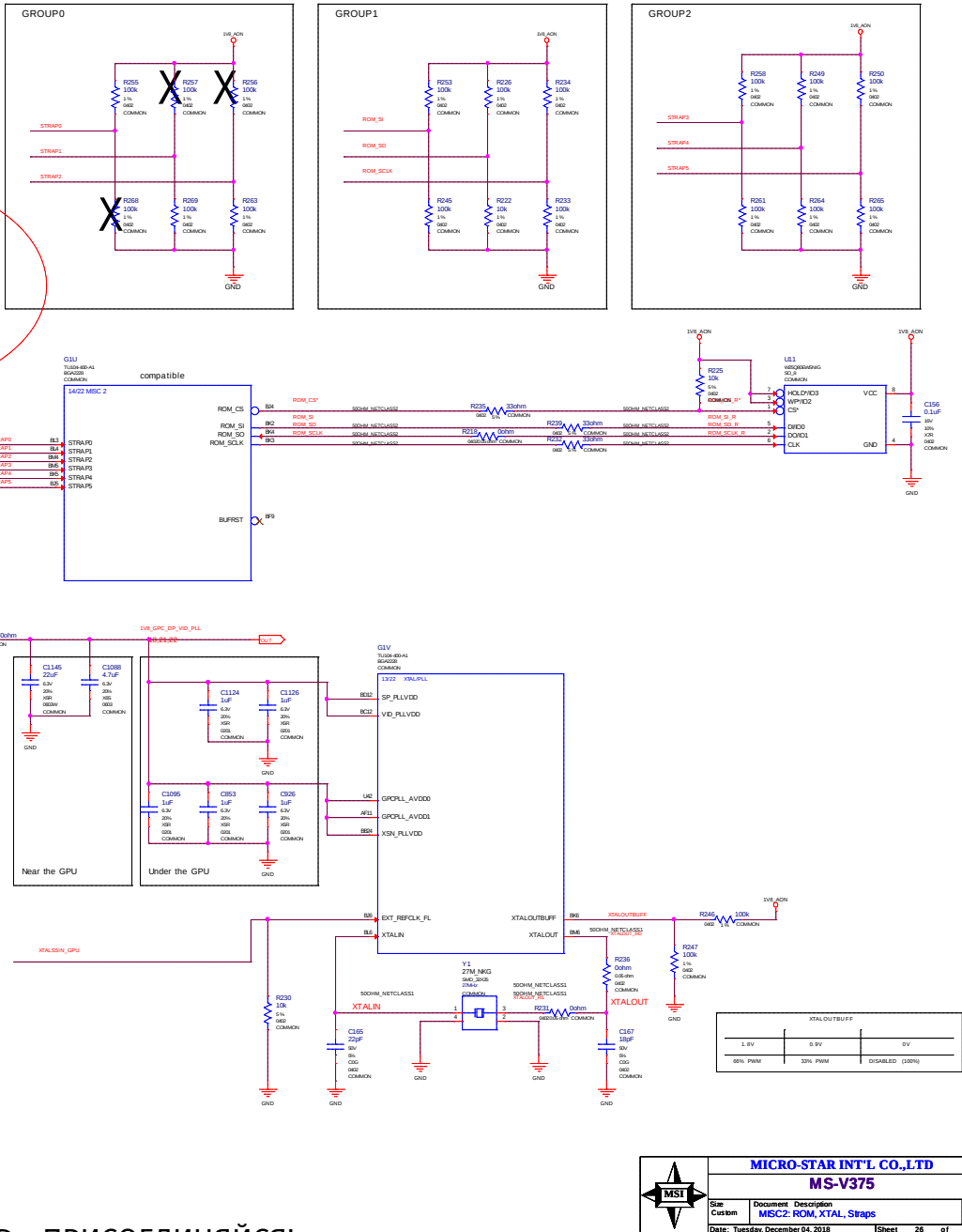
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

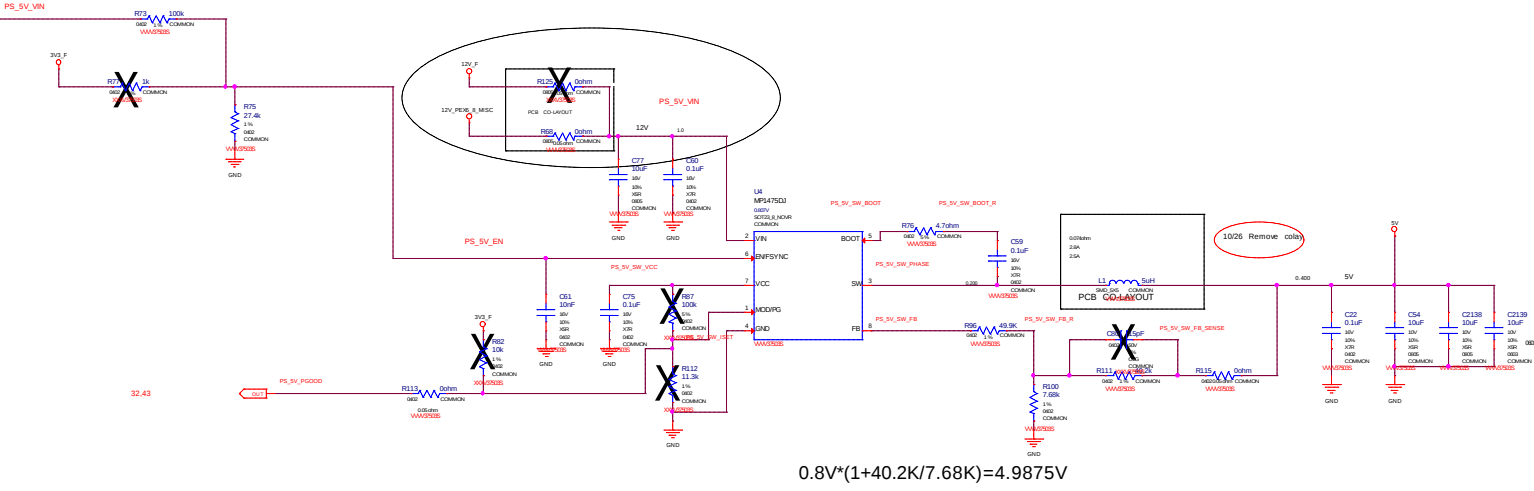
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

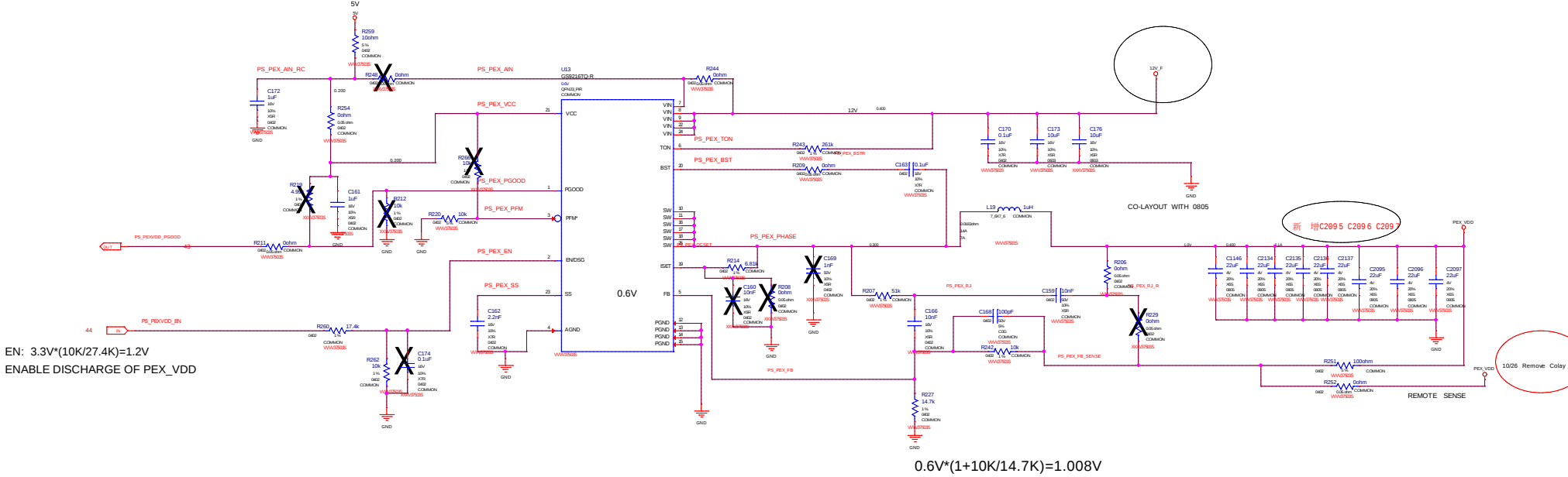
1:PCE_CFG LOW POWER
0:PCE_CFG HIGH POWER

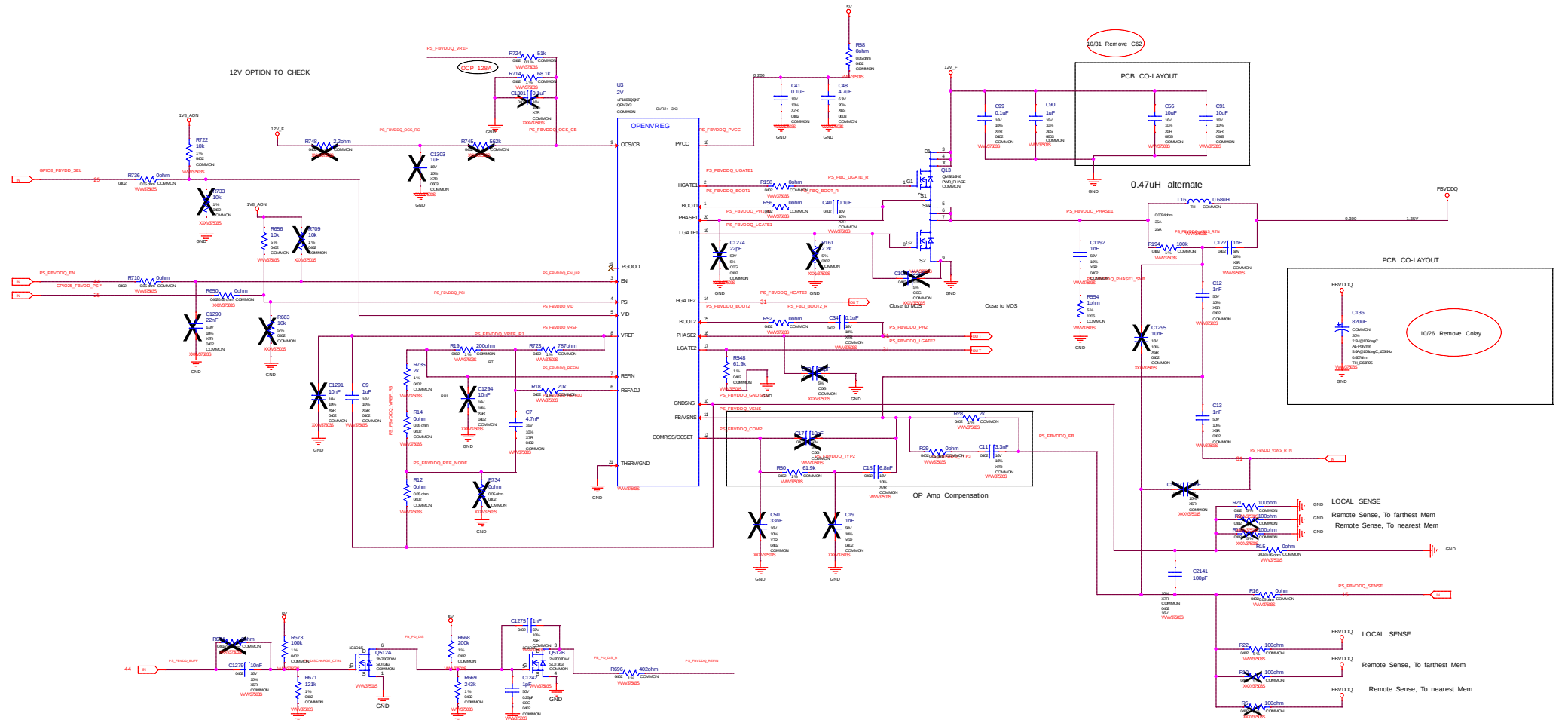
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

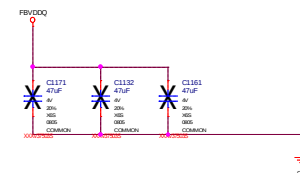
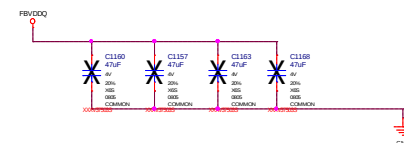
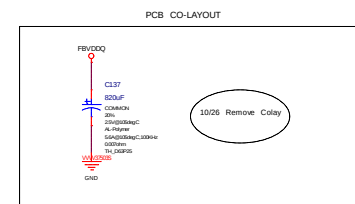
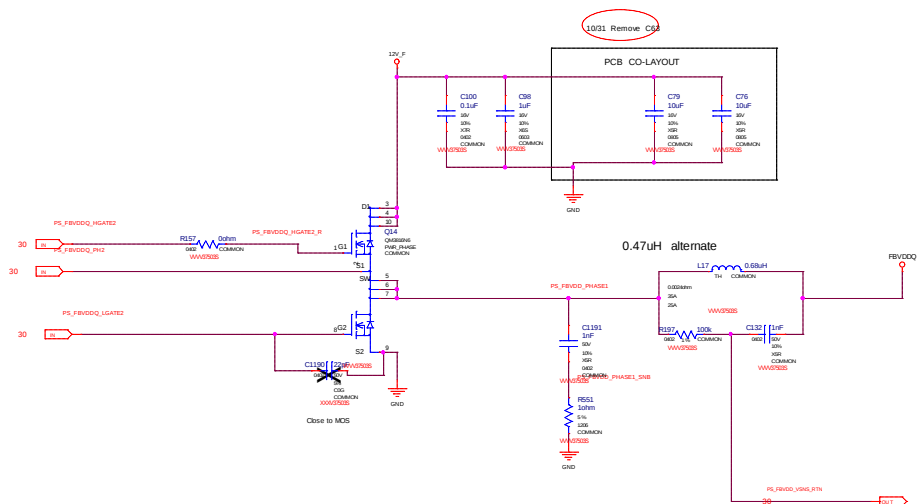


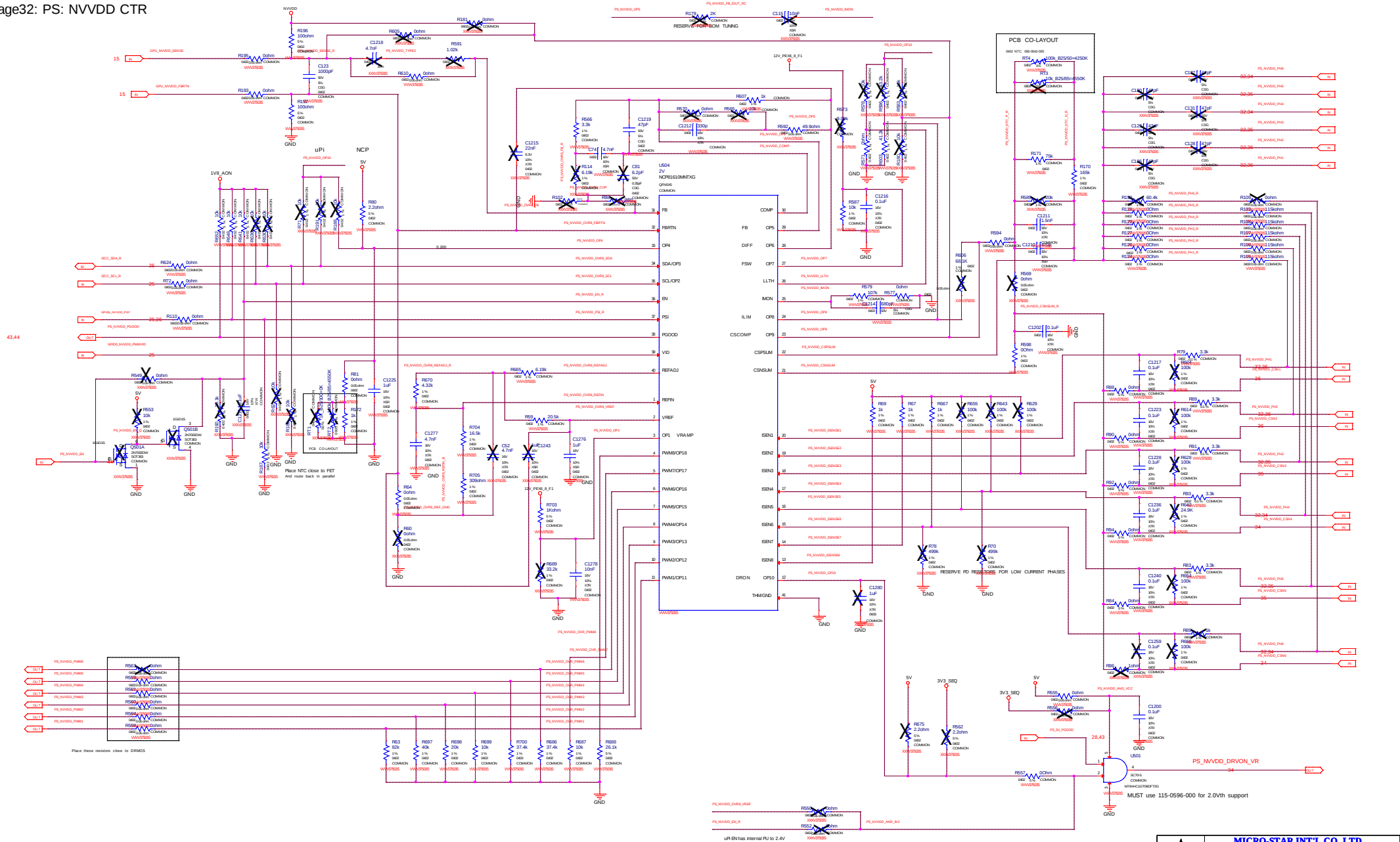


PEX Switcher









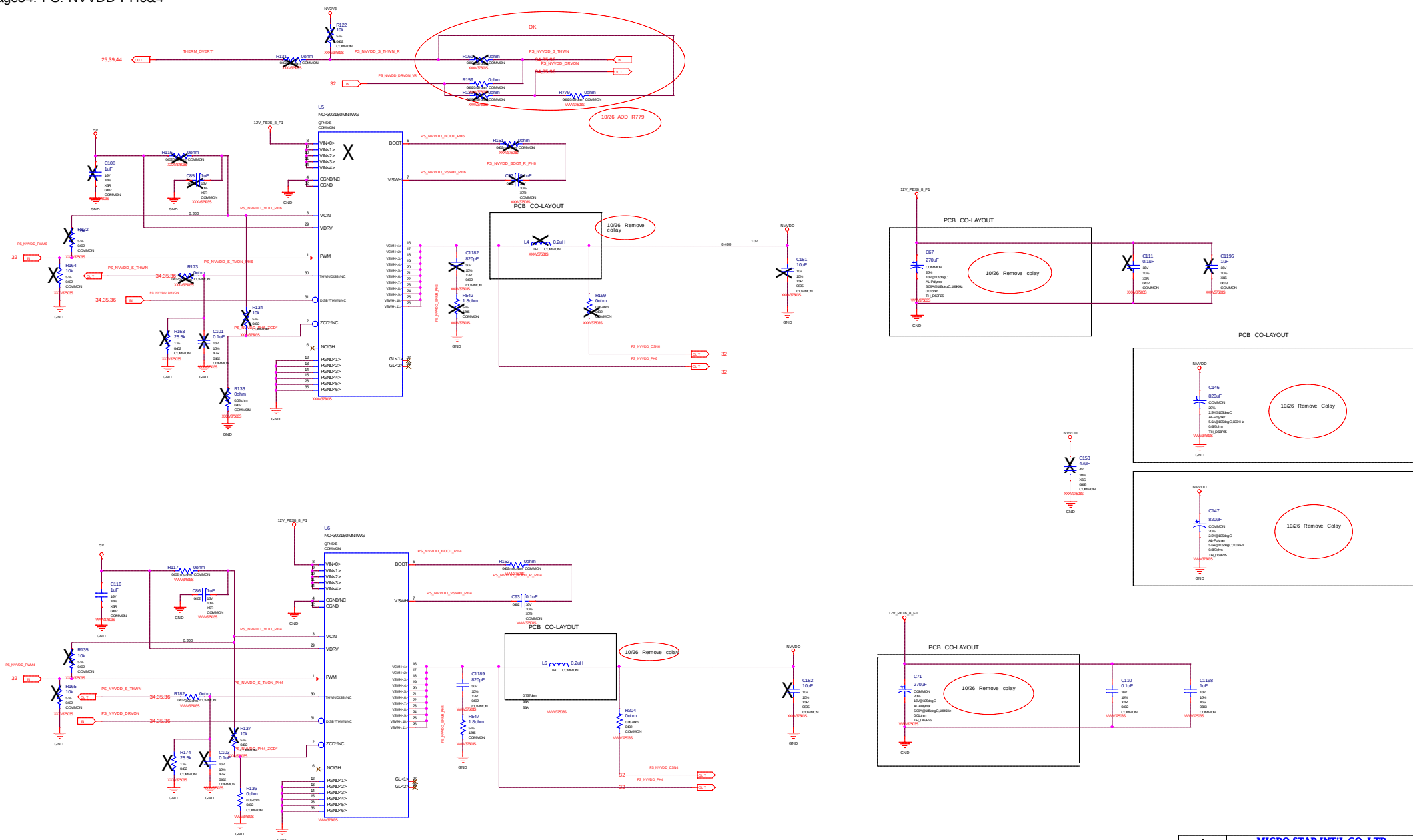
DROP OVR3i SOLUTION

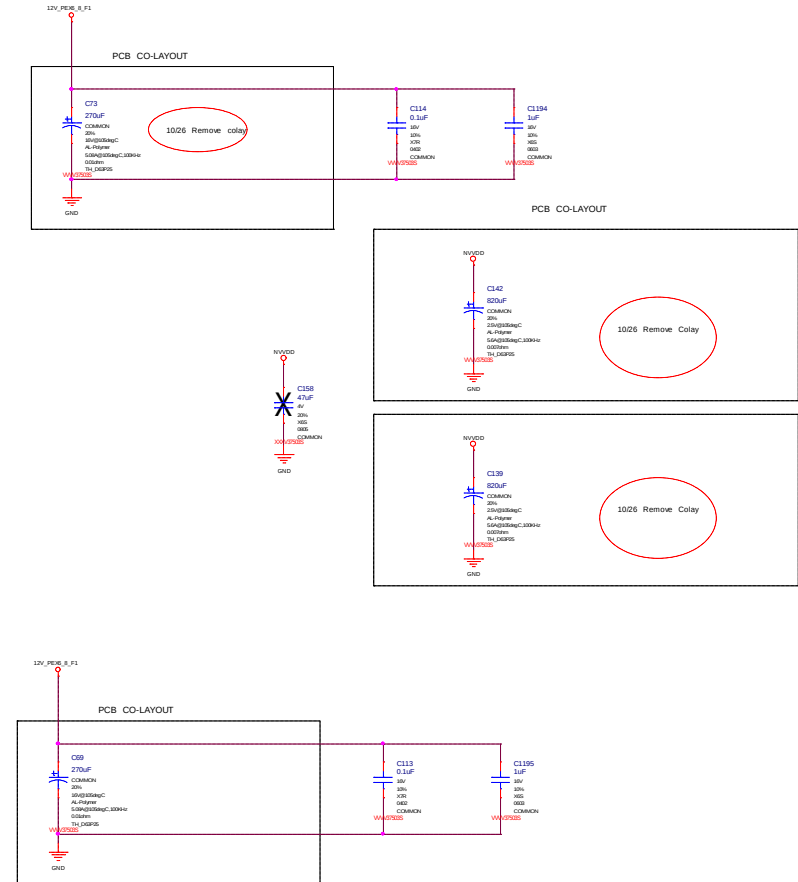
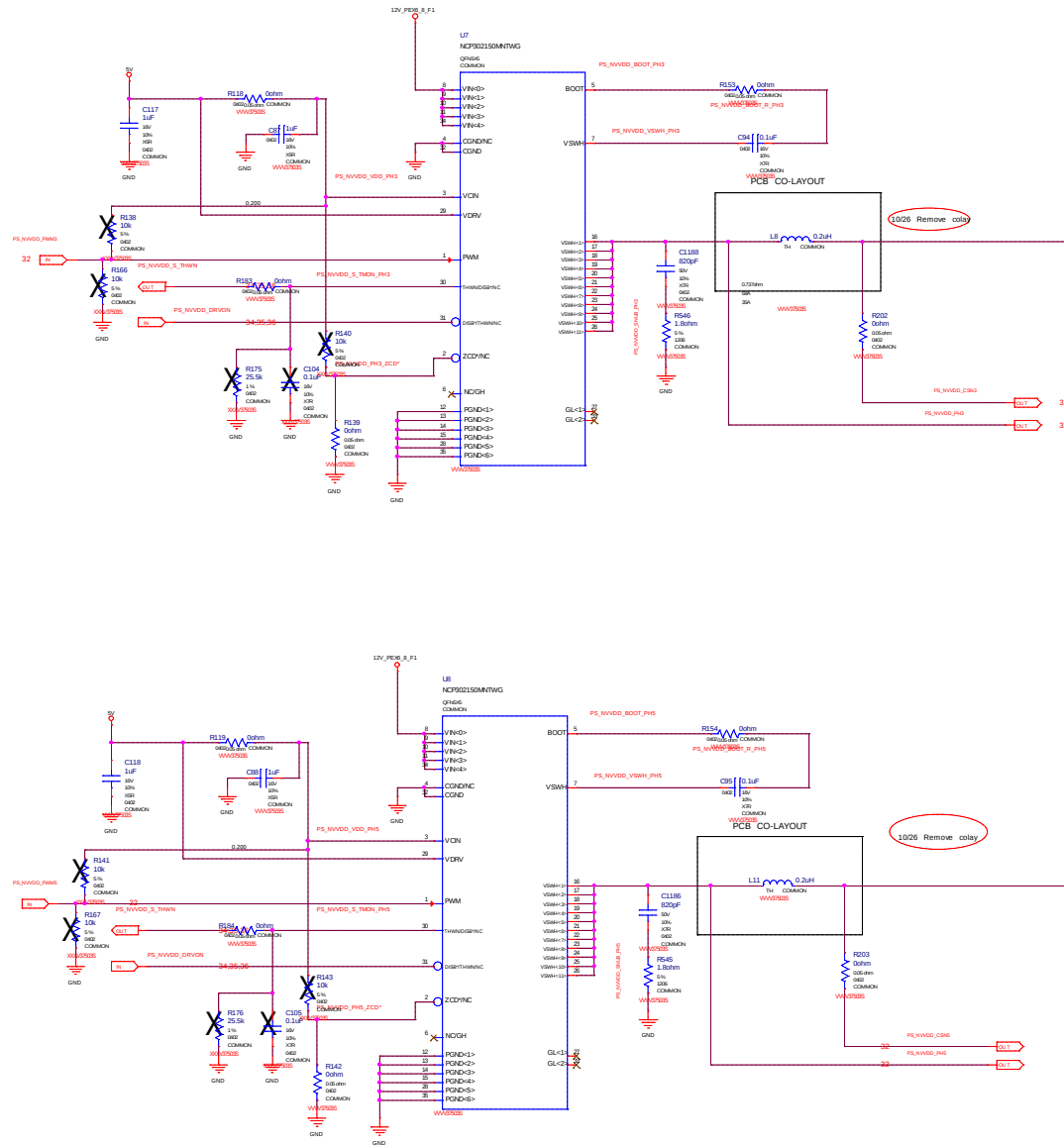


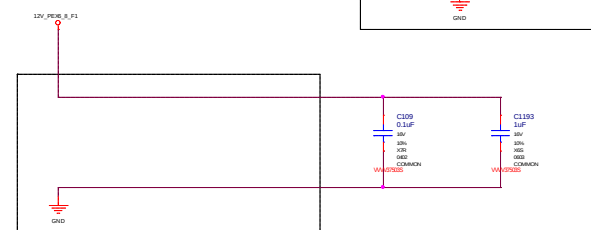
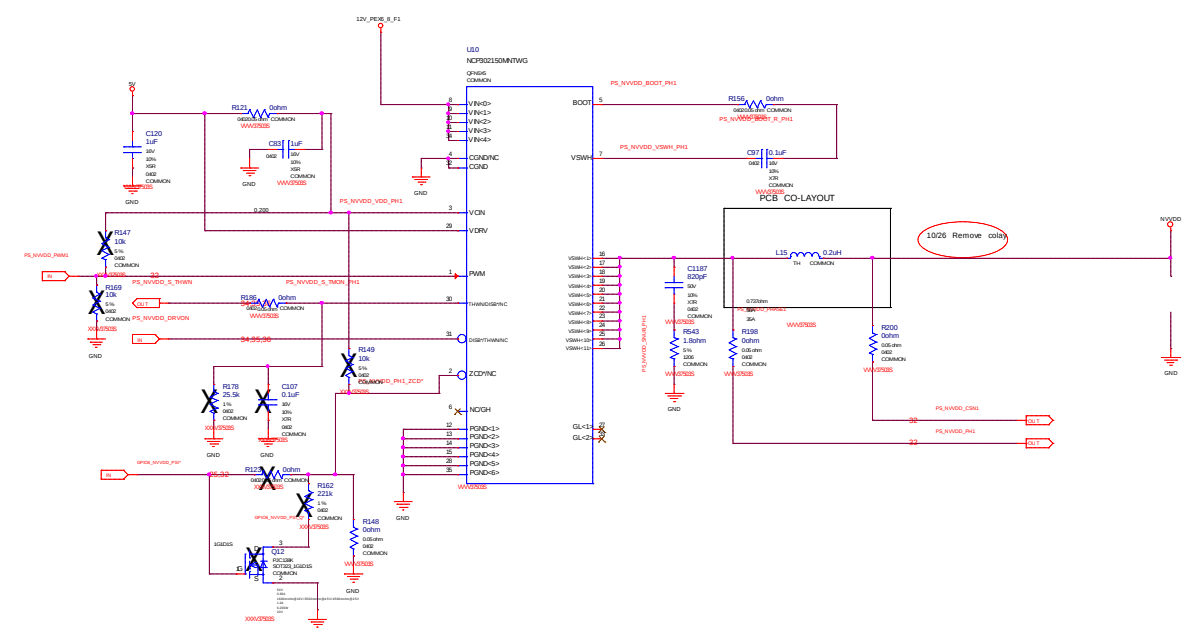
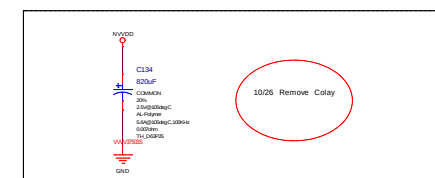
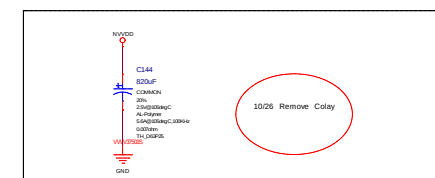
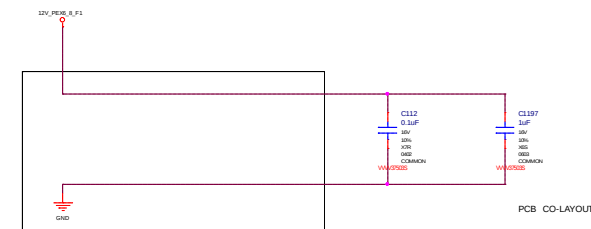
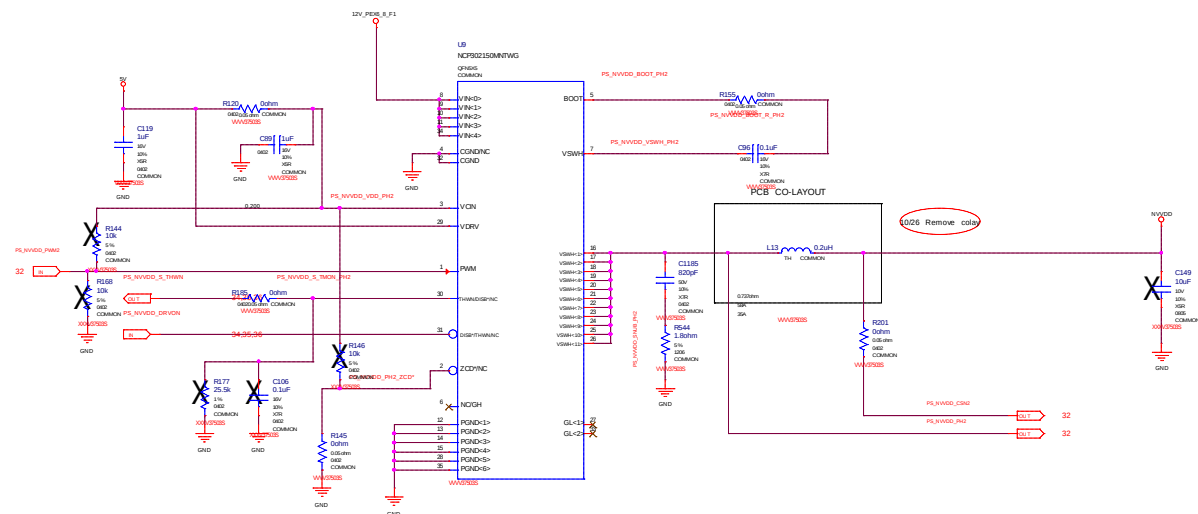
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Size	Document	Description	Rev
Custom	PS: NVVDD CTR OVR3i		2.0
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Size	Document Description	Rev
Custom	NVDD PH2&1	2.0
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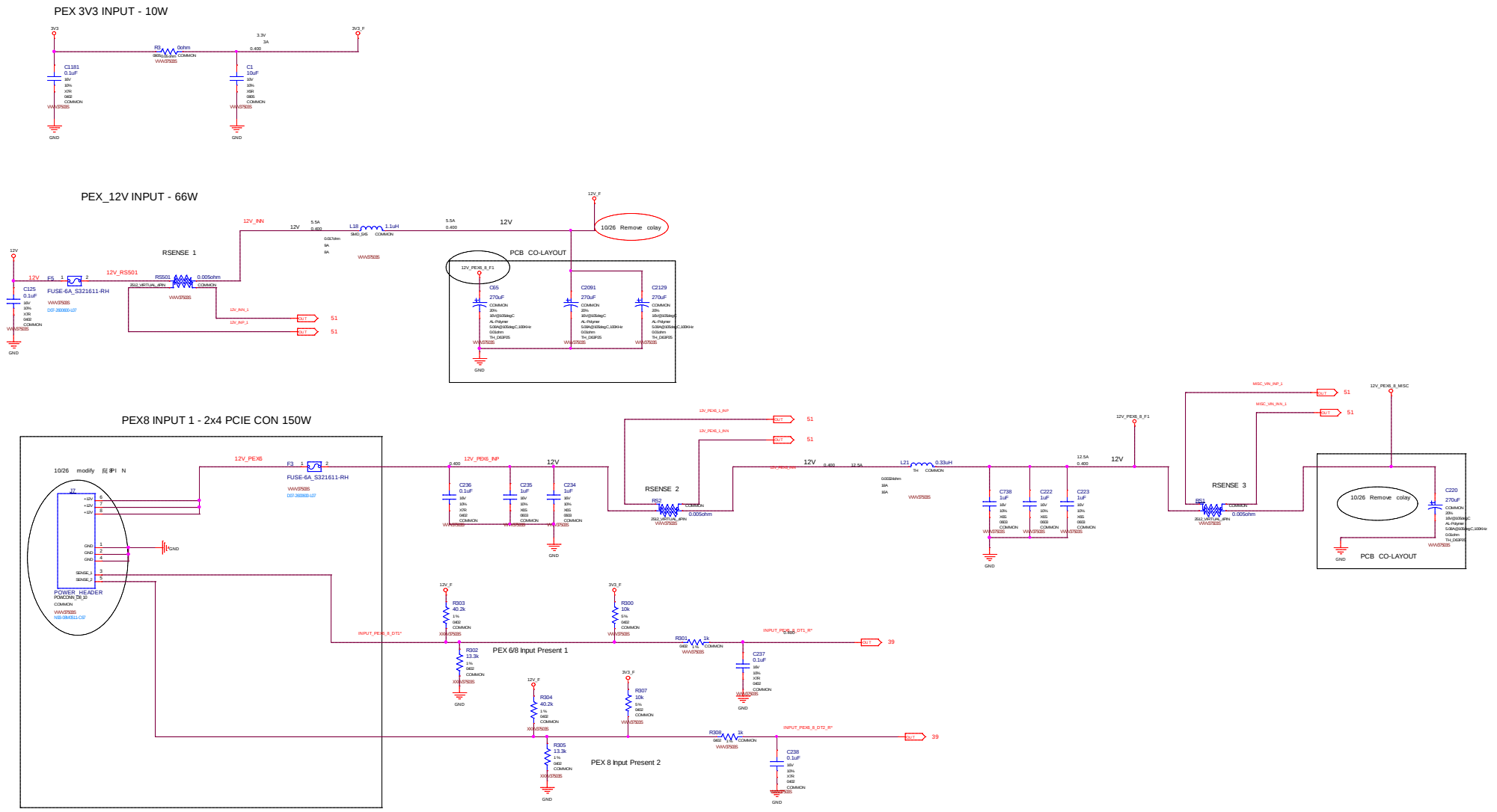
DELETE RAIL BALANCE CIRCUIT

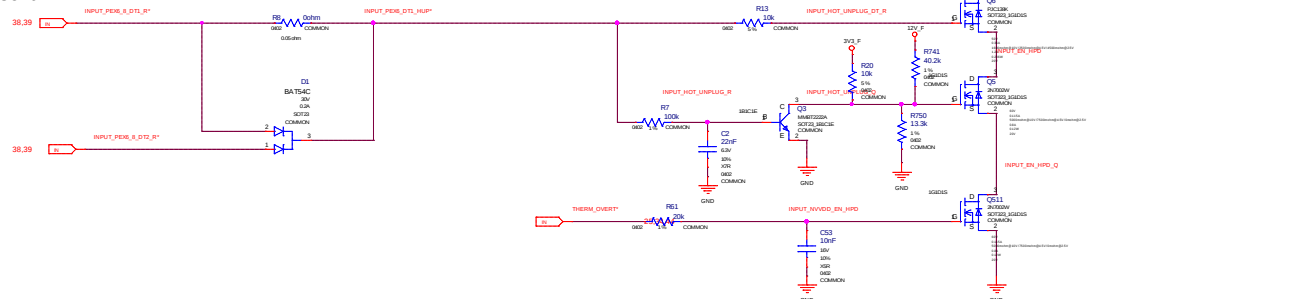


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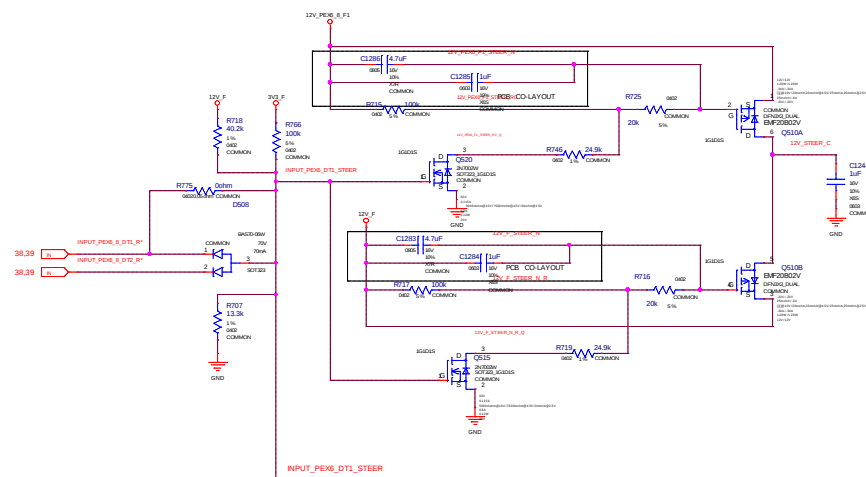
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Site	Document	Description	Rev
Custom	Input Power Balancing Switcher		2.0
Date: Tuesday, December 24, 2018			Sheet 37 of 52





GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



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1

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5



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Size	Document	Description	Rev
Custom	BUCKBOOST		2.0
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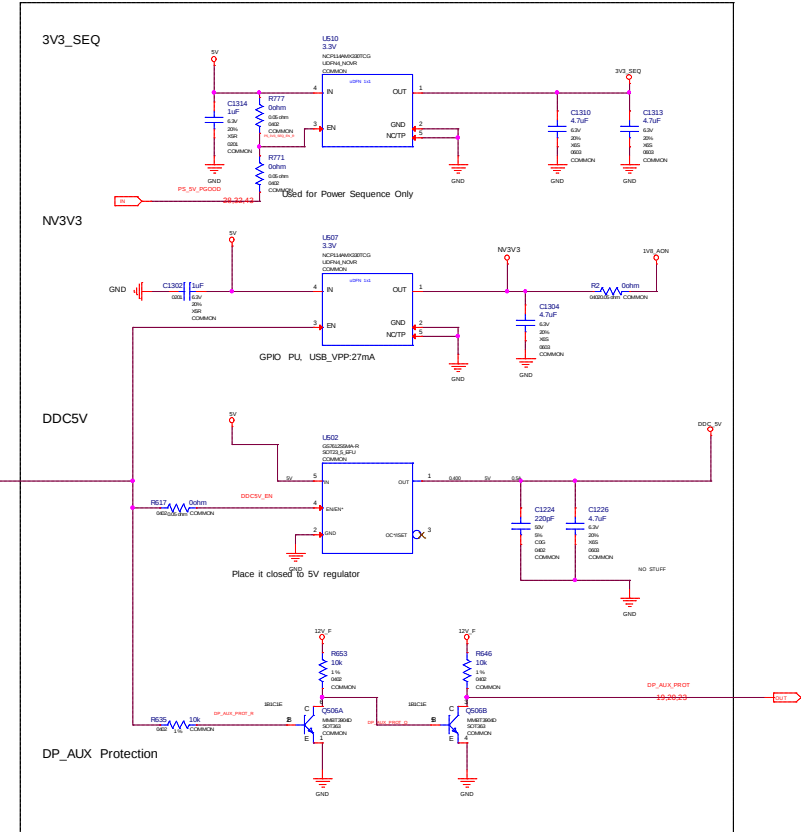
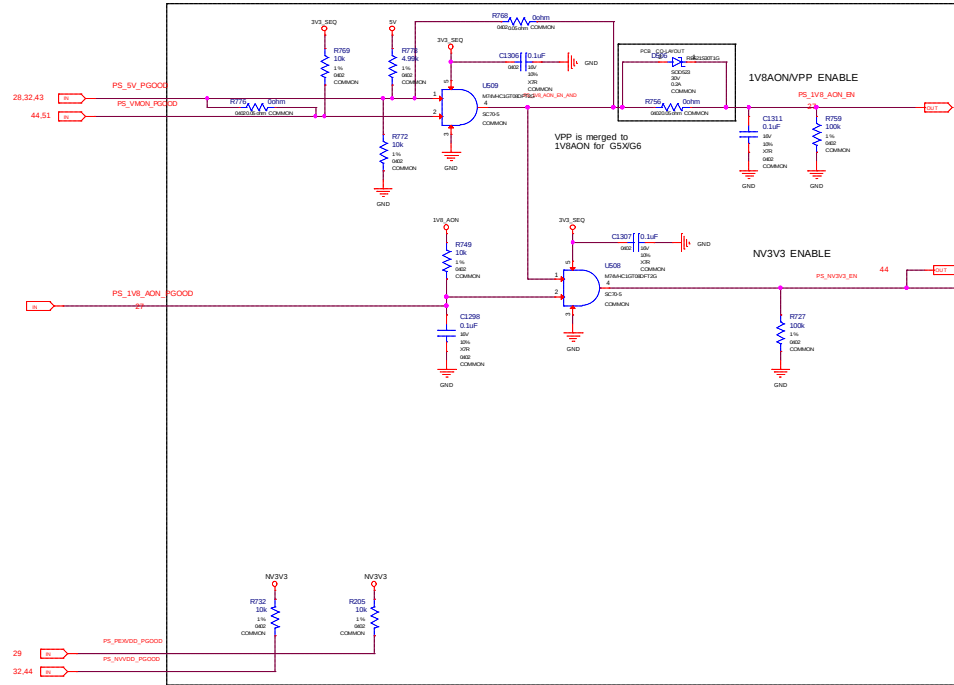
Site	Document	Description	Rev
Custom	PP/C		2.0
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Size	Document	Description	Rev
Custom	12V & 3V3_A SWITCHER		2.0
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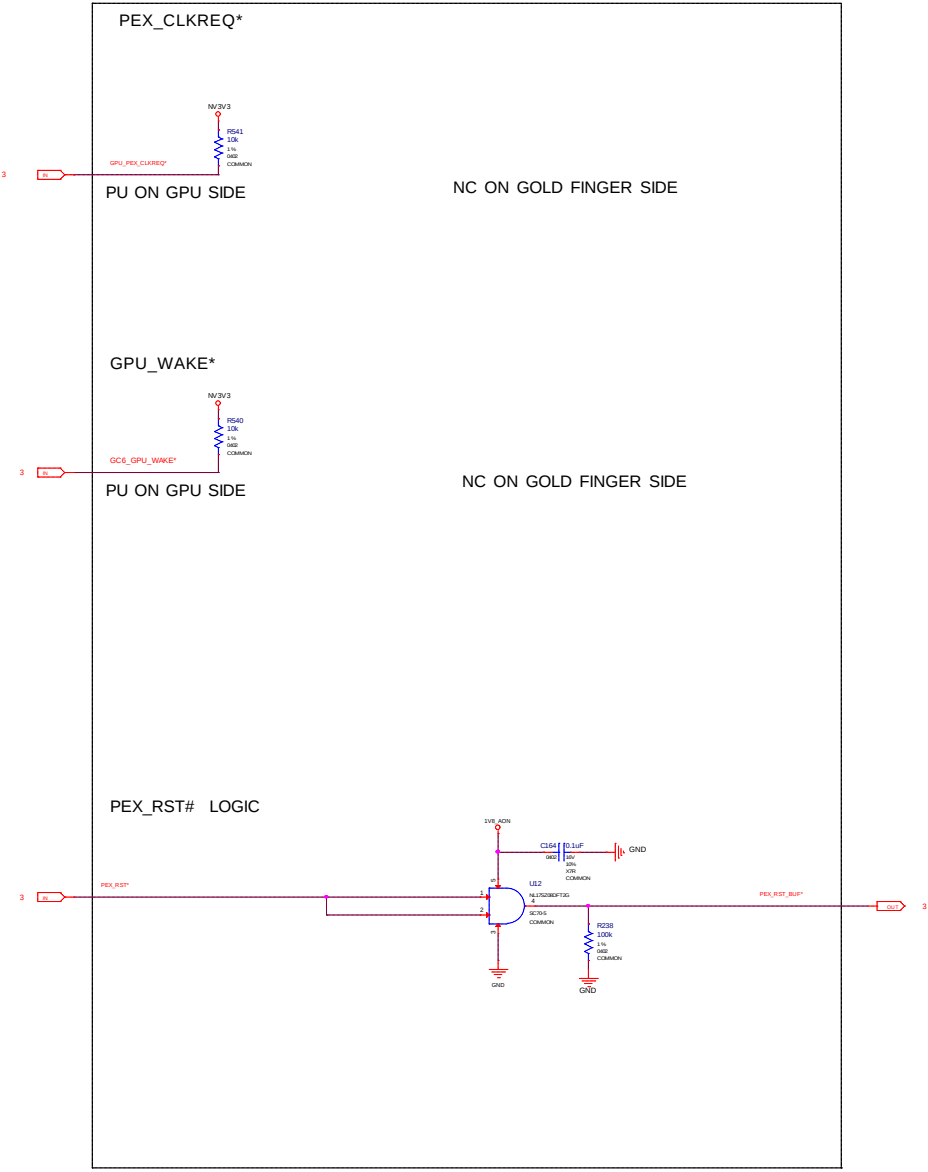
Size	Document	Description	Rev
Custom	SEQUENCE:Voltage	Monitor	2.0
Date: Tuesday, December 24, 2018			Sheet 45 of 52



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Size	Document	Description	Rev
Custom	SEQUENCE:Discharge		2.0
Date: Tuesday, December 24, 2018			Sheet 46 of 52



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Doc	Document Description	Rev
Custom	SEQUENCE:MISC	2.0
Date:	Tuesday, December 24, 2016	Sheet 47 of 53

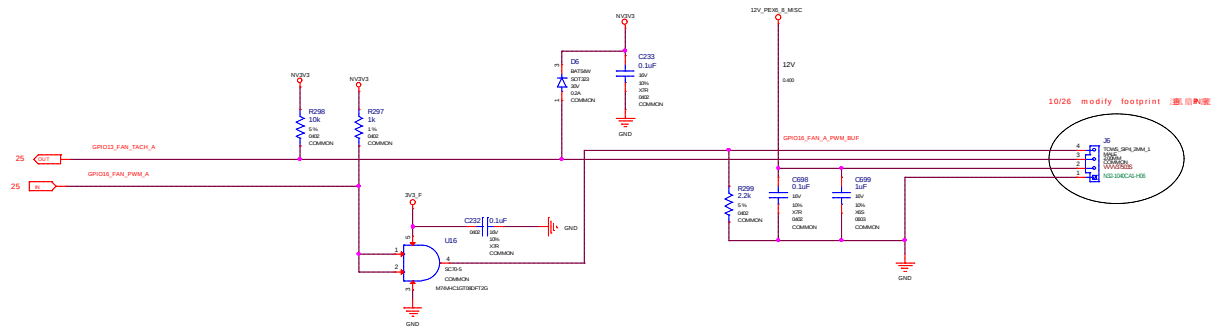


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Custom	LOGO LED		2.0
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BRK1
BRK1_DUAL_ATX_27AR_PG155
ATX_2X_DP
COMMON

MECH. MOUNTING ALL

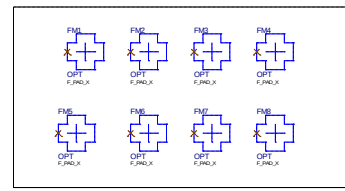
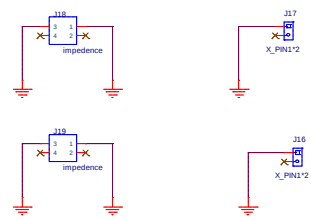
1

2

GND

The diagram shows a 12V battery connected to a common ground and a common positive rail. Ten MCUs are connected to this common positive rail through 1 Ohm DCRs. The MCUs are labeled MC1-1 through MC1-10, each with a 5V VDDGND pin.

The diagram shows a 4-wire RTD circuit. A common wire (blue) connects all four RTD modules (MEC2-9, MEC2-10, MEC2-11, MEC2-12) to a common ground (GND). The other three wires (red, green, yellow) are connected to the RTD modules in a specific sequence: Red to MEC2-9 (1), MEC2-10 (2), MEC2-11 (3), MEC2-12 (4); Green to MEC2-9 (2), MEC2-10 (3), MEC2-11 (4), MEC2-12 (1); Yellow to MEC2-9 (3), MEC2-10 (4), MEC2-11 (1), MEC2-12 (2).





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Custom	PTC		2.0
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