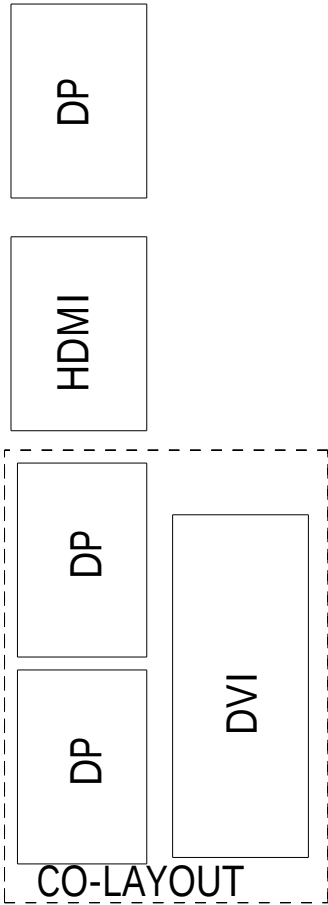
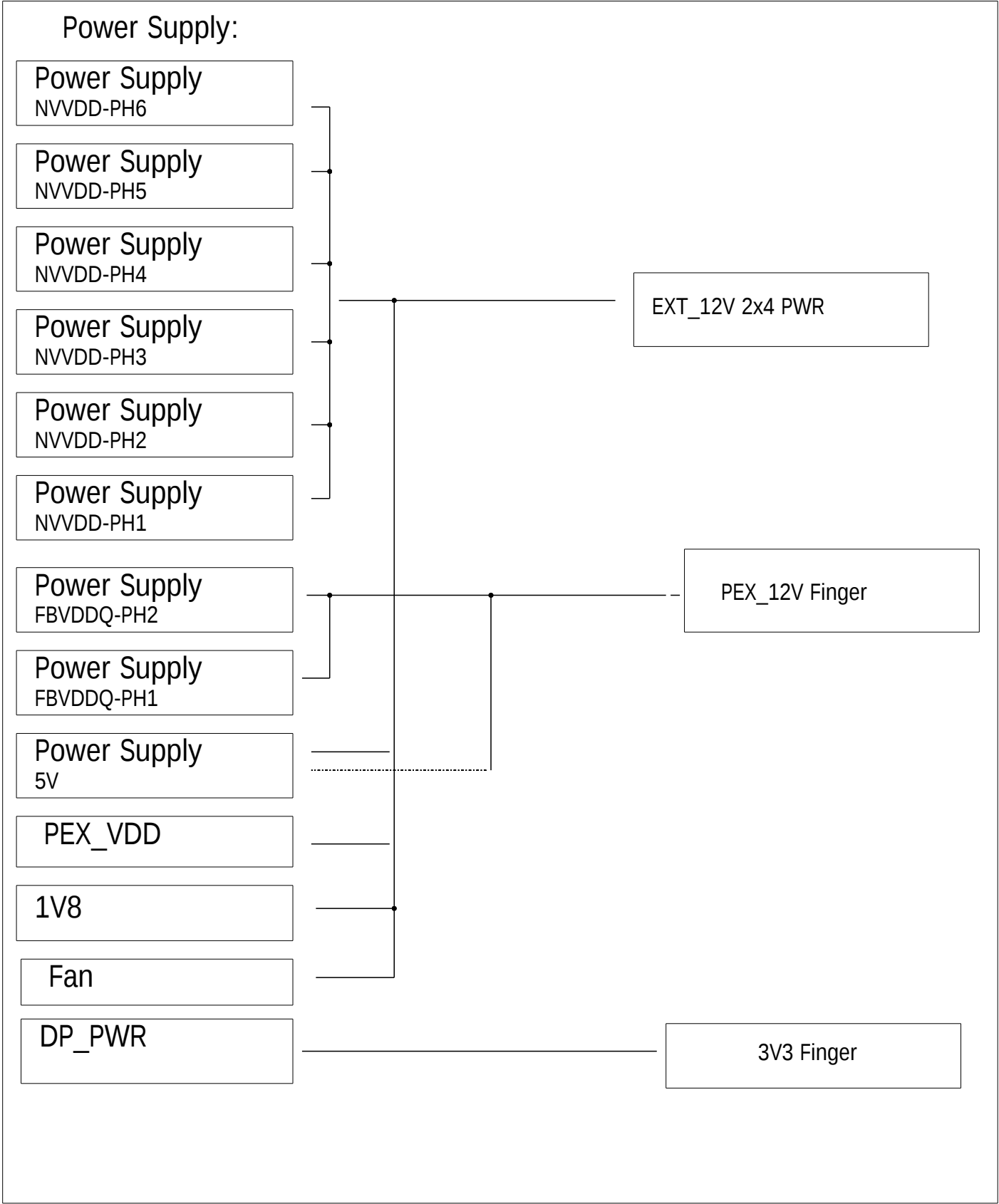
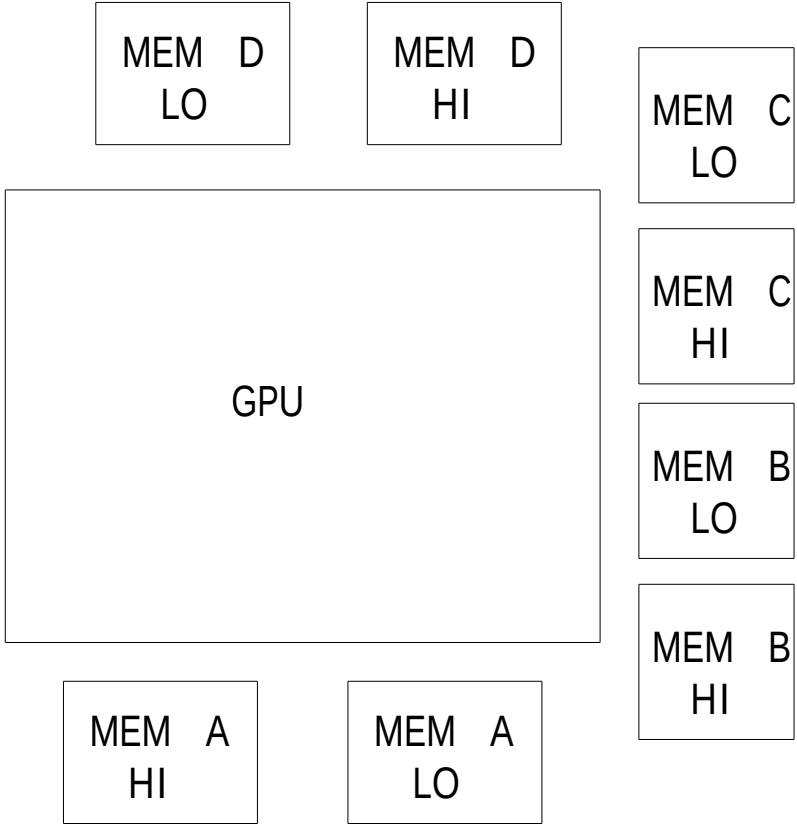
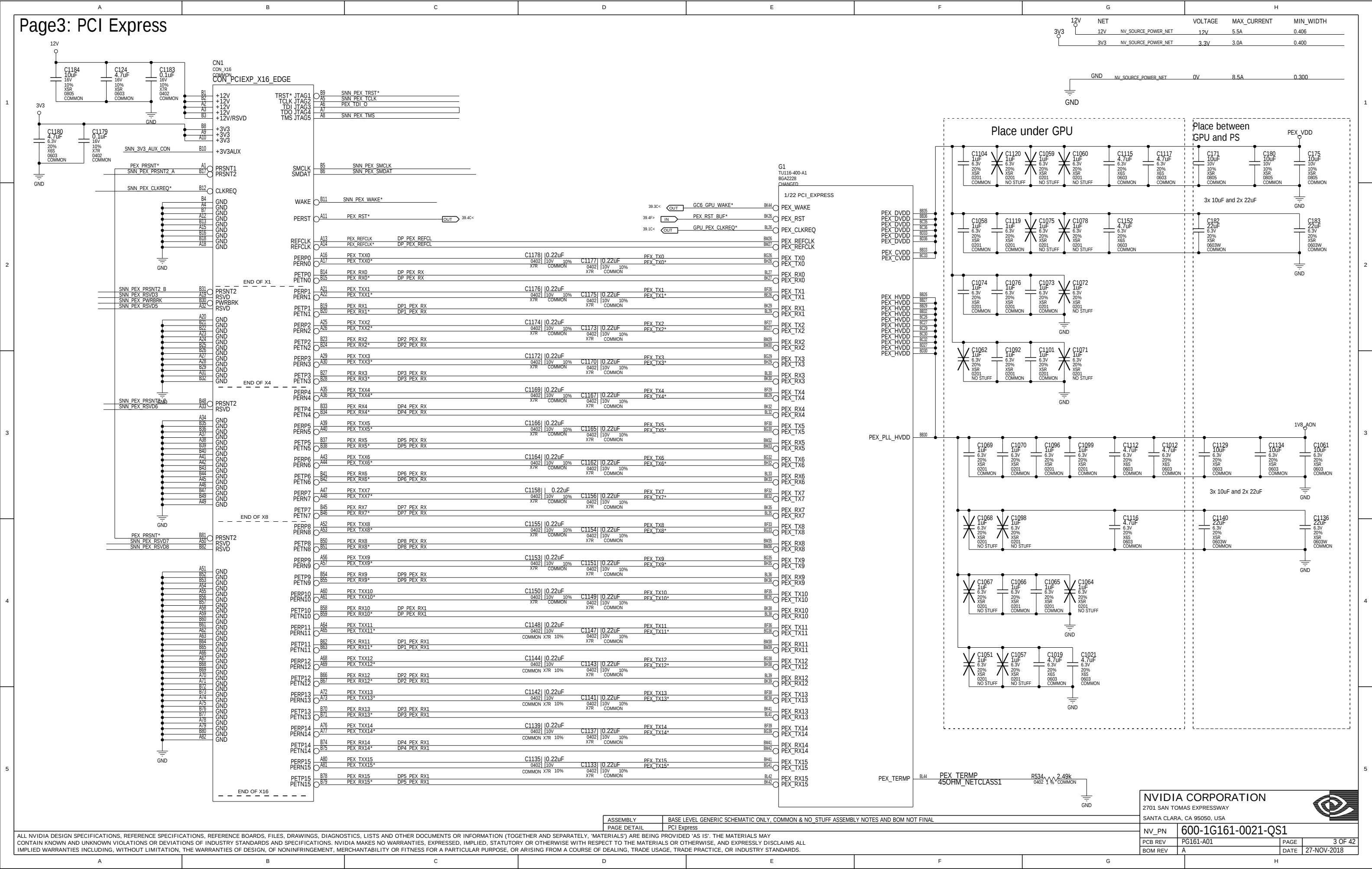


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	ASSEMBLY PAGE DETAIL BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL Table of Contents NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA NV_PN 600-1G161-0021-QS1 PCB REV PG161-A01 PAGE 1 OF 42 BOM REV A DATE 27-NOV-2018 ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.																																																																																																																																																																			
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600-1G161-0021-QS1

PCB REV

PG161-A01

BOM REV

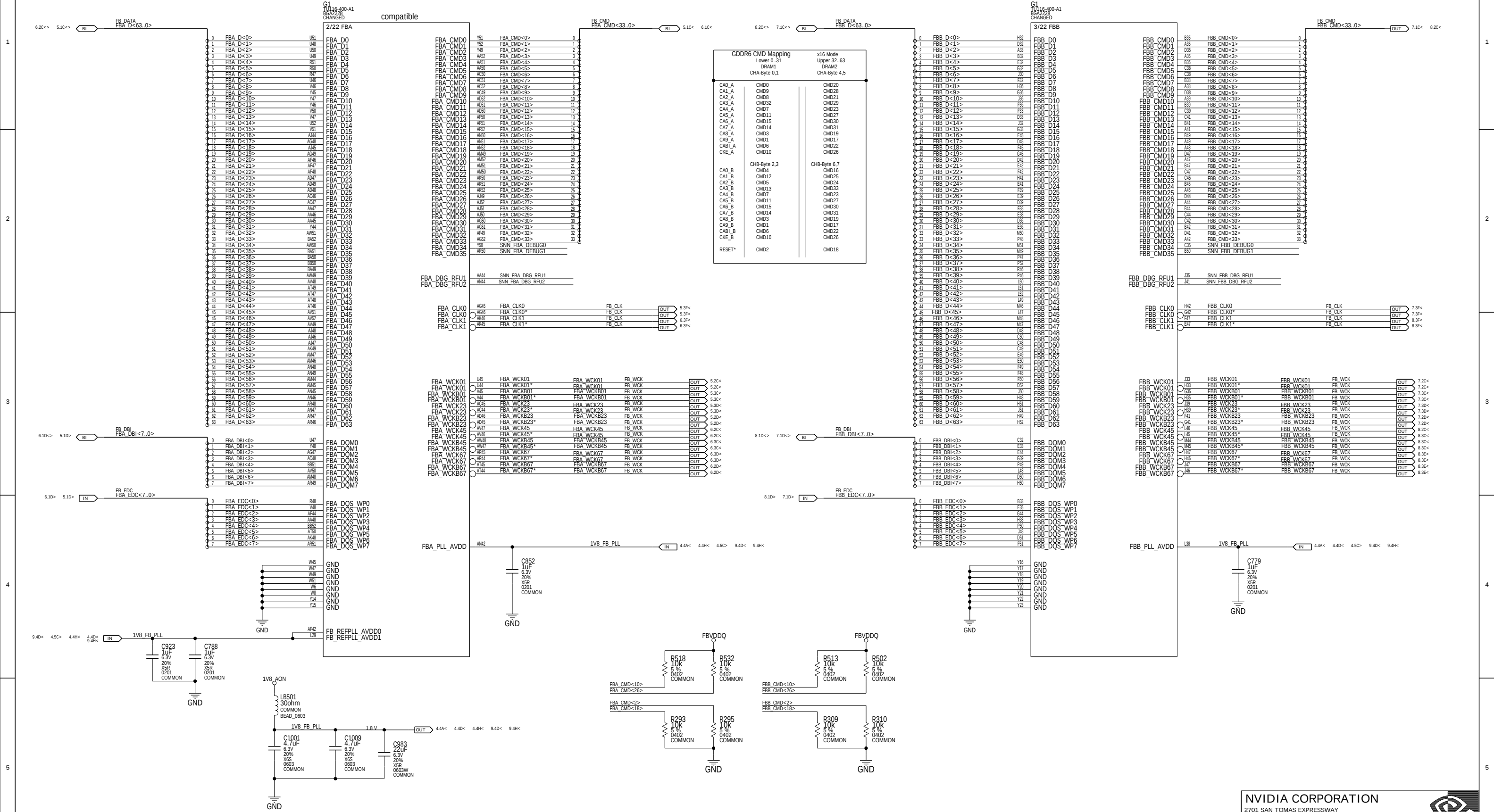
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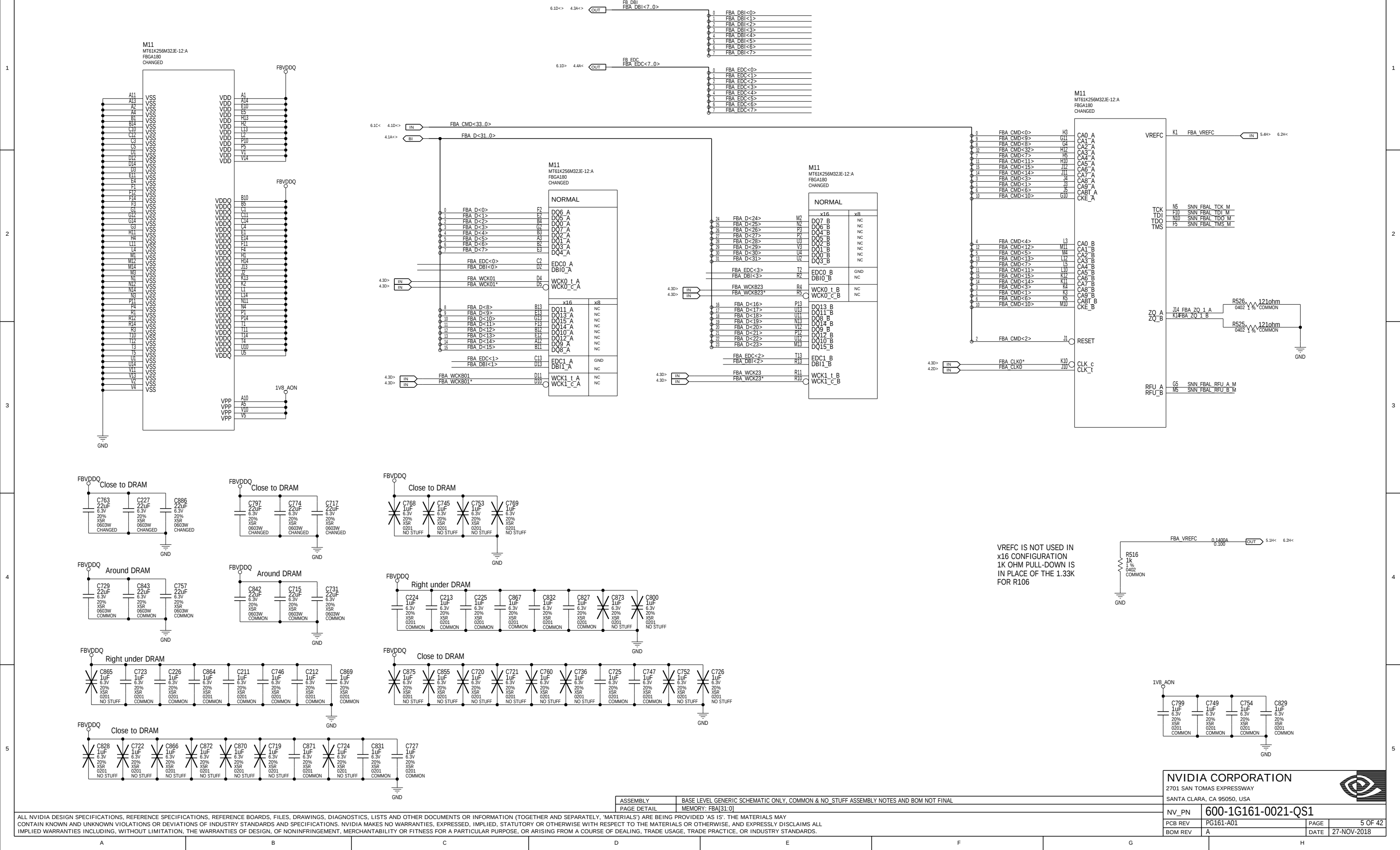
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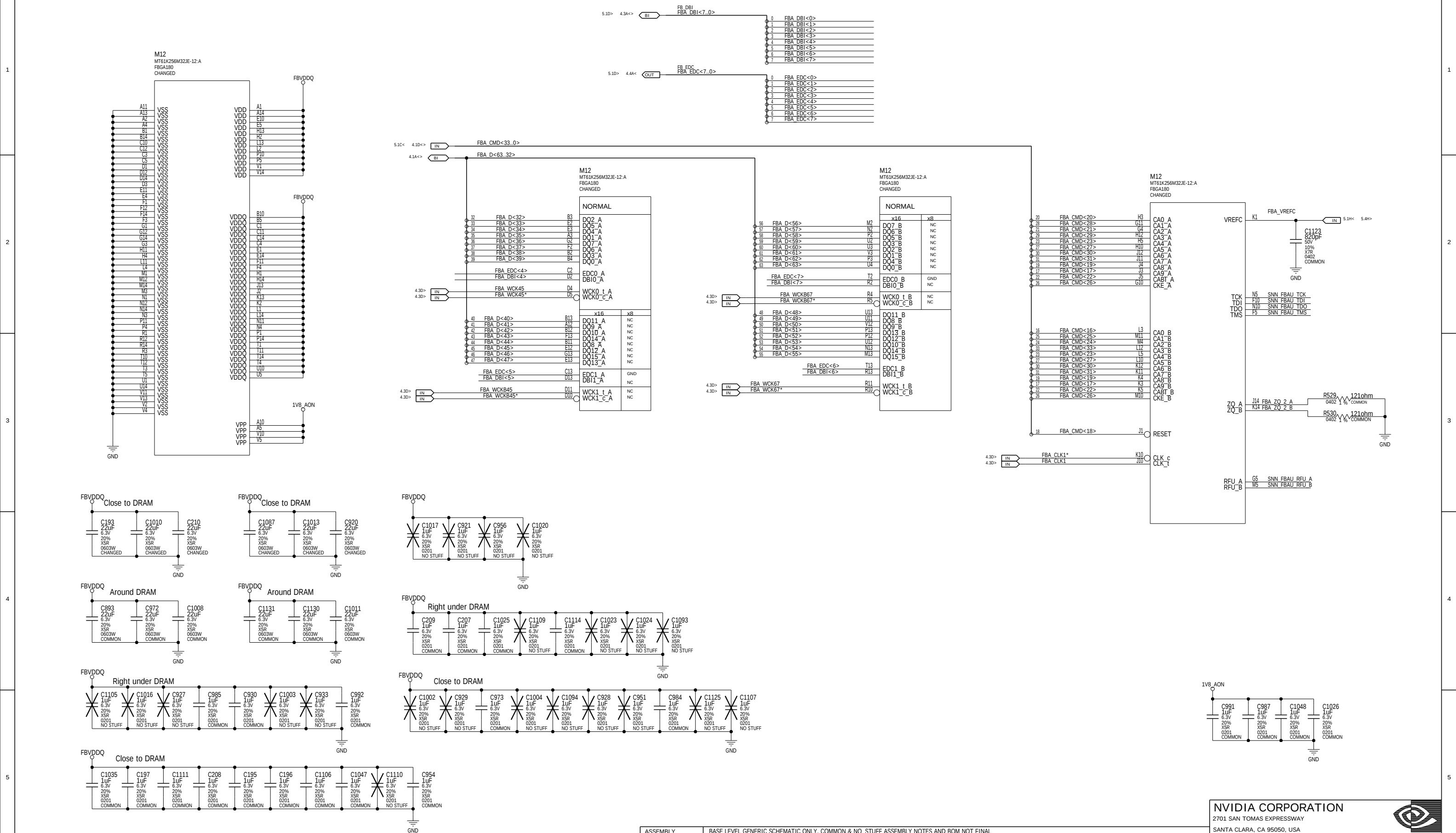
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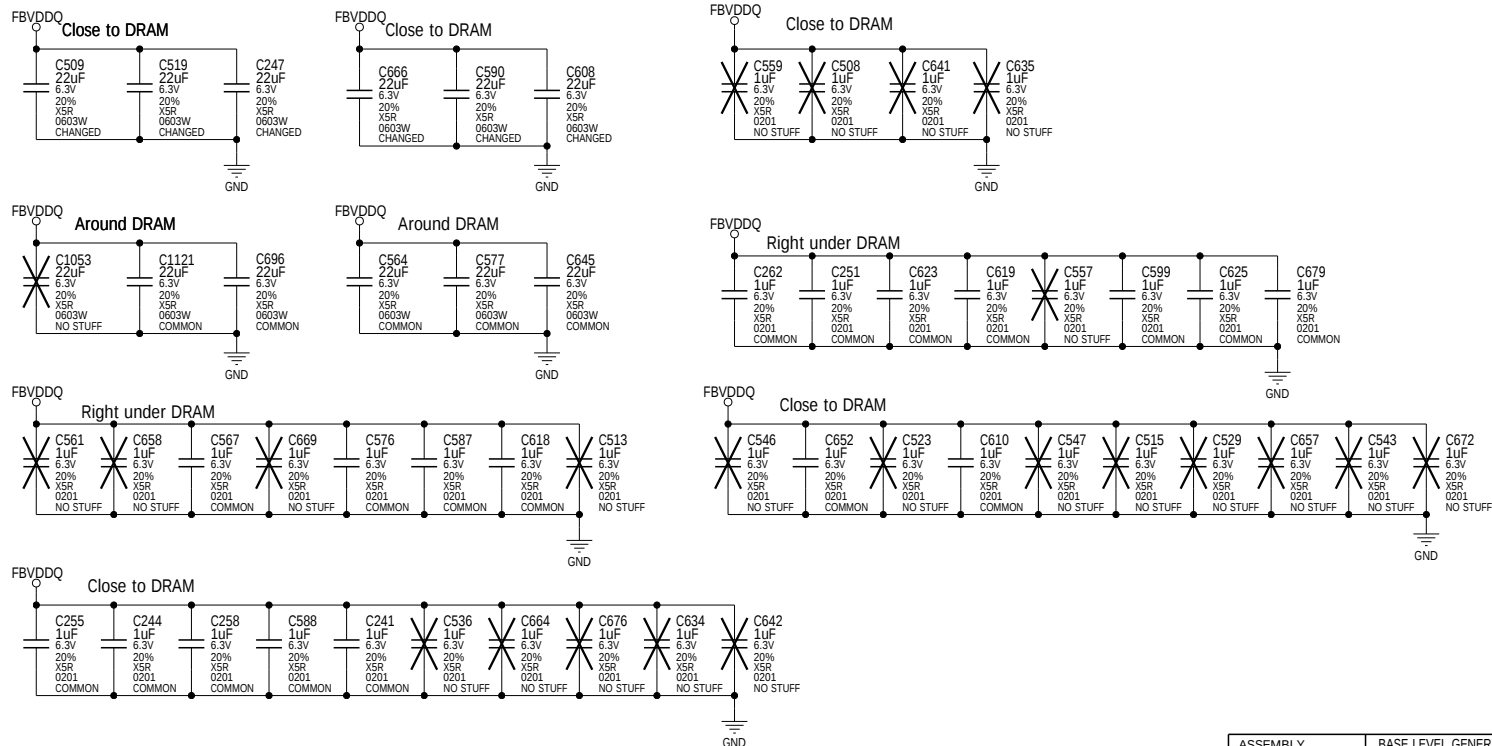
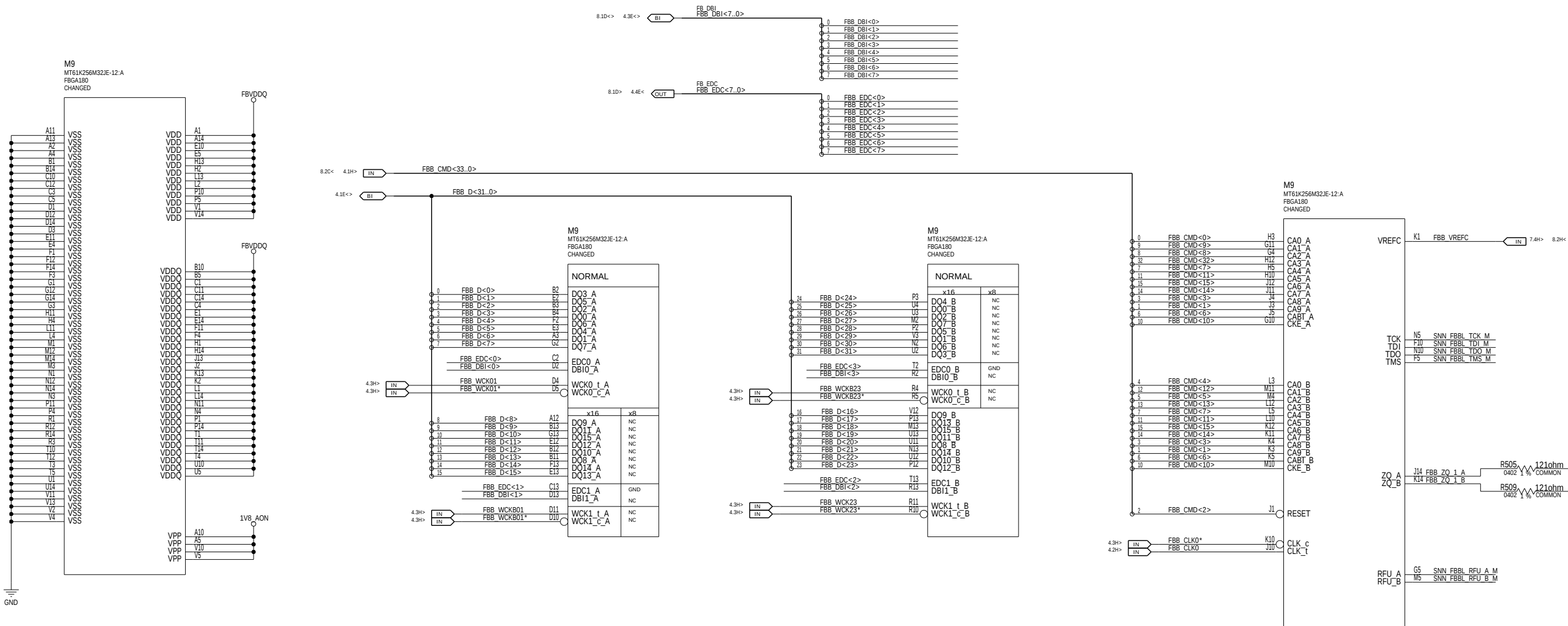
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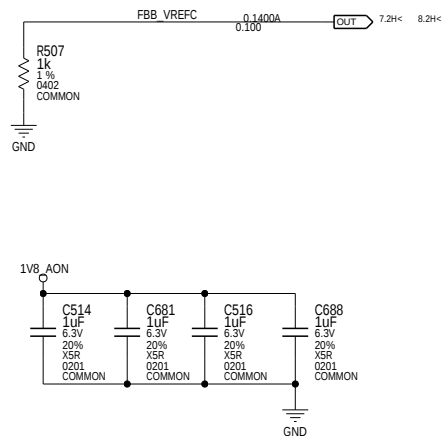
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PAGE DETAIL	MEMORY: FBA{63:32}	NV_PN	600-1G161-0021-QS1		
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VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R104



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2701 SAN TOMAS EXPRESSWAY

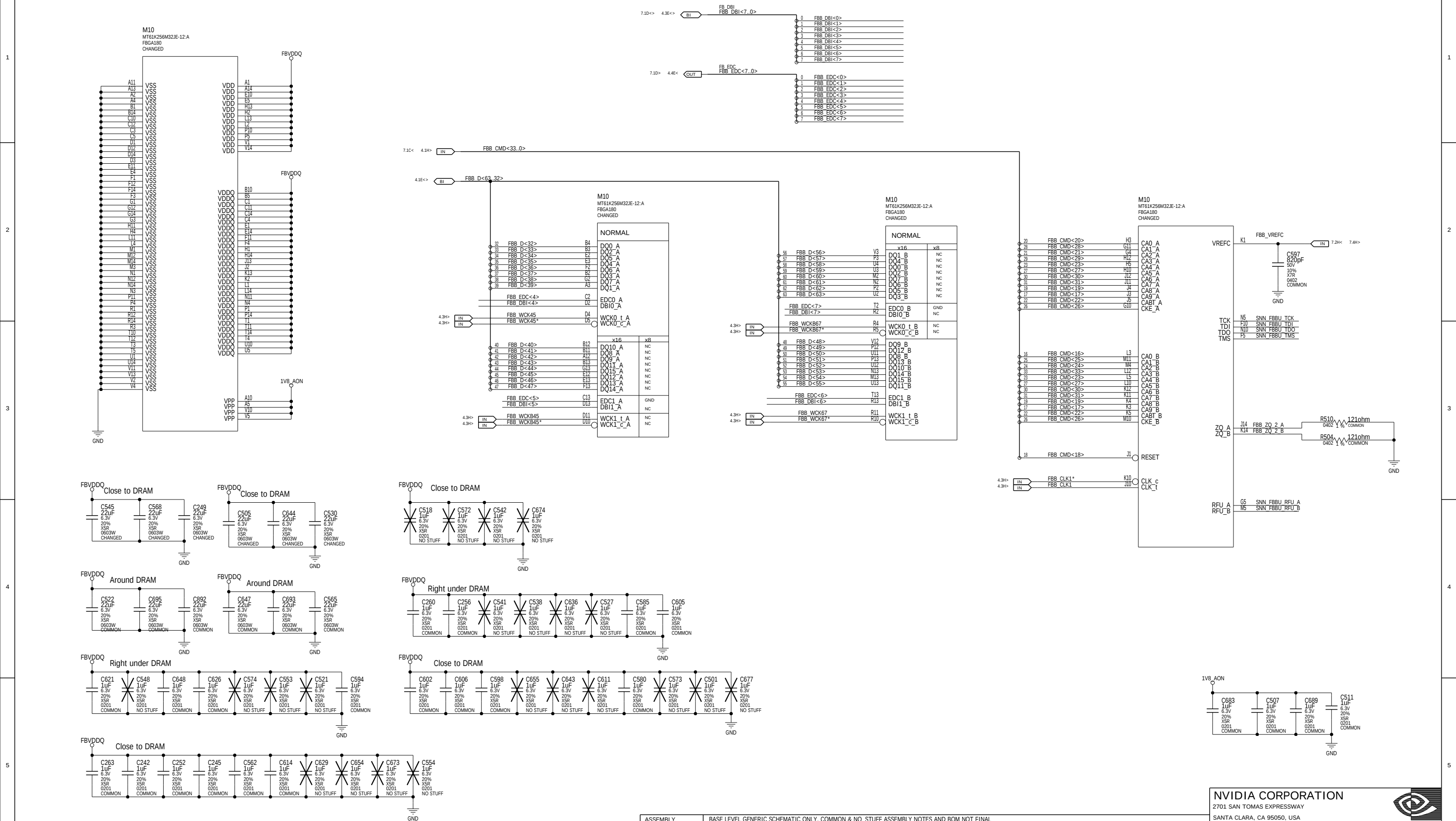
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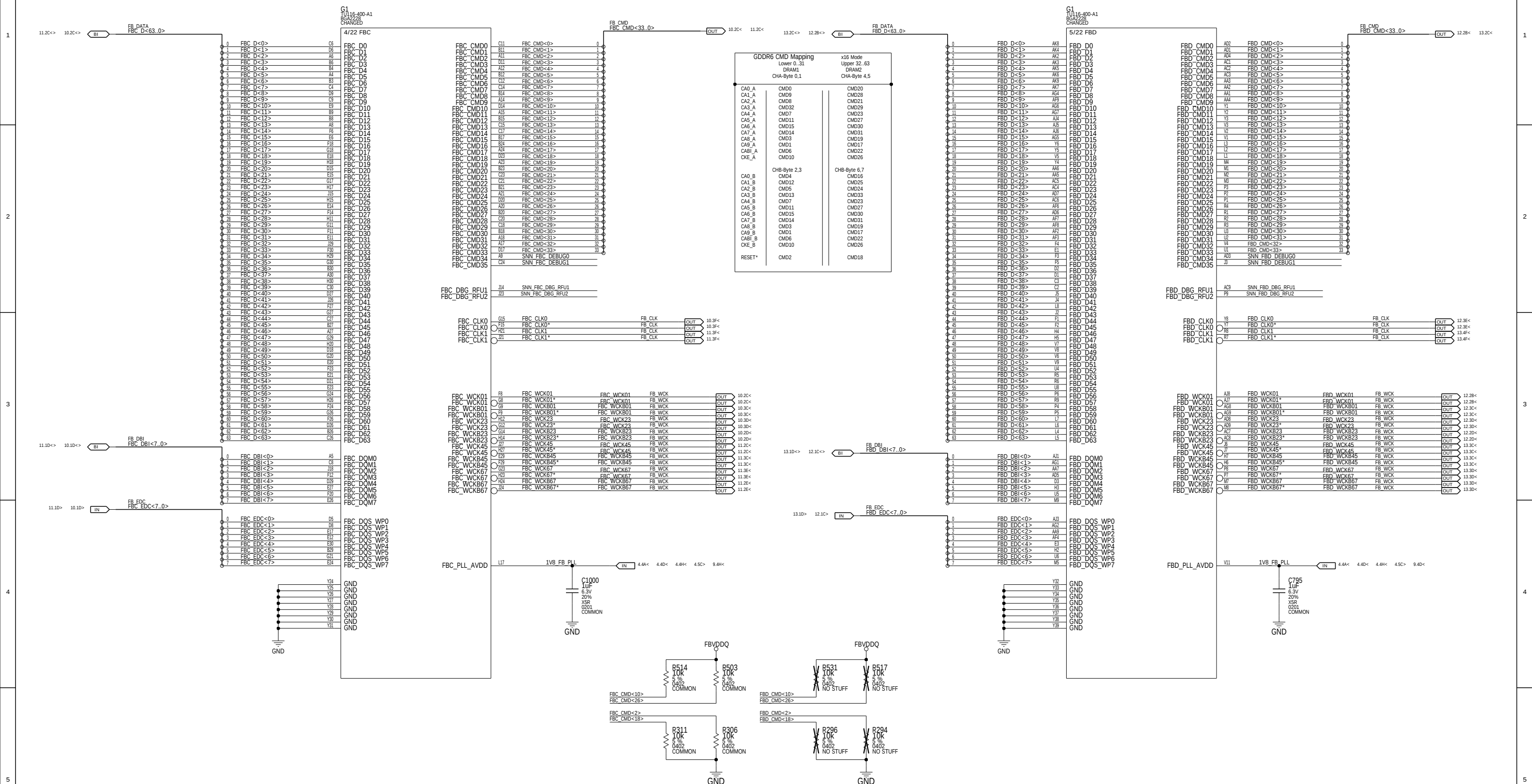
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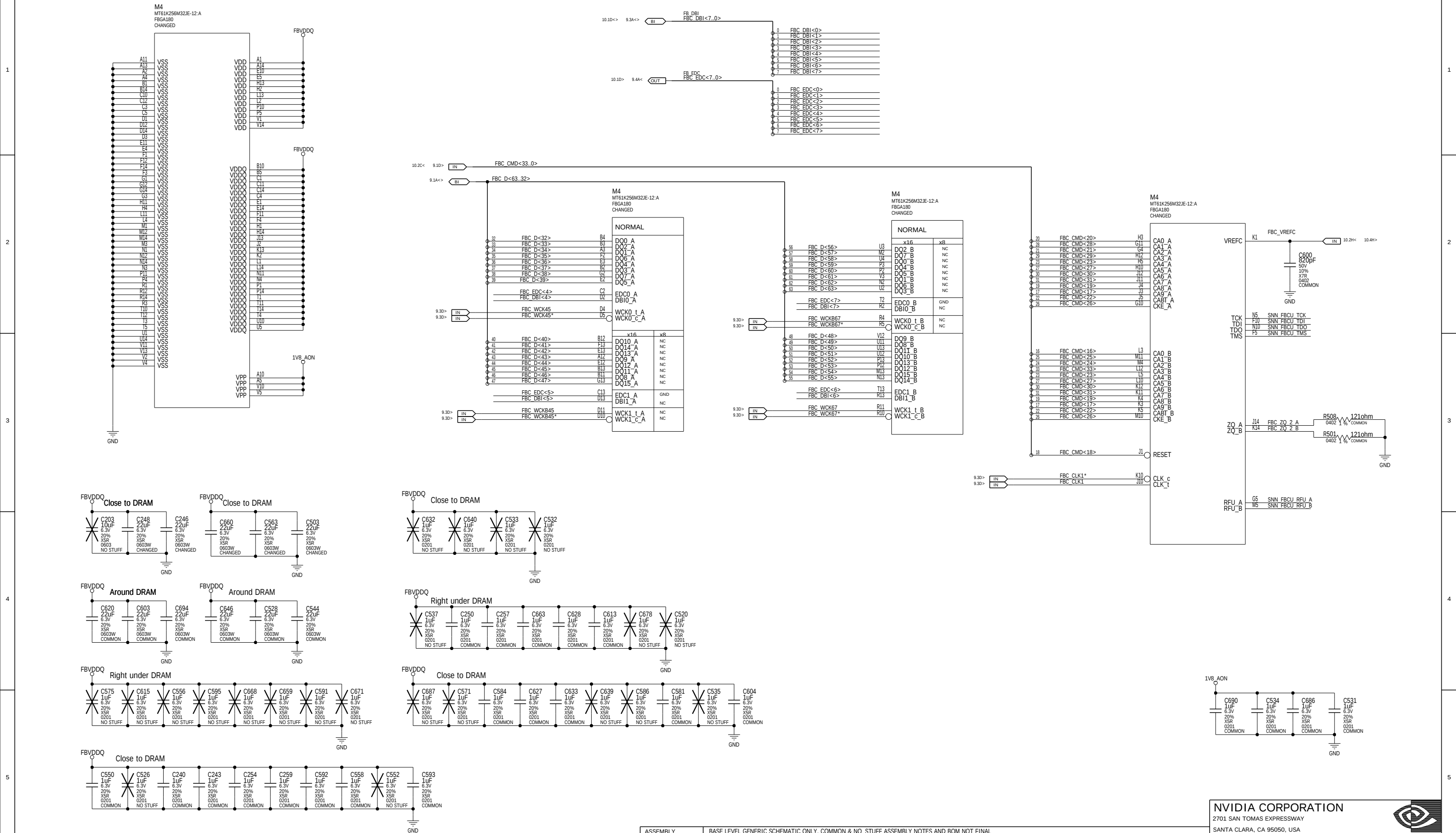


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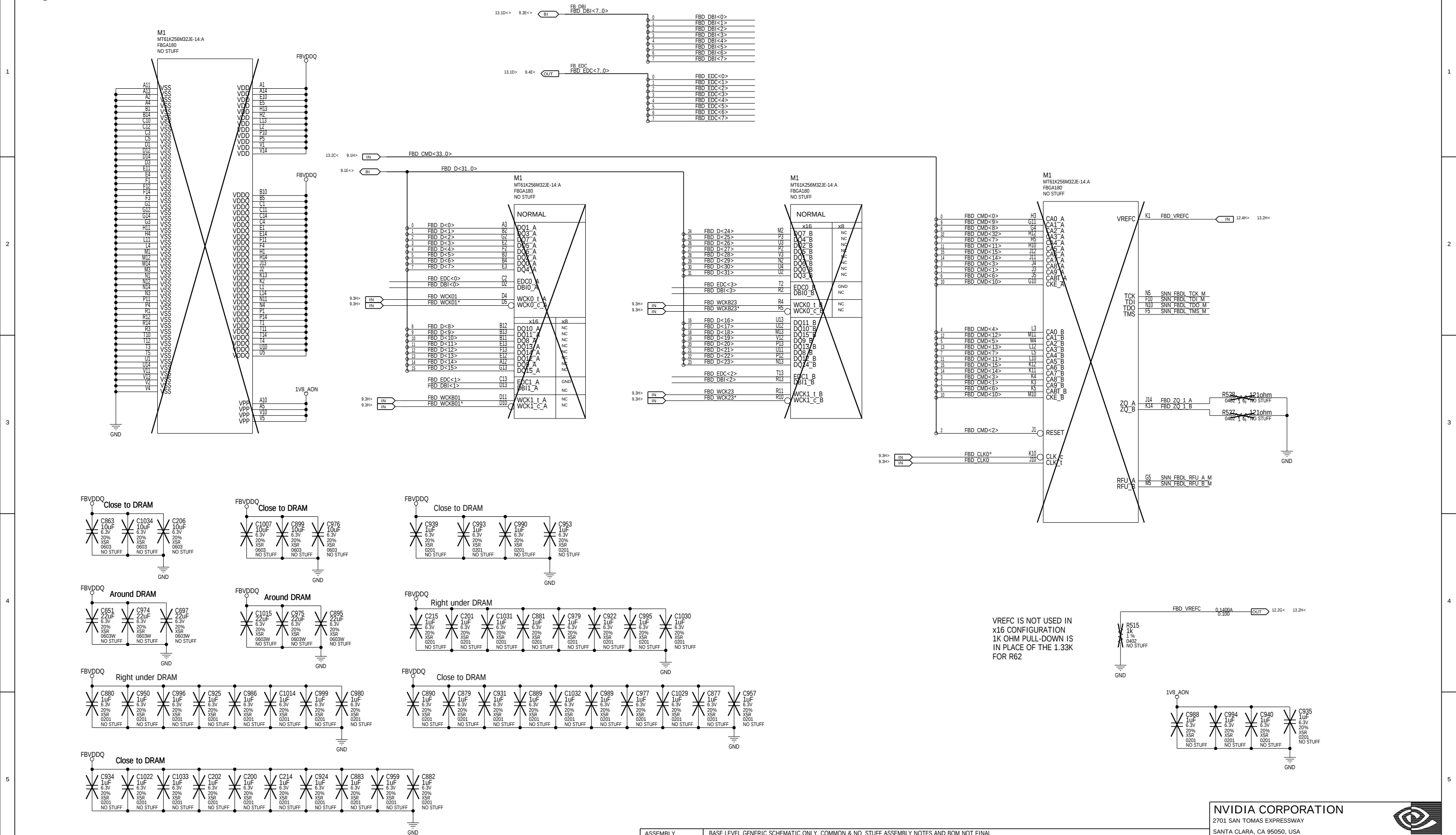
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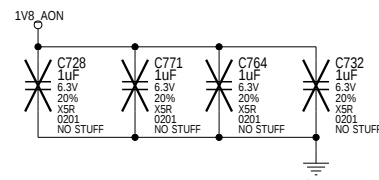
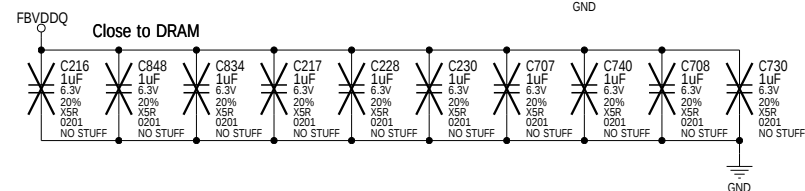
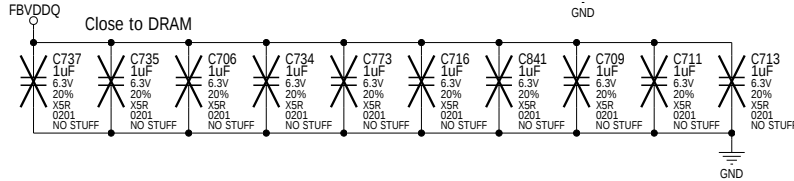
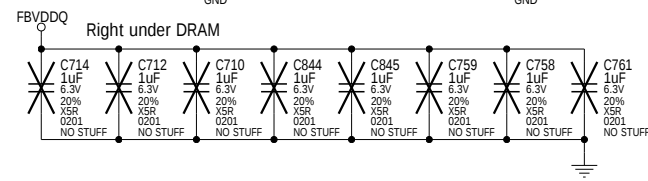
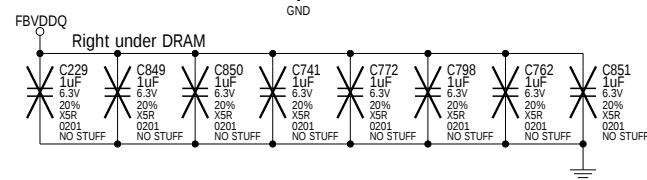
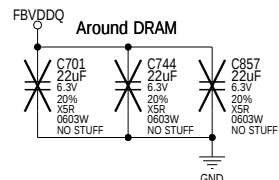
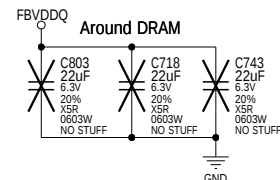
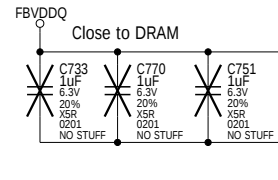
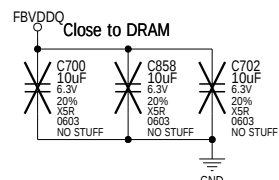
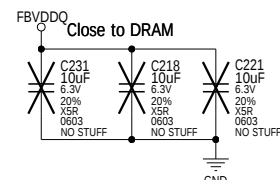
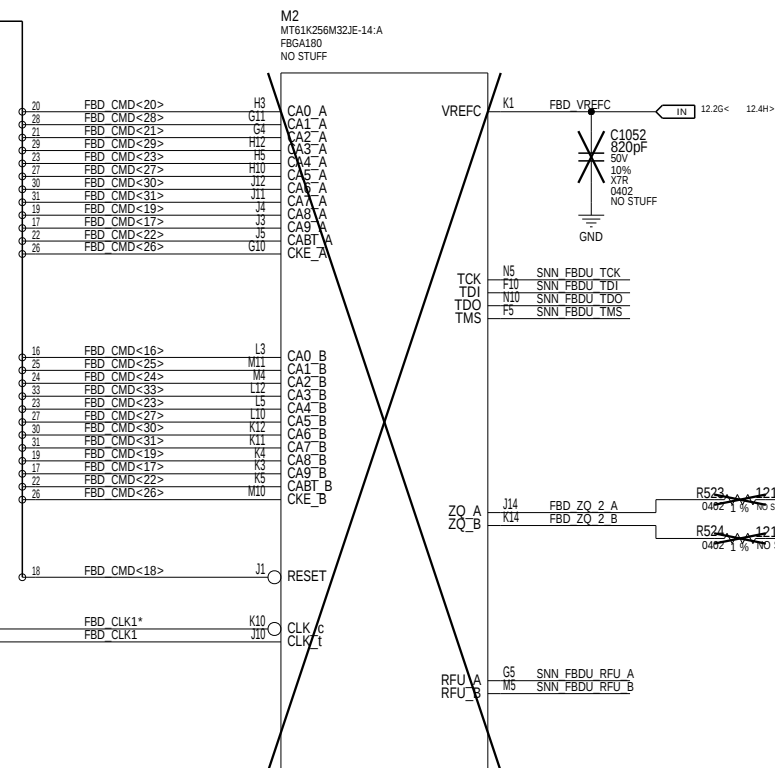
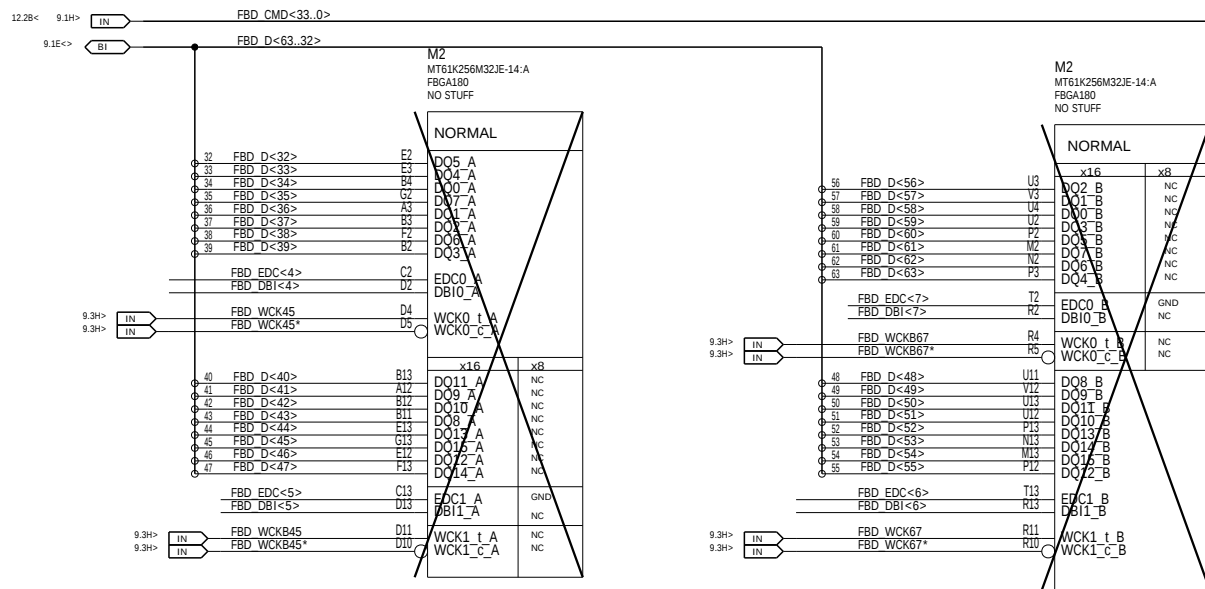
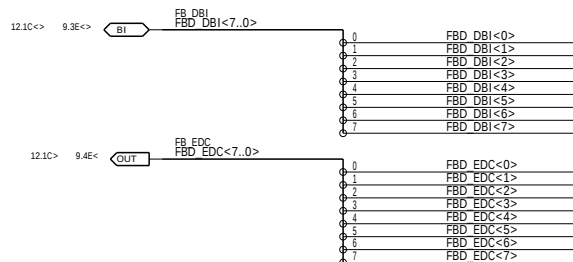
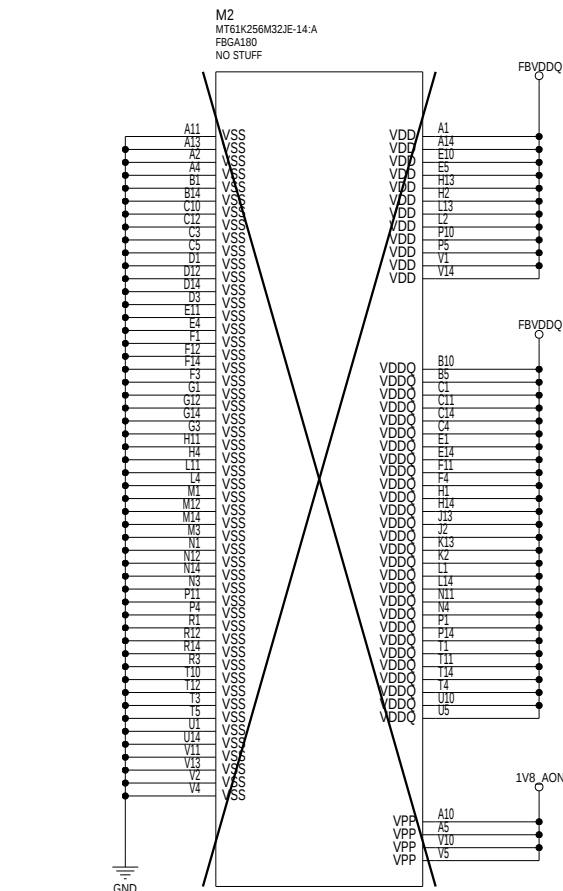
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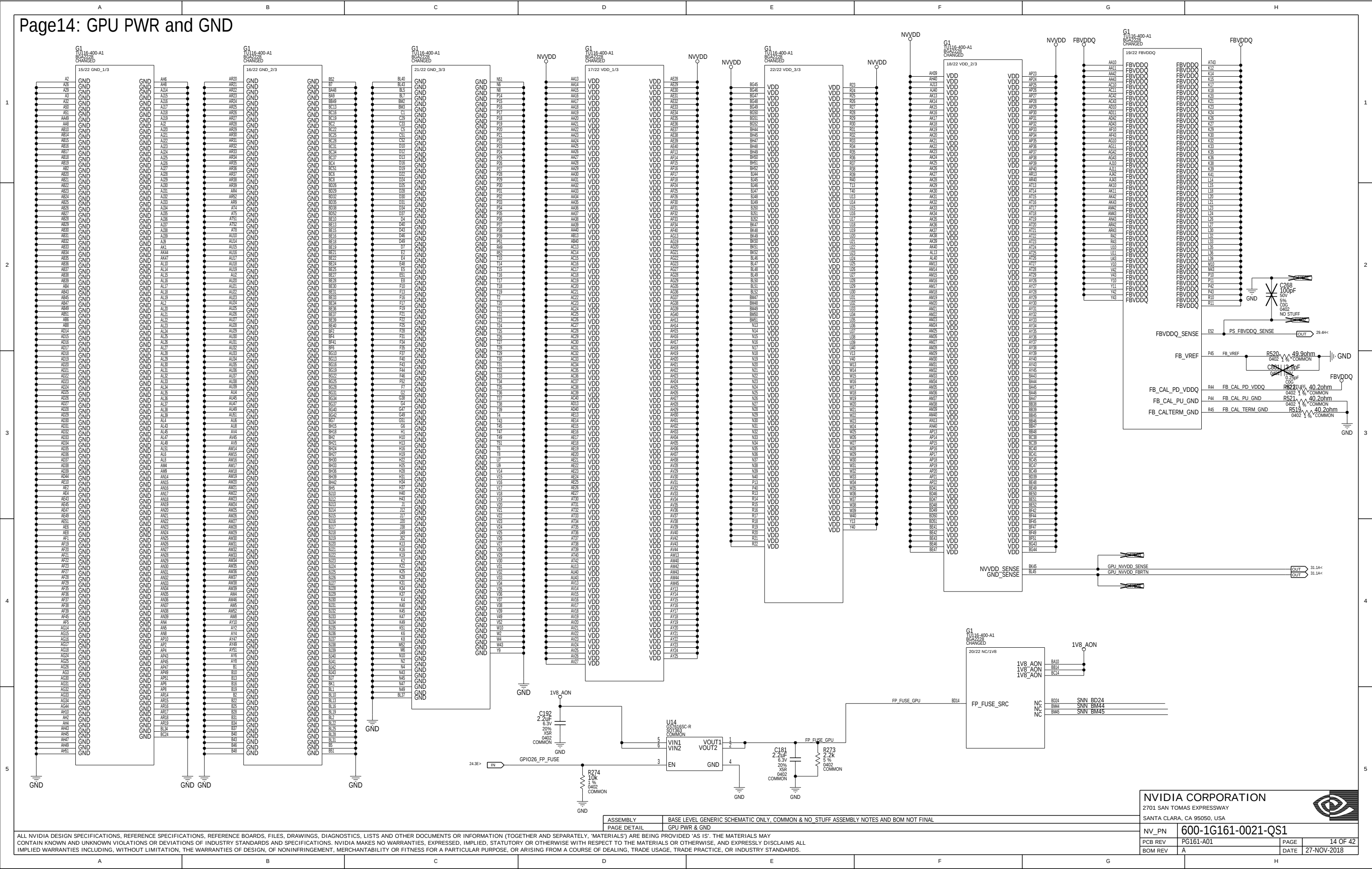
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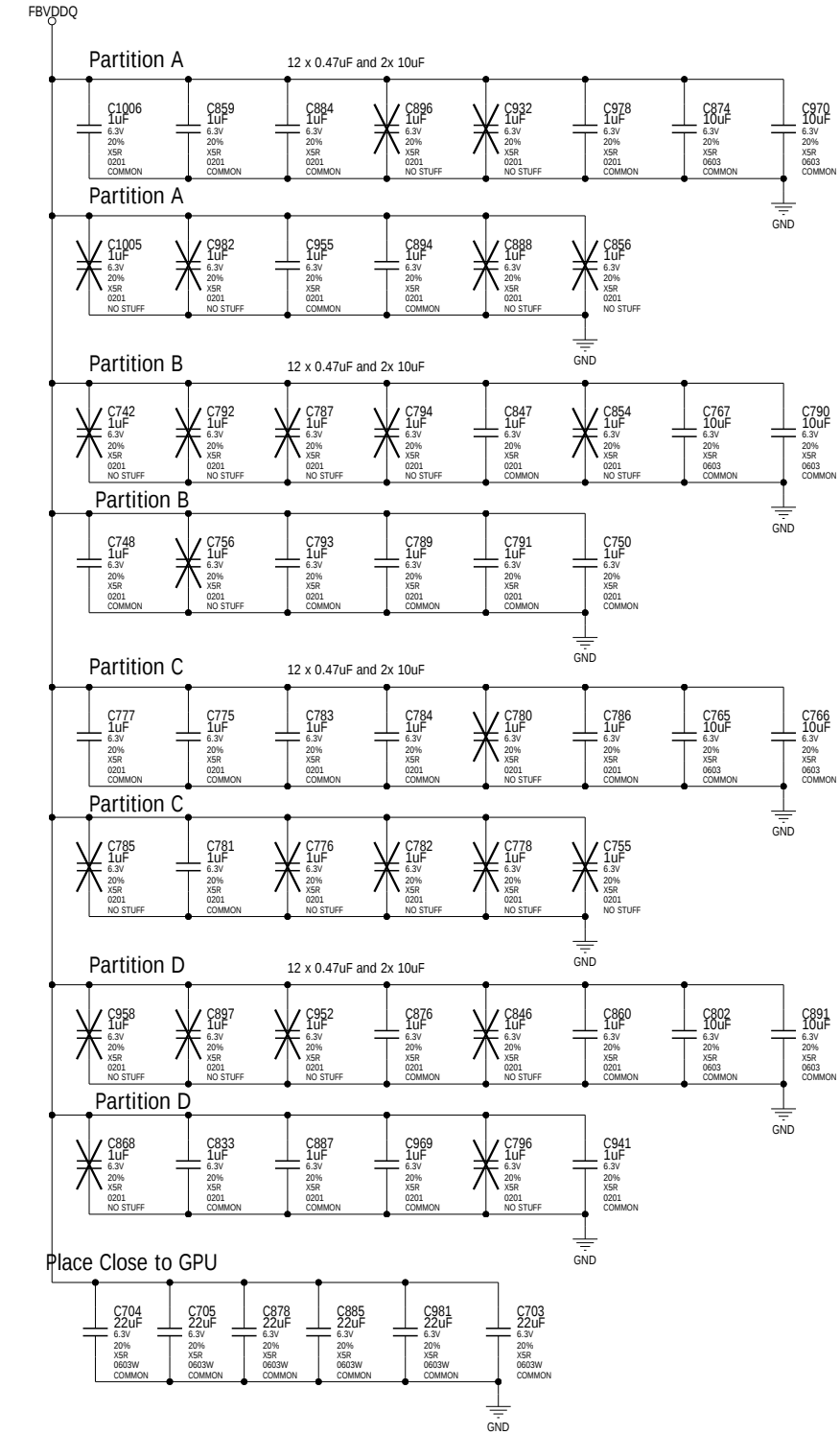
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Page14: GPU PWR and GND

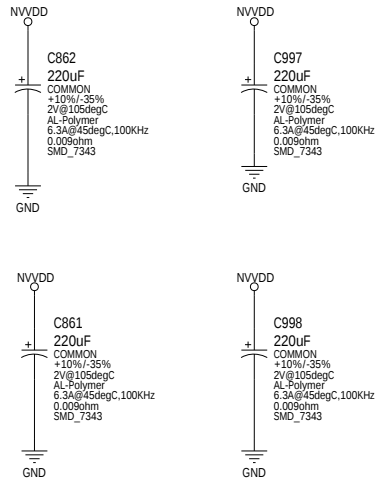


Page15: GPU Decoupling 1

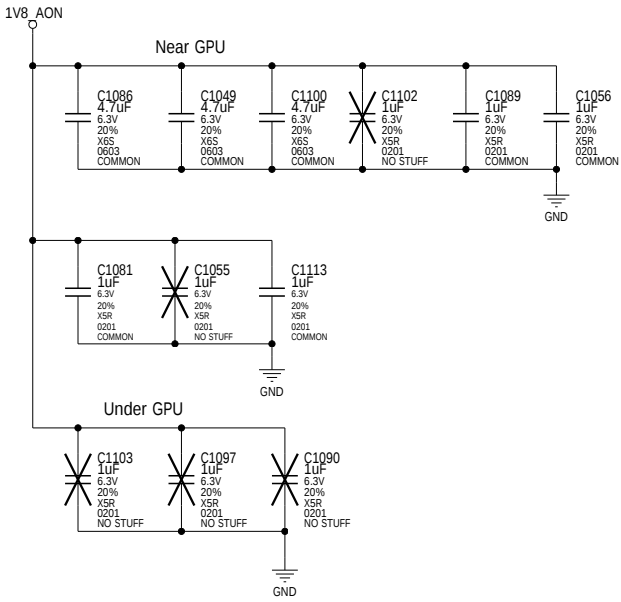
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NVVD



1V8_AON

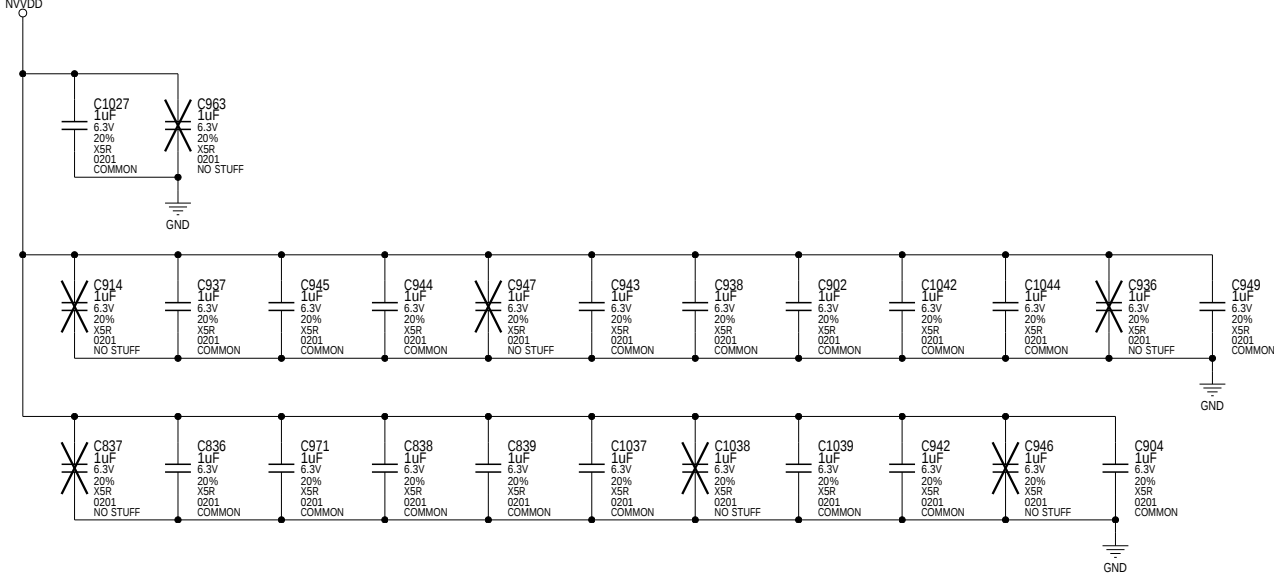
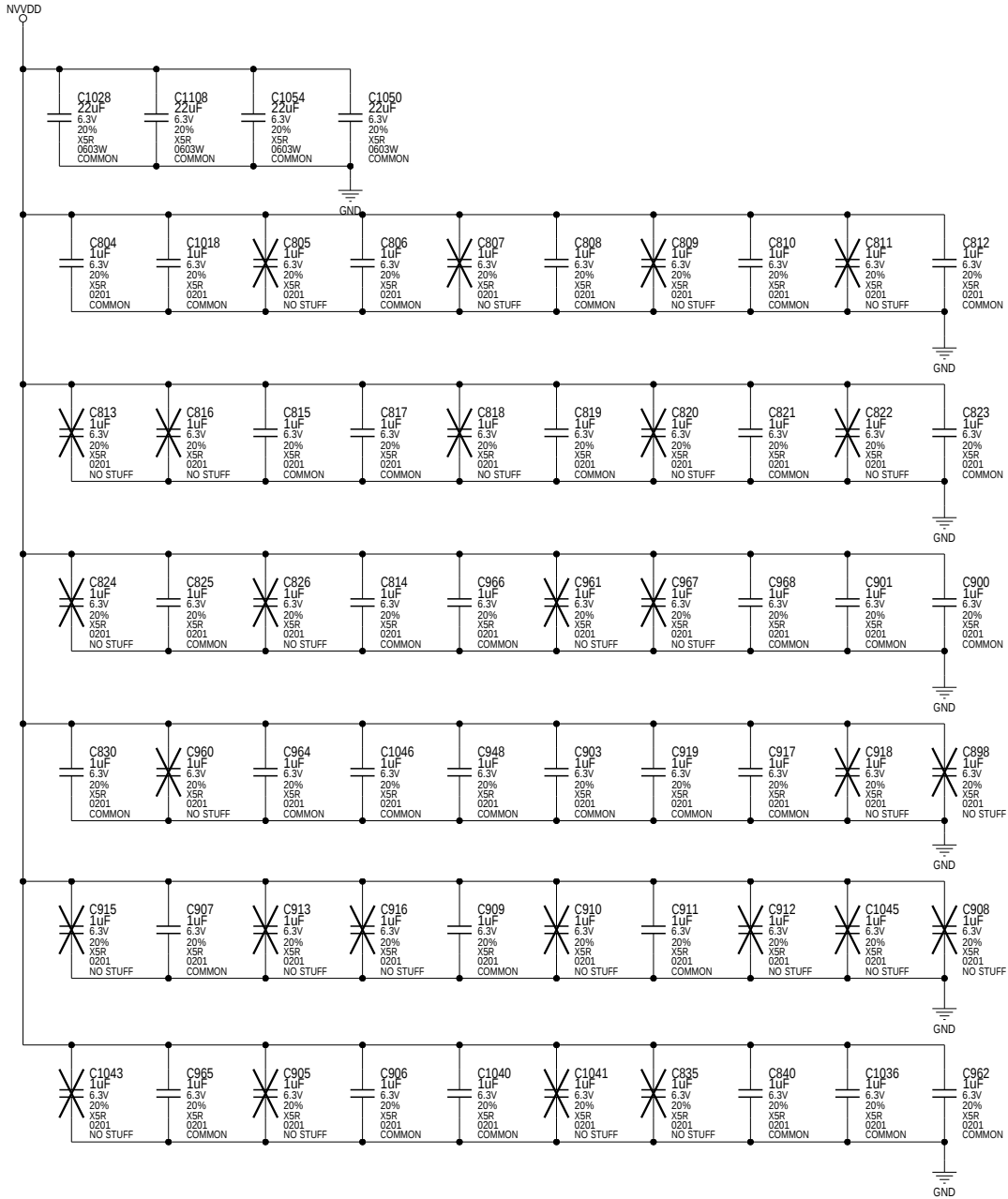


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Page16: GPU Decoupling 2

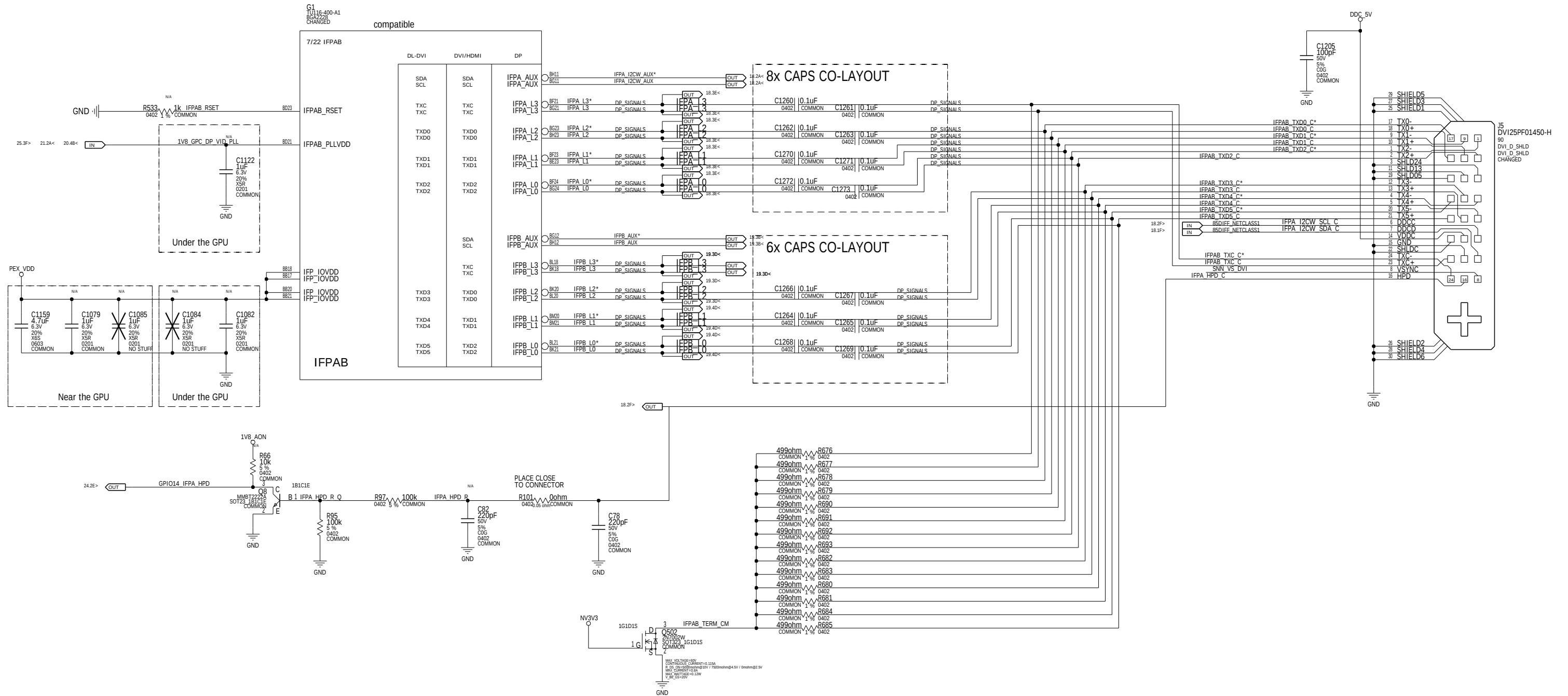
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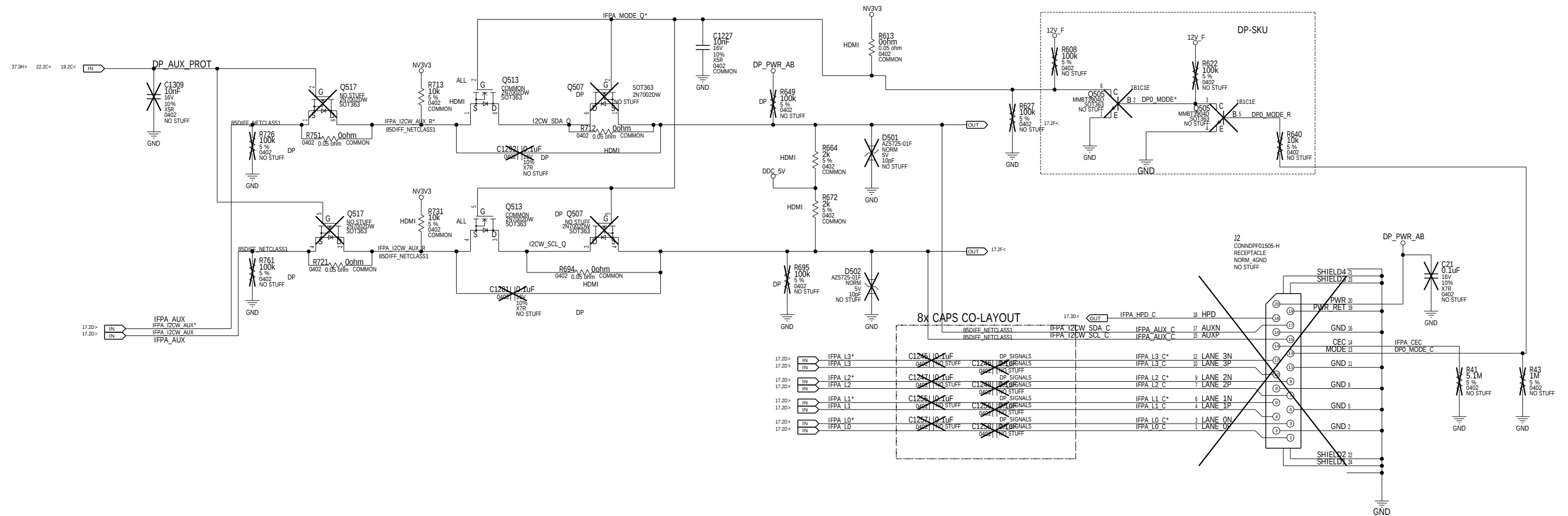


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IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP





IFPA DP CO-LAYOUT WITH IFPAB DVI-D-DL

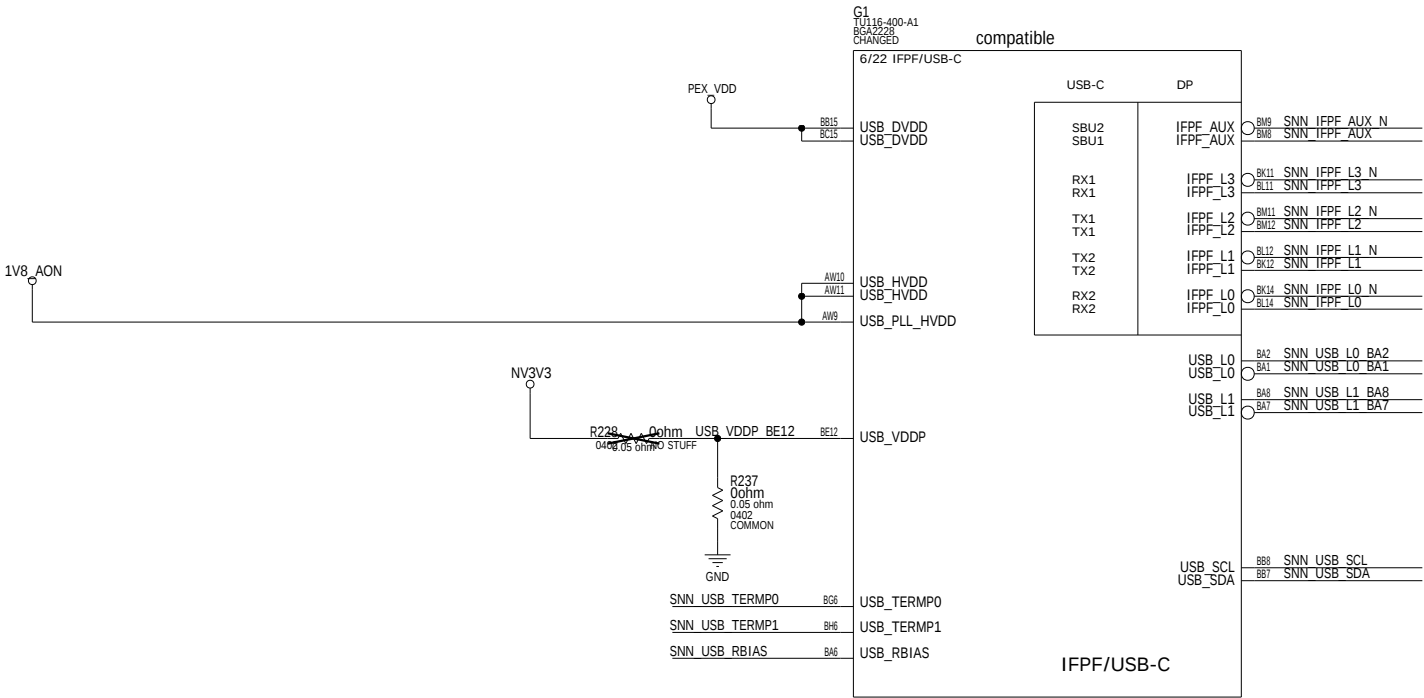
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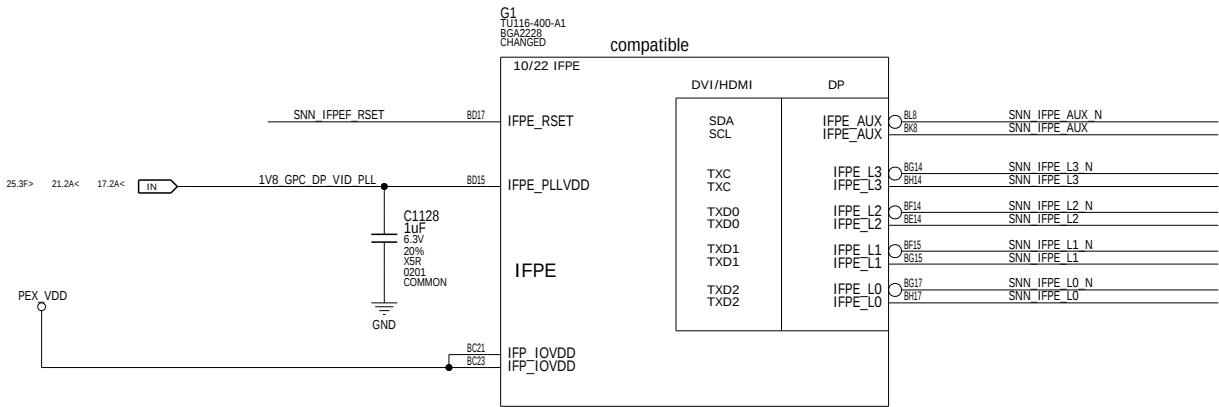
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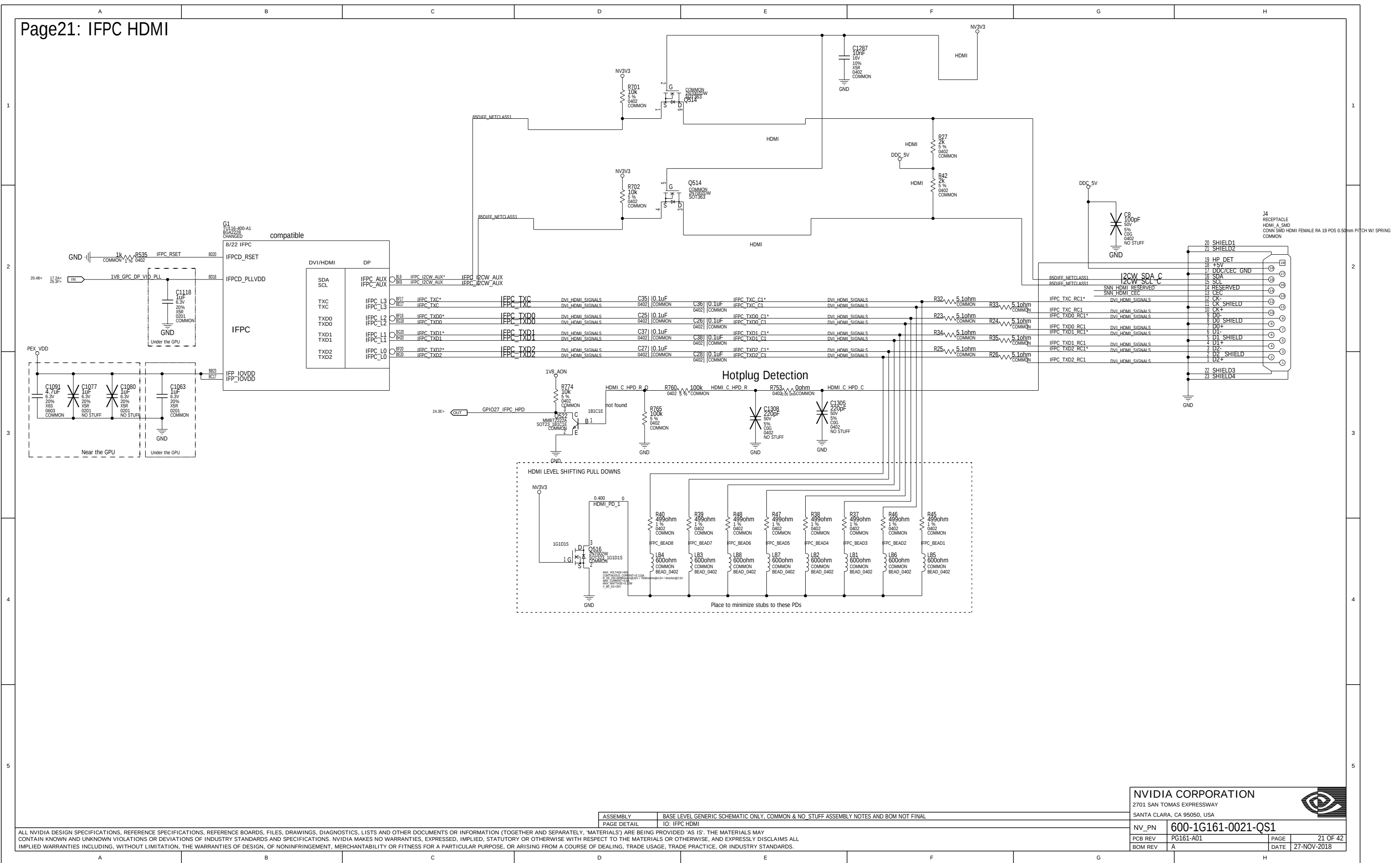
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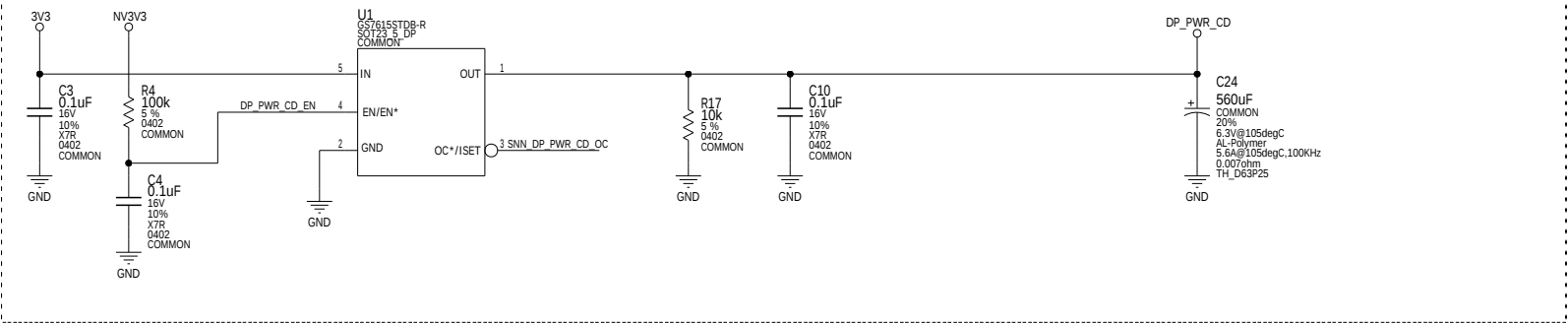
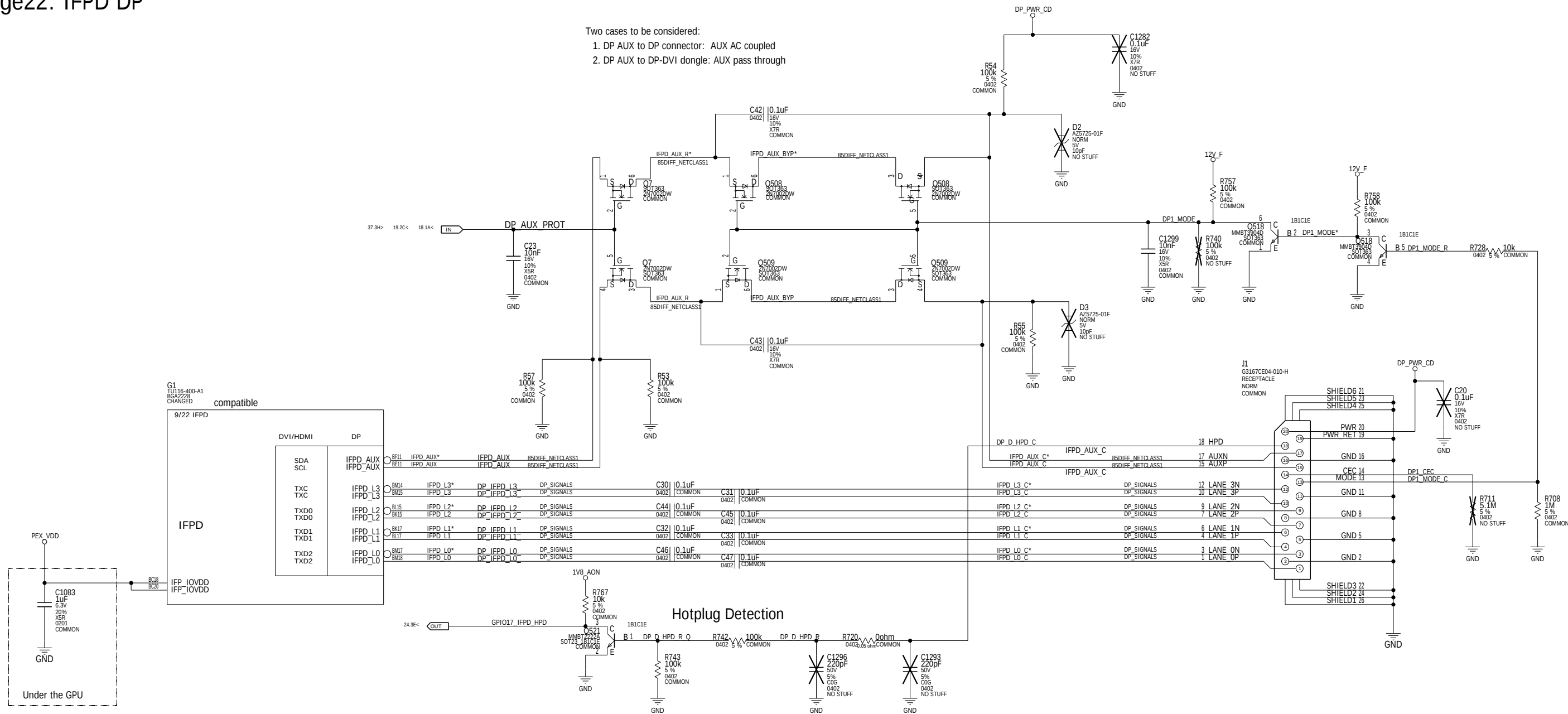
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Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

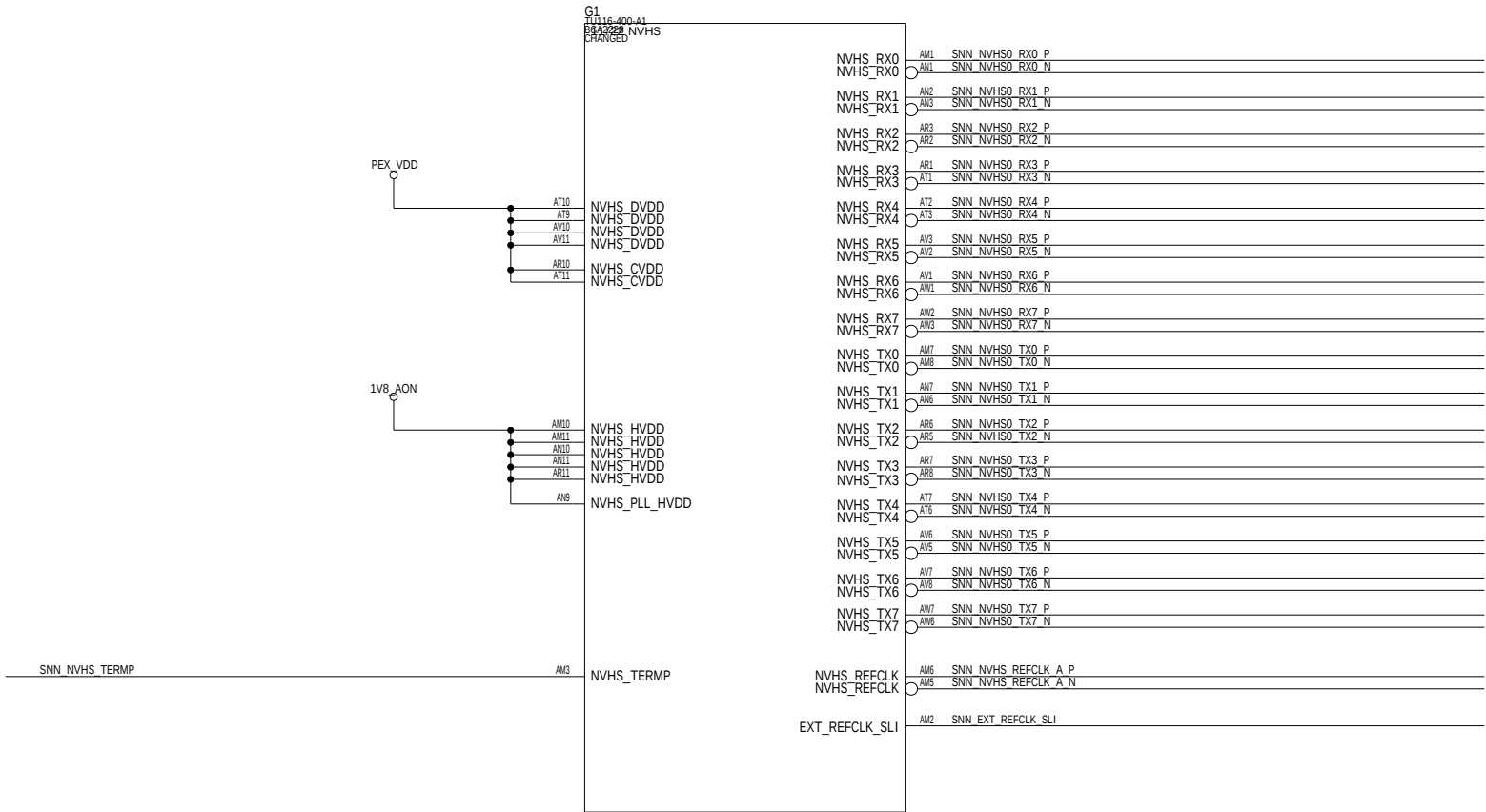


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PAGE DETAIL	IO: IFPD DP

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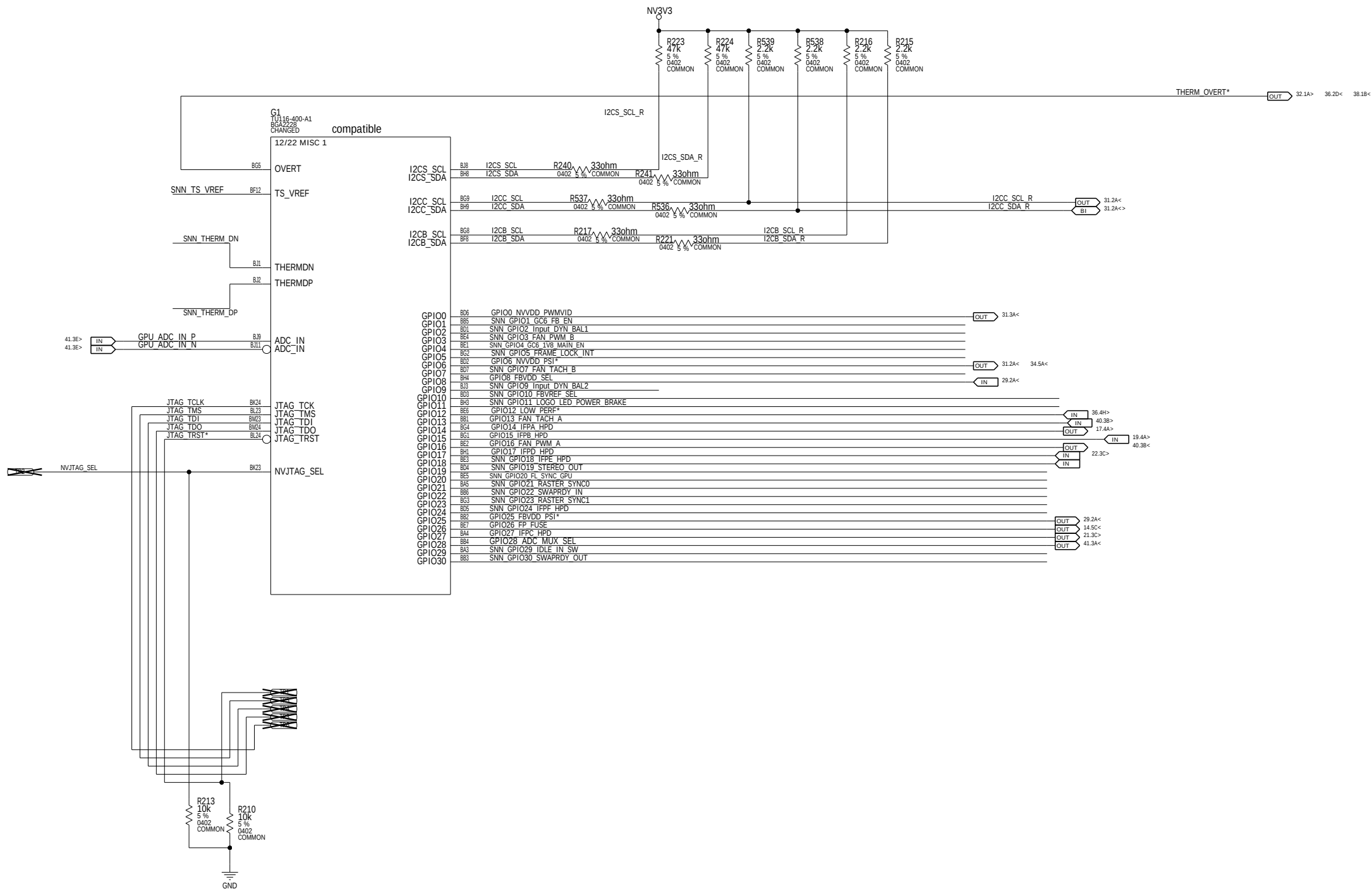
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Page23: NVHS Interface and Frame Lock



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Page24: MISC1: Fan, Thermal, JTAG, GPIO



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1

2

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1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
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1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



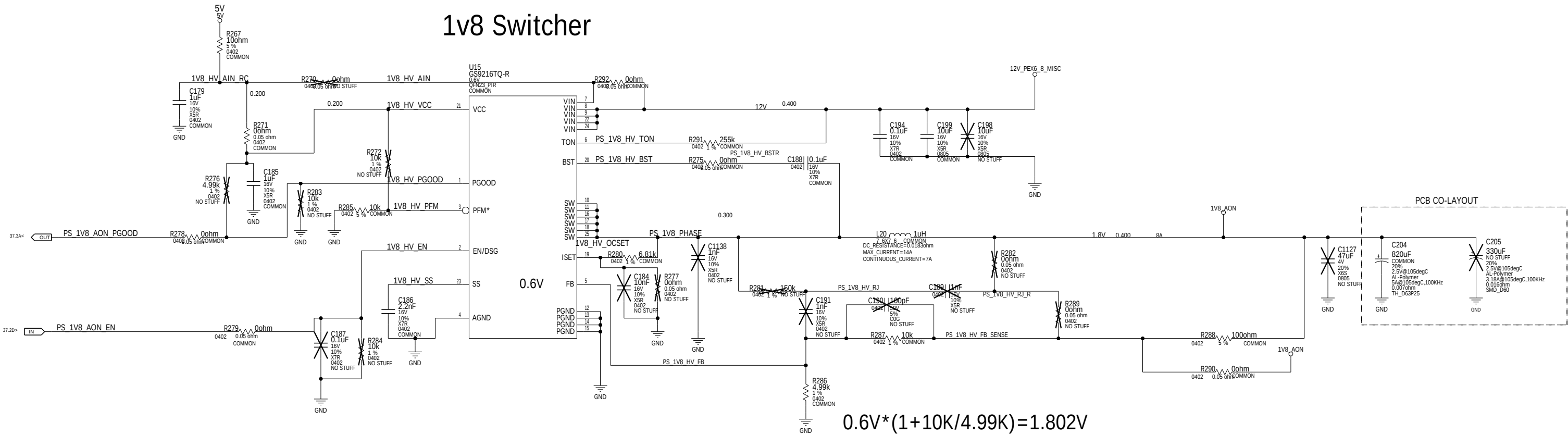
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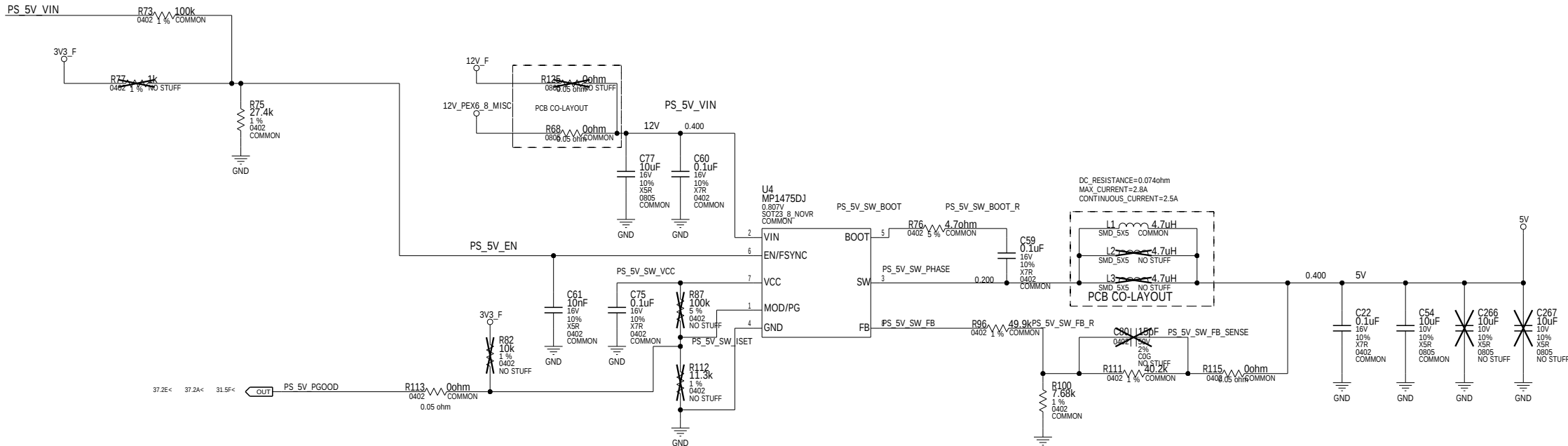
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1v8 Switcher



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$$0.8V^*(1+40.2K/7.68K)=4.9875V$$

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PAGE DETAIL	PS: 5V

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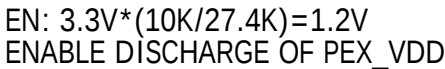
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PEX Switcher



$$0.6V \cdot (1 + 10K/14.7K) = 1.008V$$

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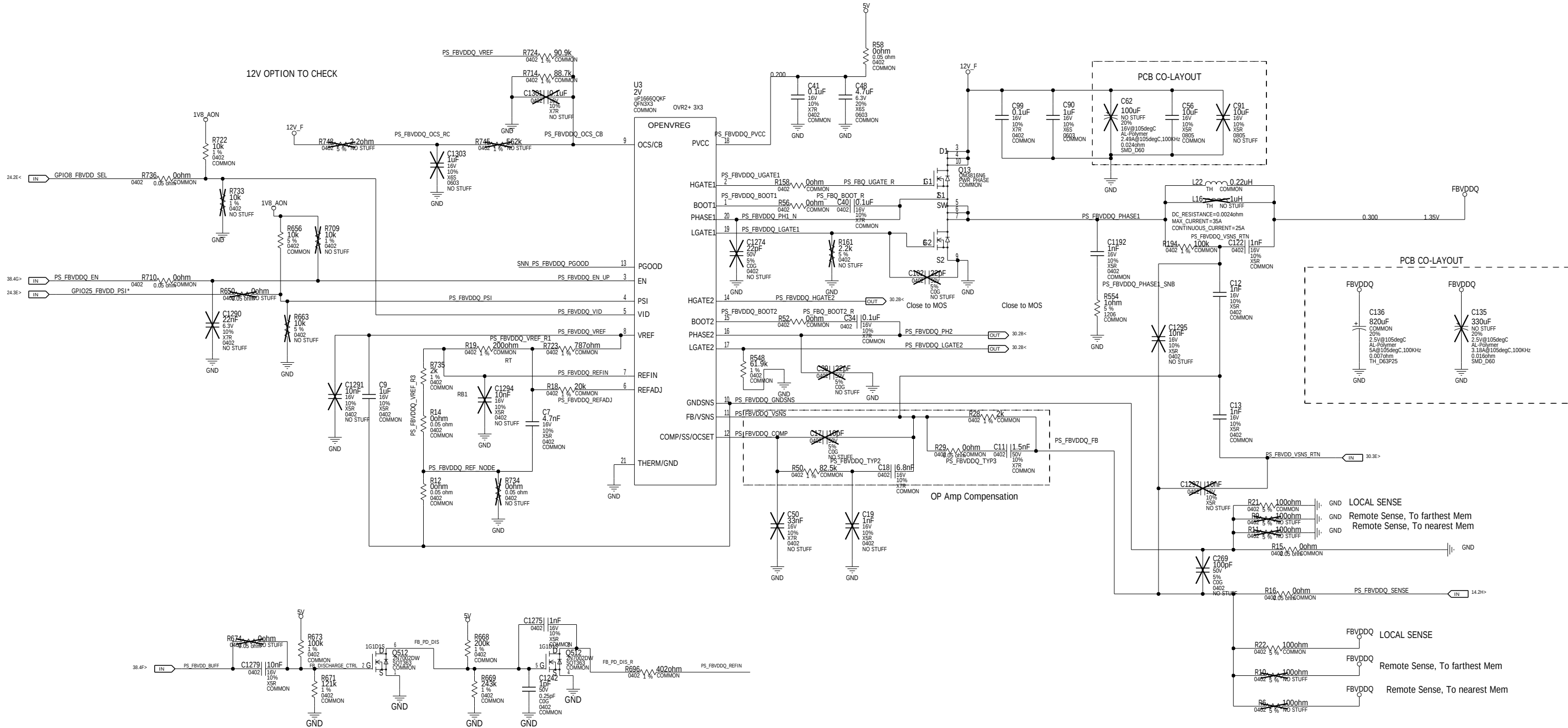
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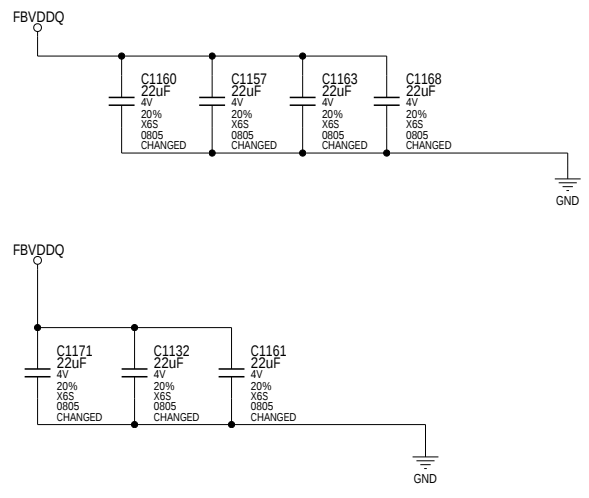
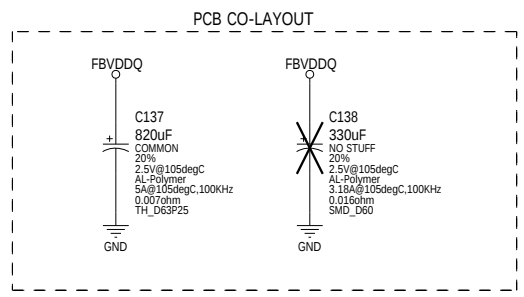
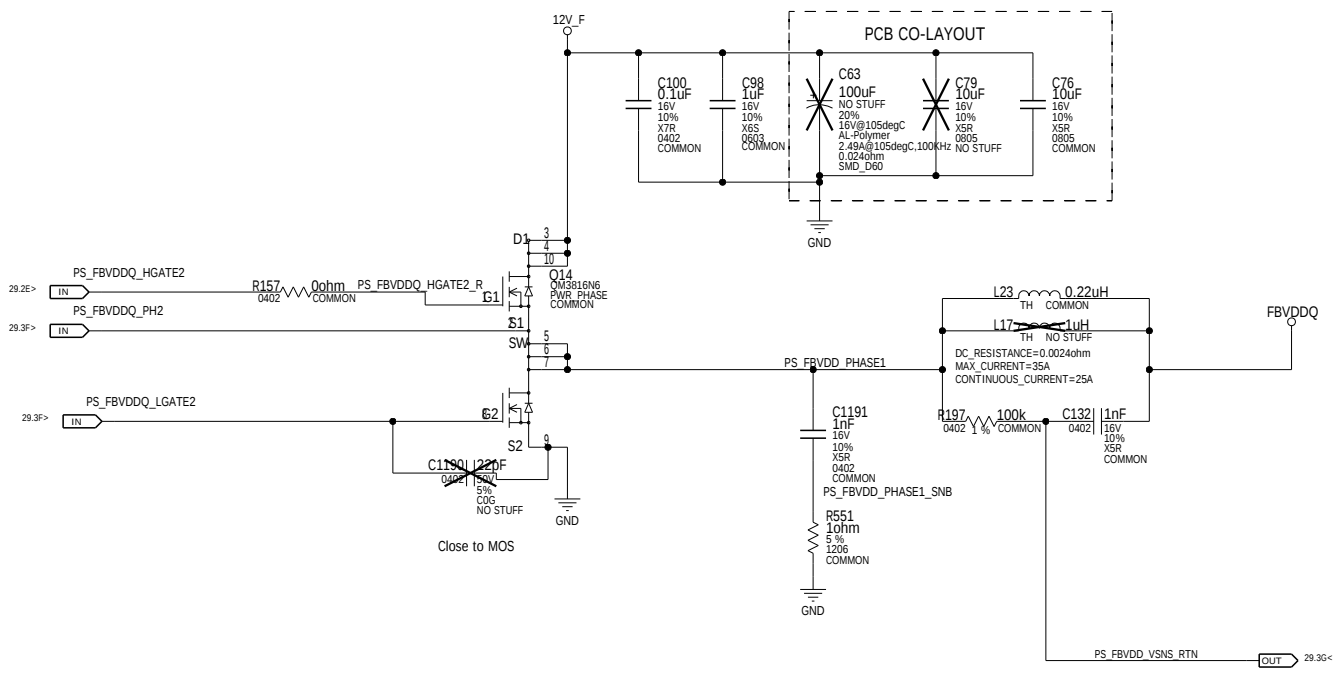
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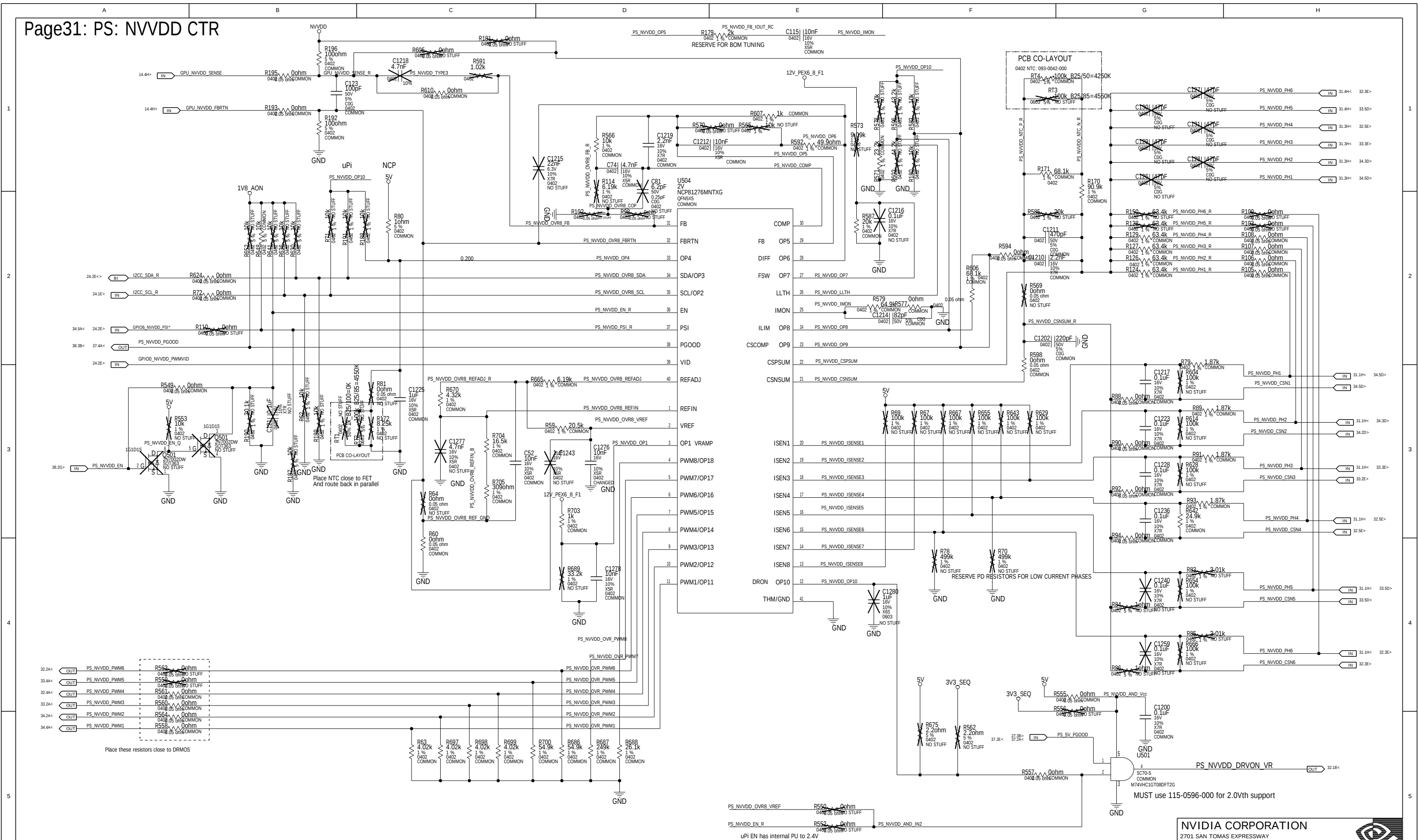
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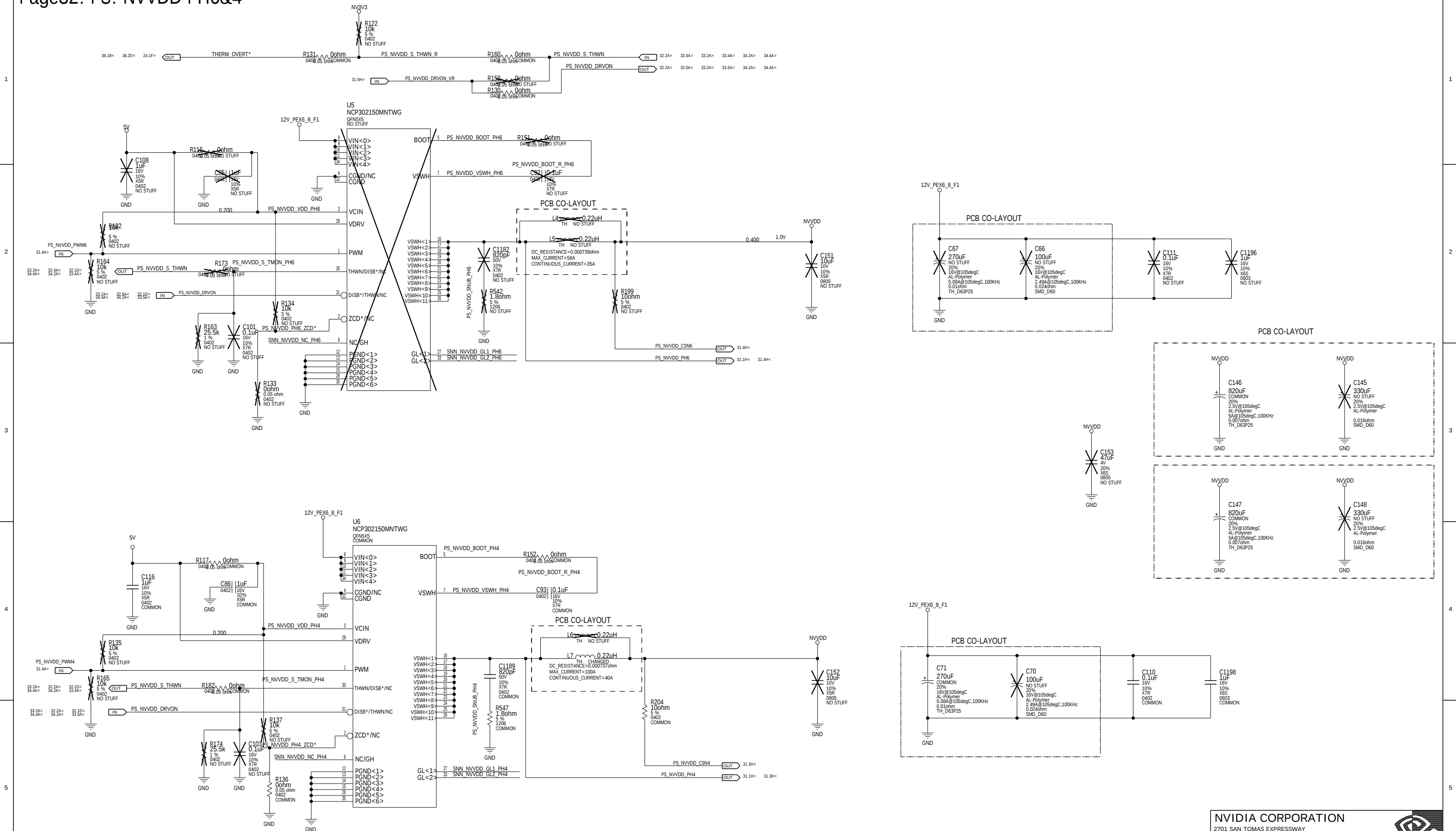
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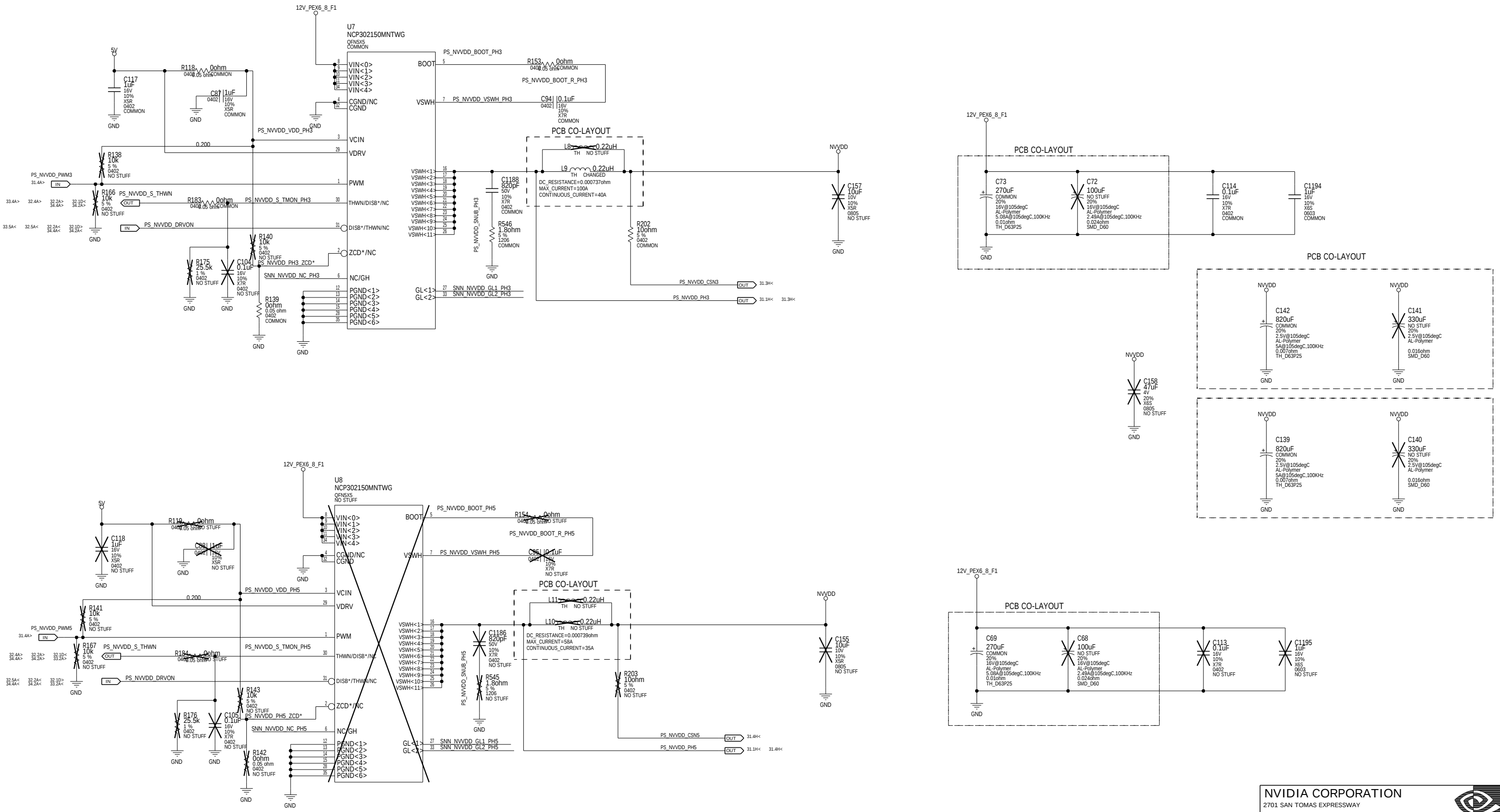
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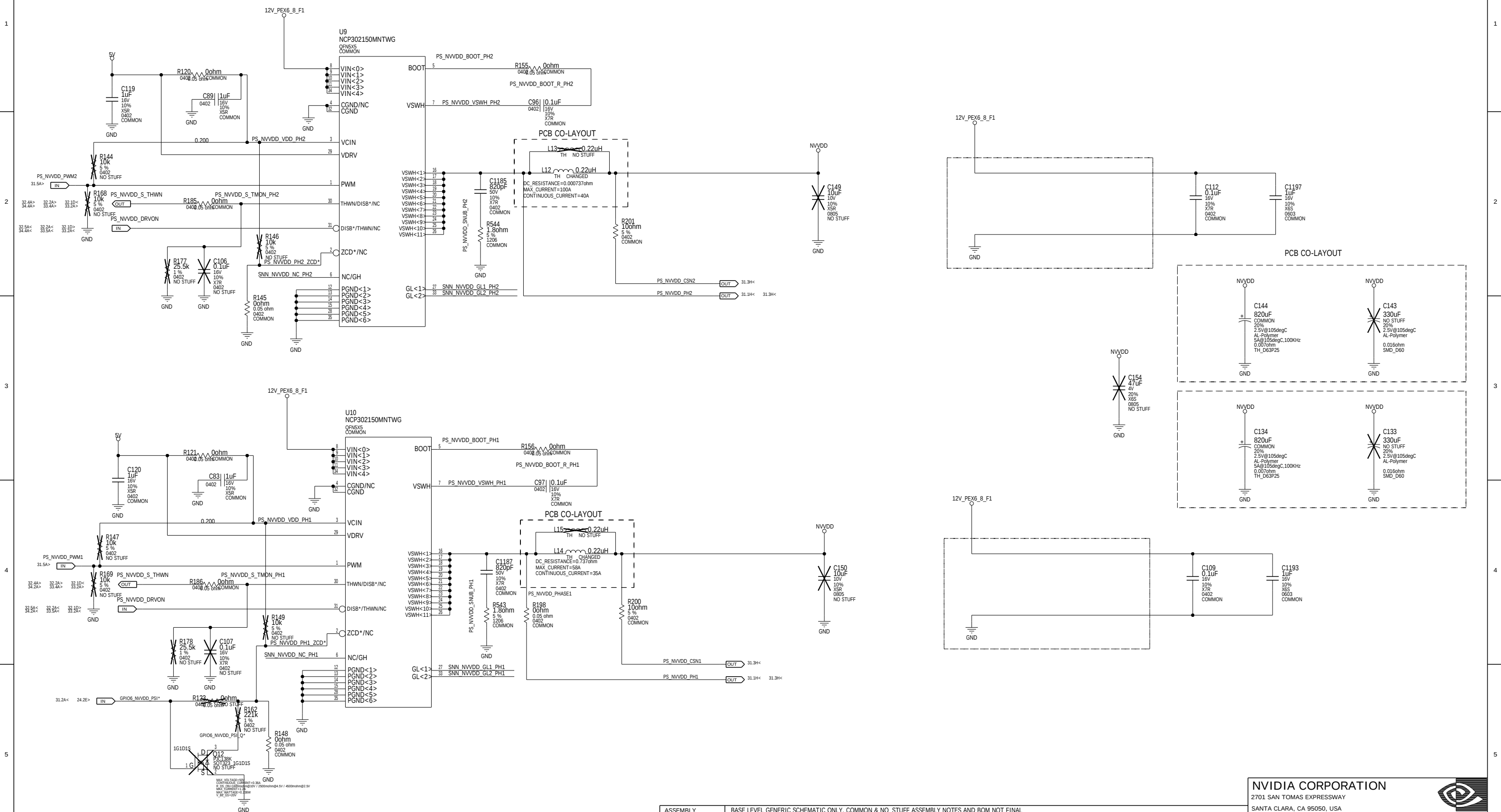
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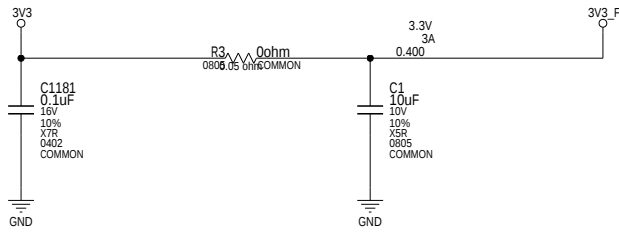


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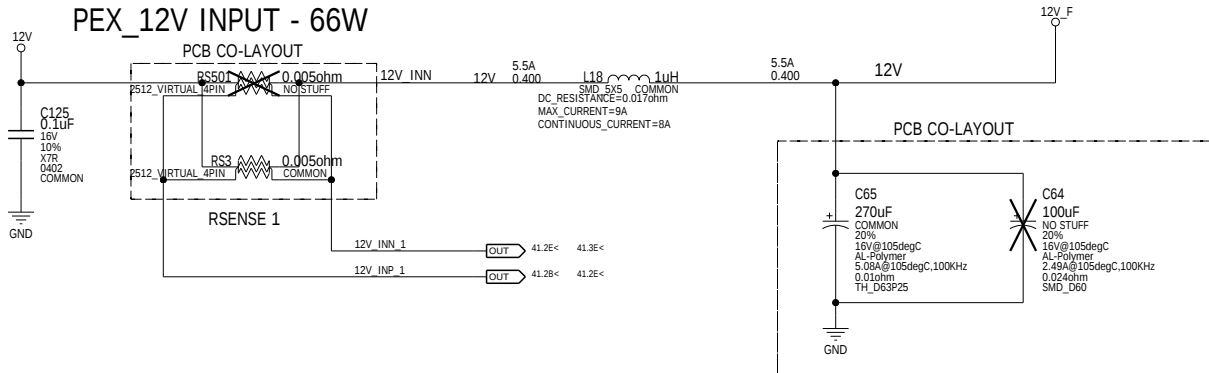
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PAGE DETAIL	PS: NVVDD Phase 2,1

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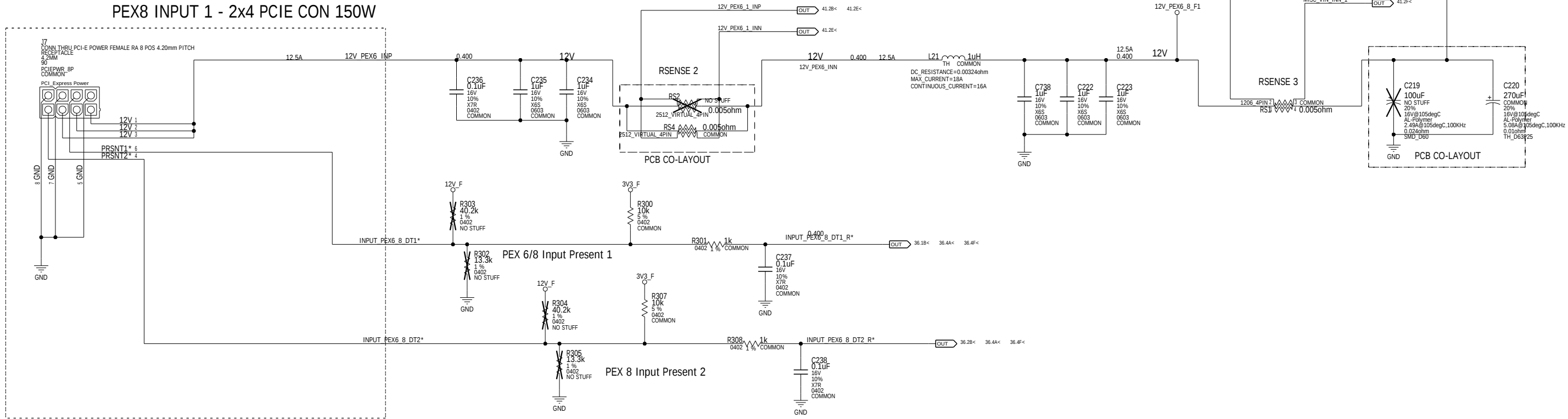
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PEX_12V INPUT - 66W



PEX8 INPUT 1 - 2x4 PCIE CON 150W



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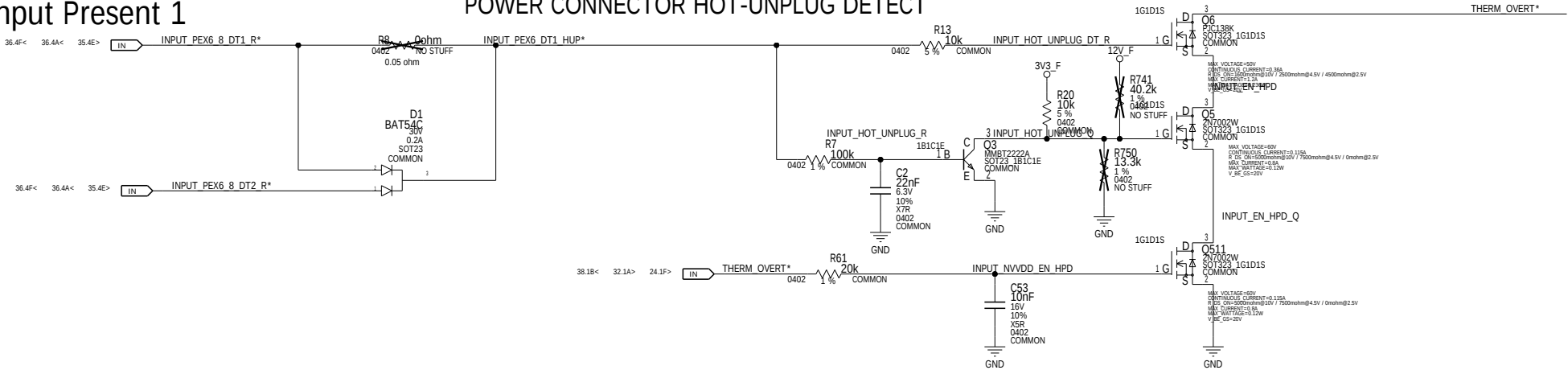
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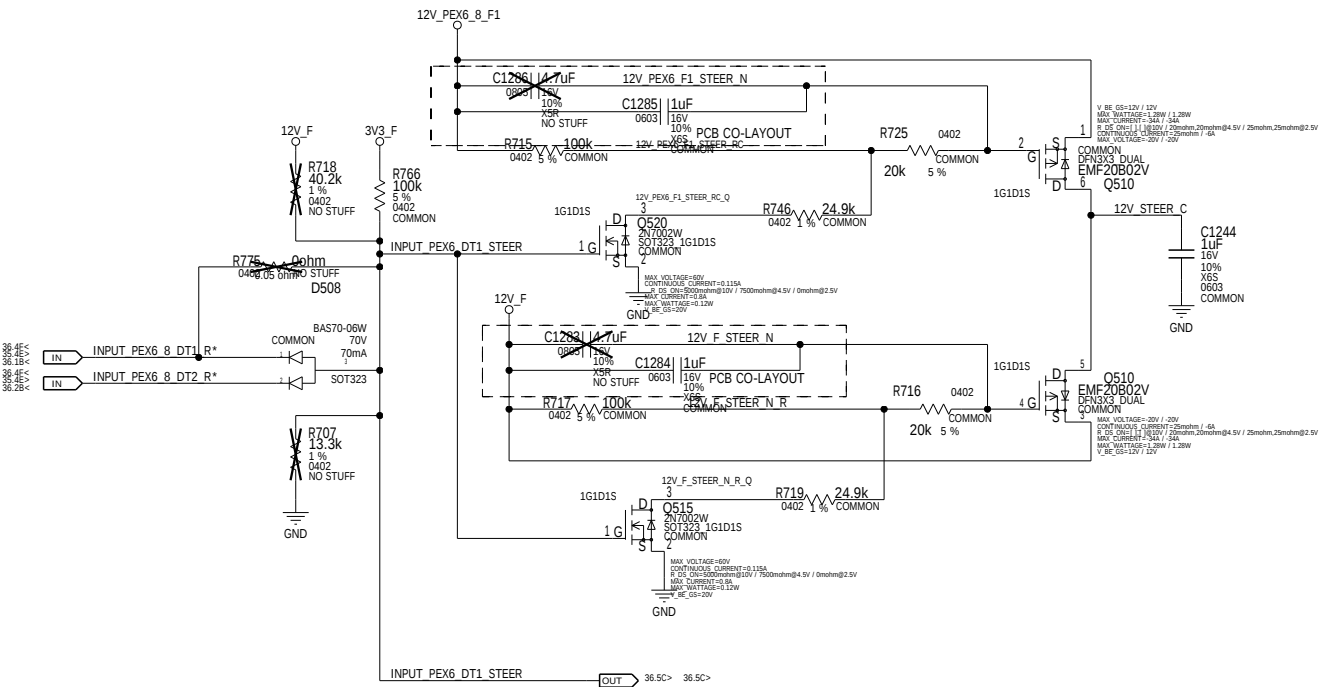
PEX Input Present 1

POWER CONNECTOR HOT-UNPLUG DETECT

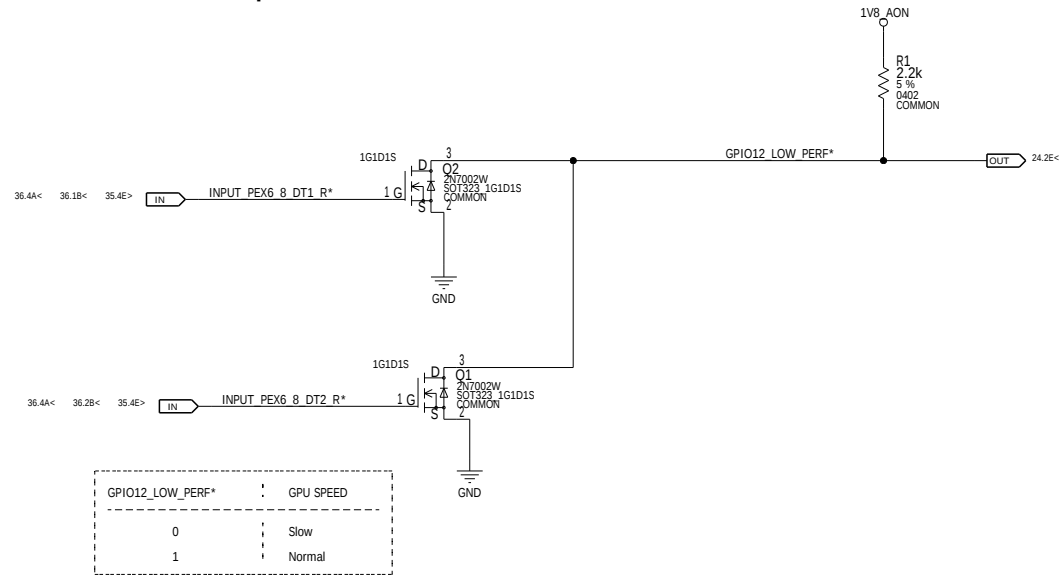


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA

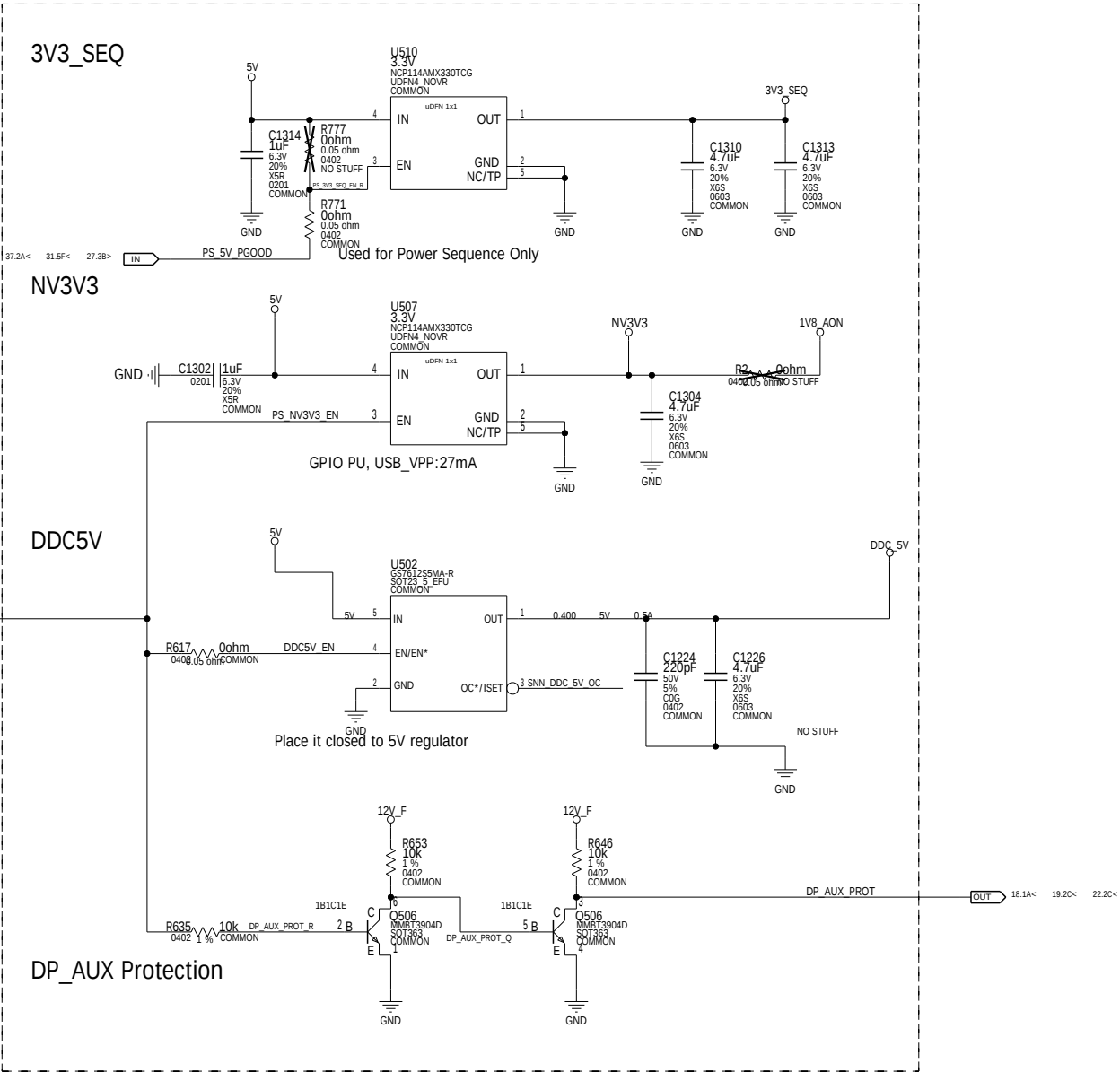
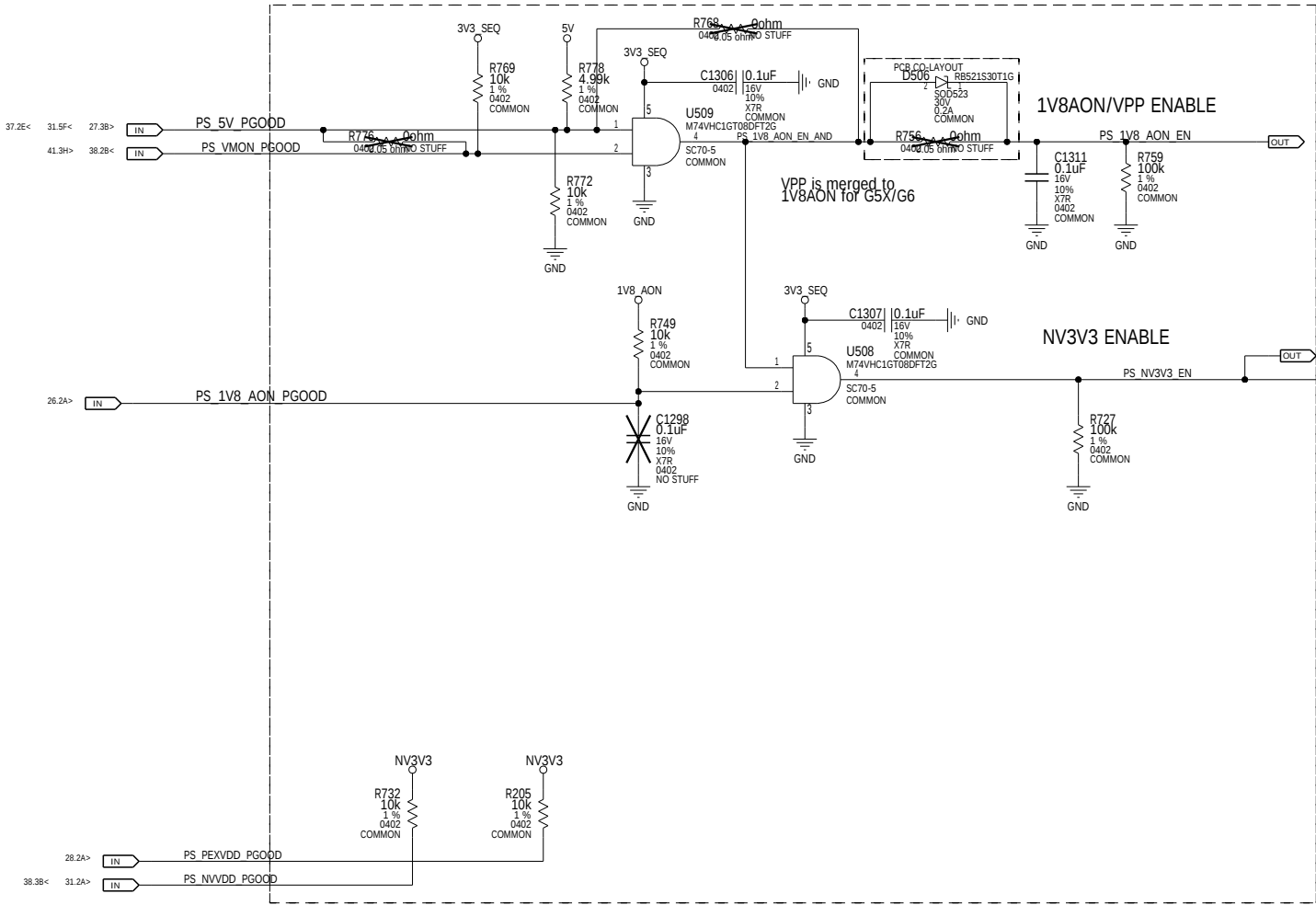


PEX Input - Power Level/PSI* Control

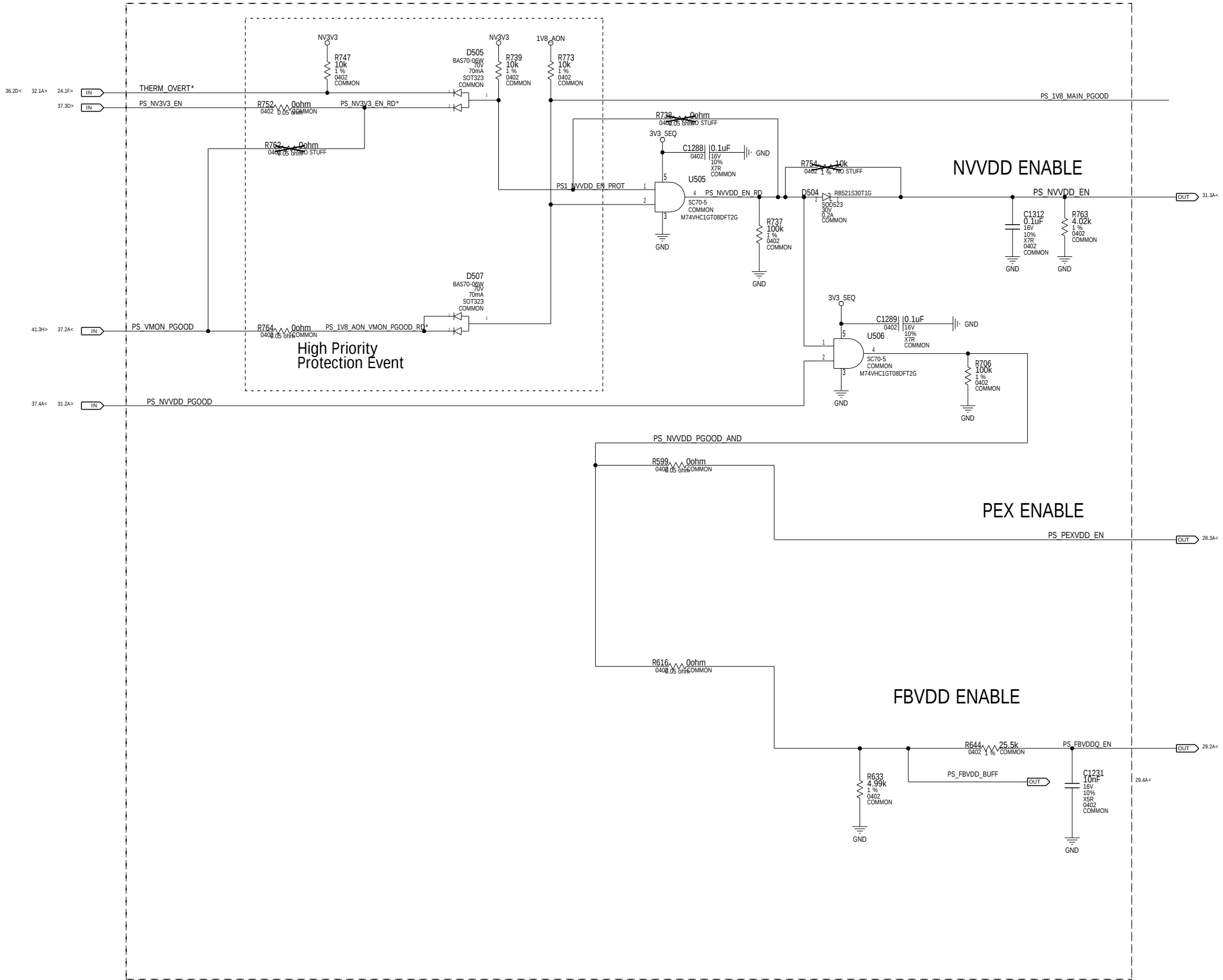


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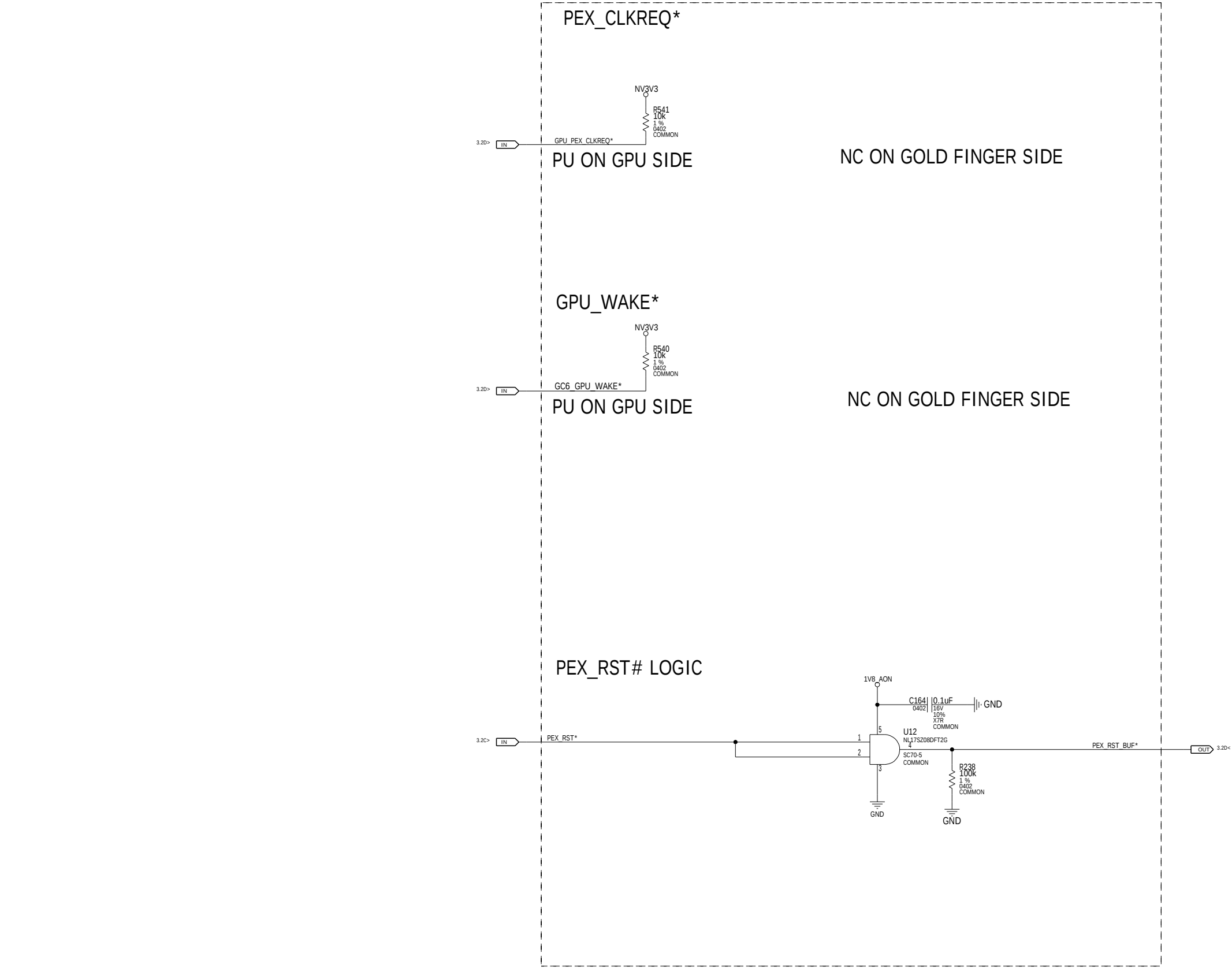


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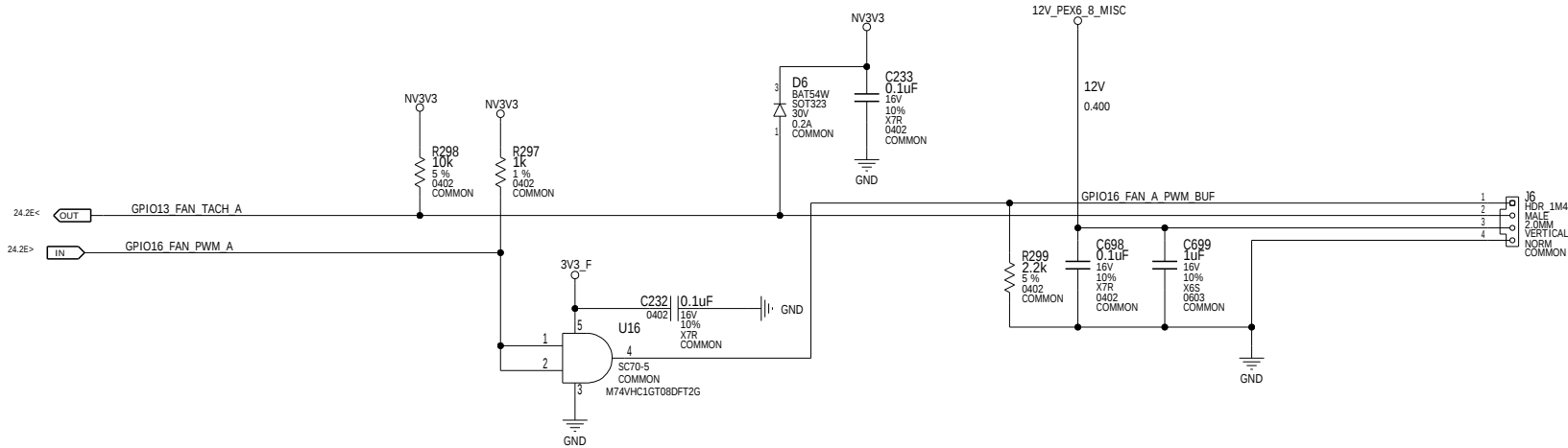


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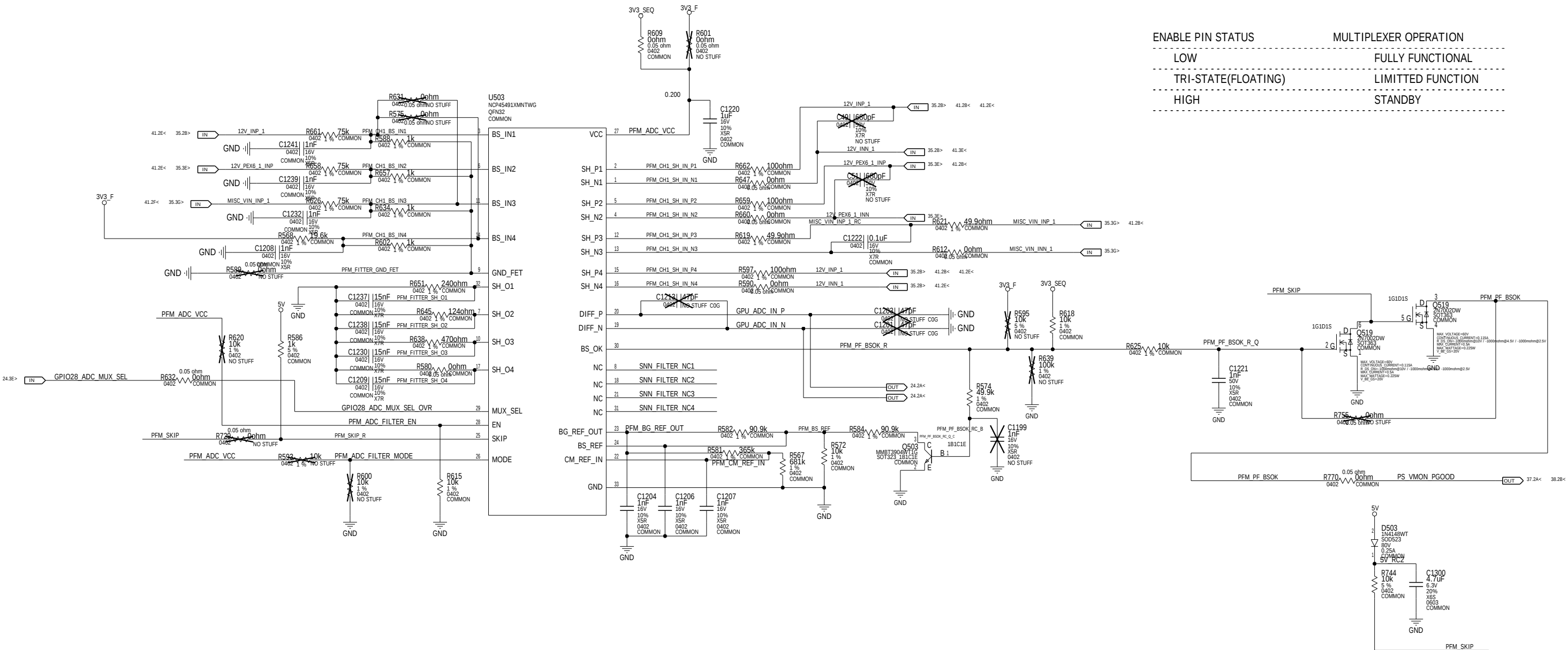


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MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

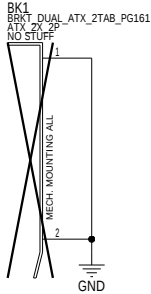
ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY



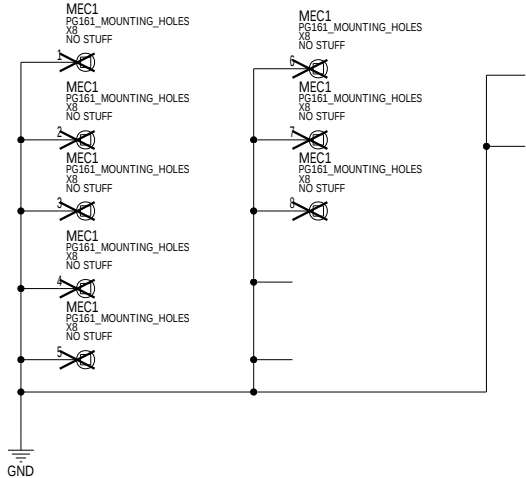
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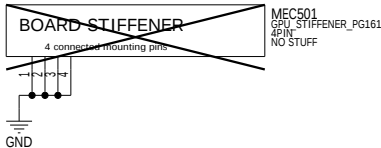
Bracket:



MOUNTING HOLES FOR HS:



BACK STIFFENER:



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