

PG161-A00

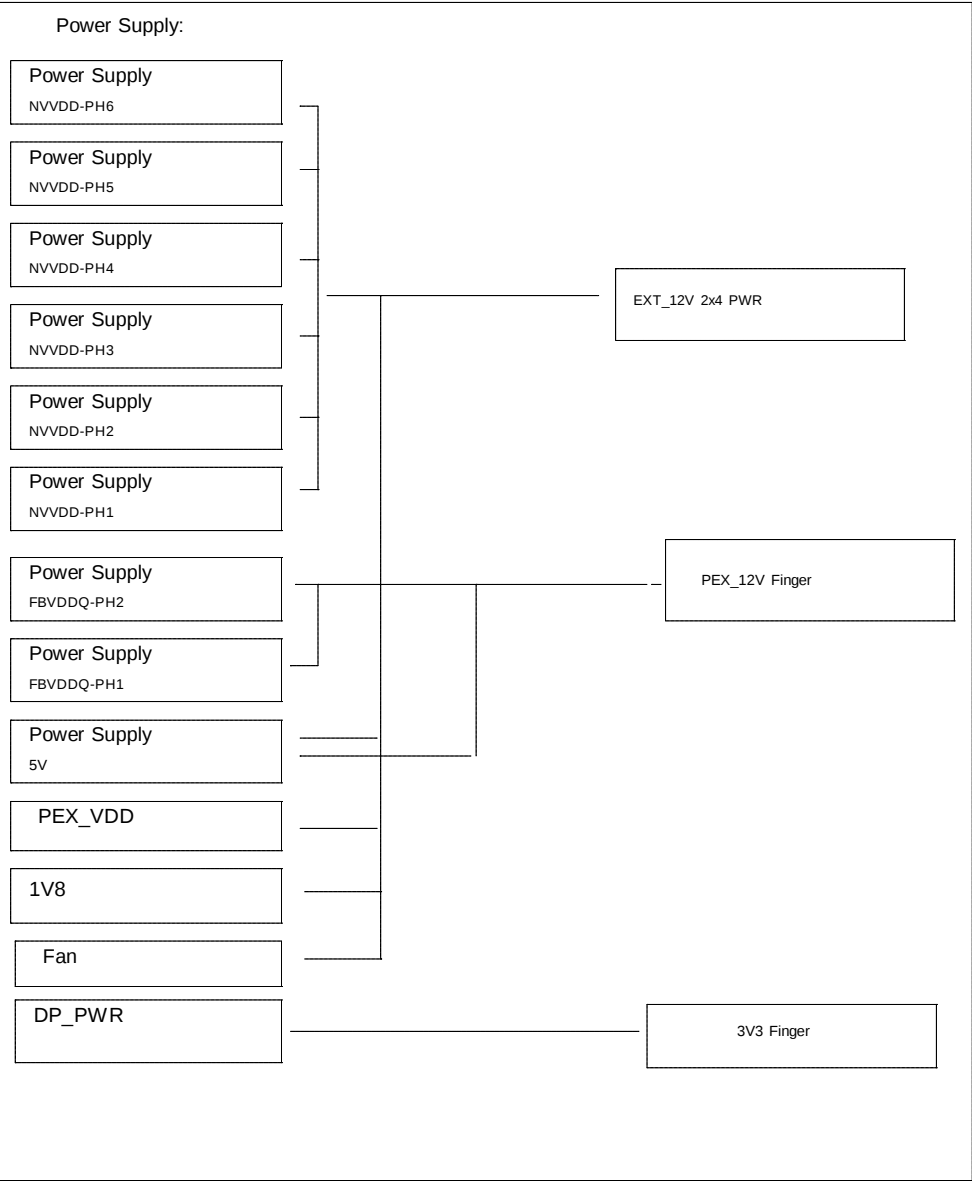
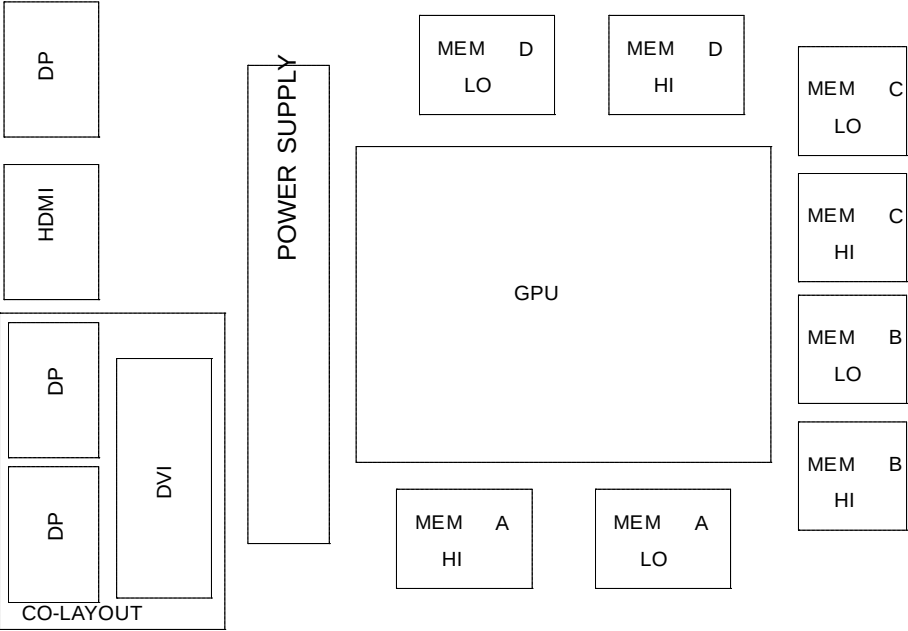
TU106 6GB GDDR6, 192b, X16
DVI-D/DP + DP + HDMI

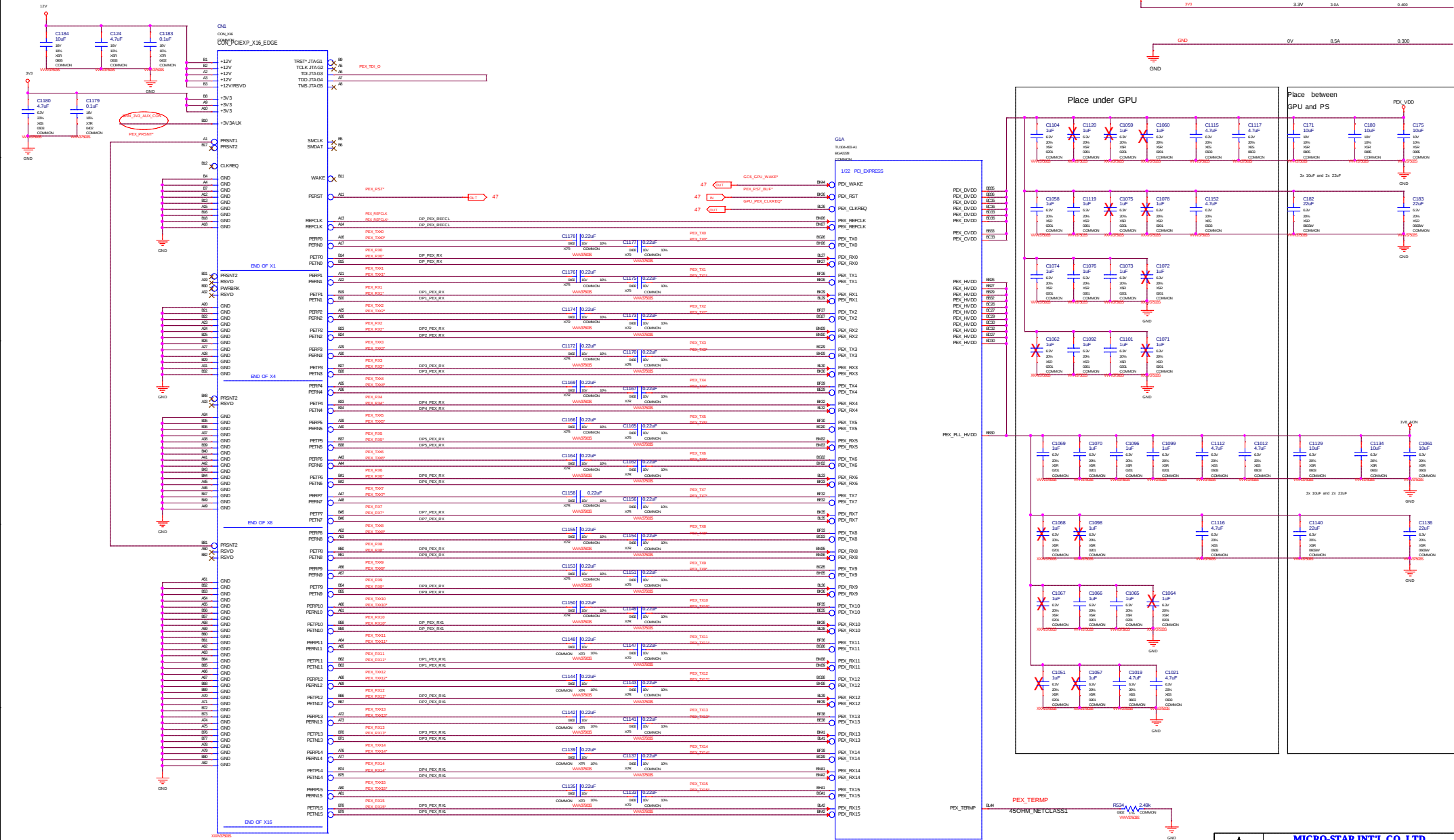
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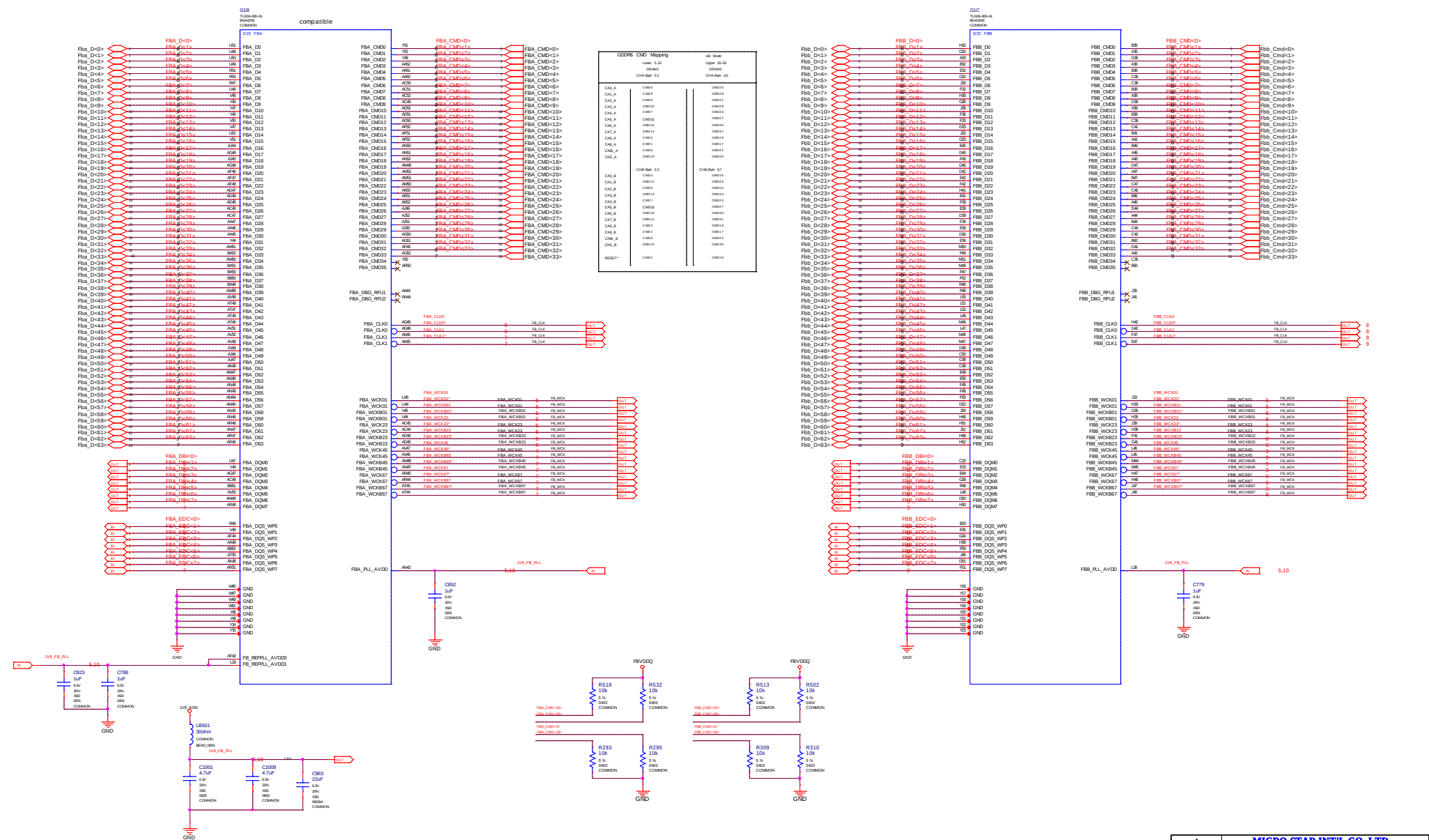
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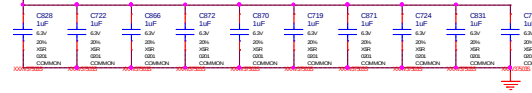
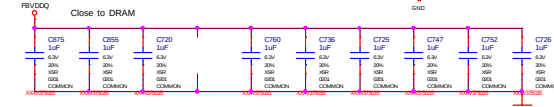
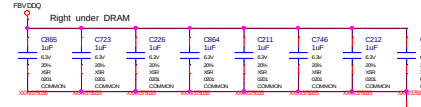
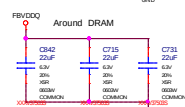
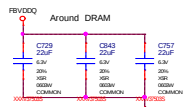
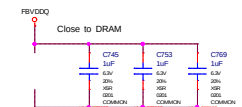
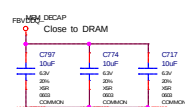
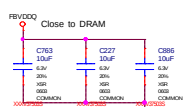
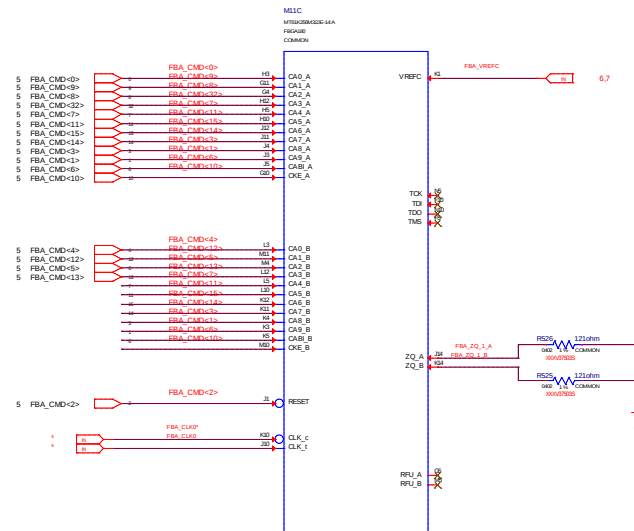
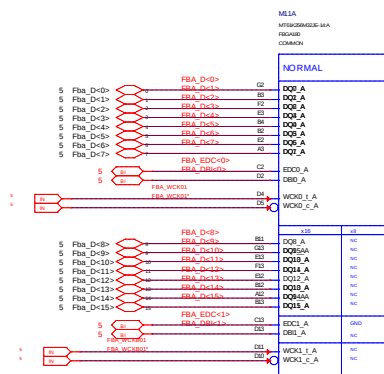
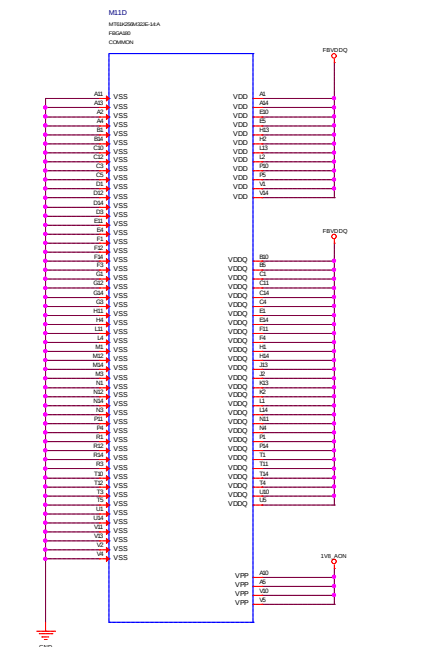
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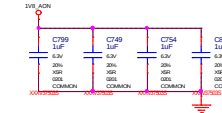
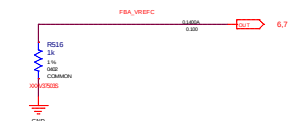


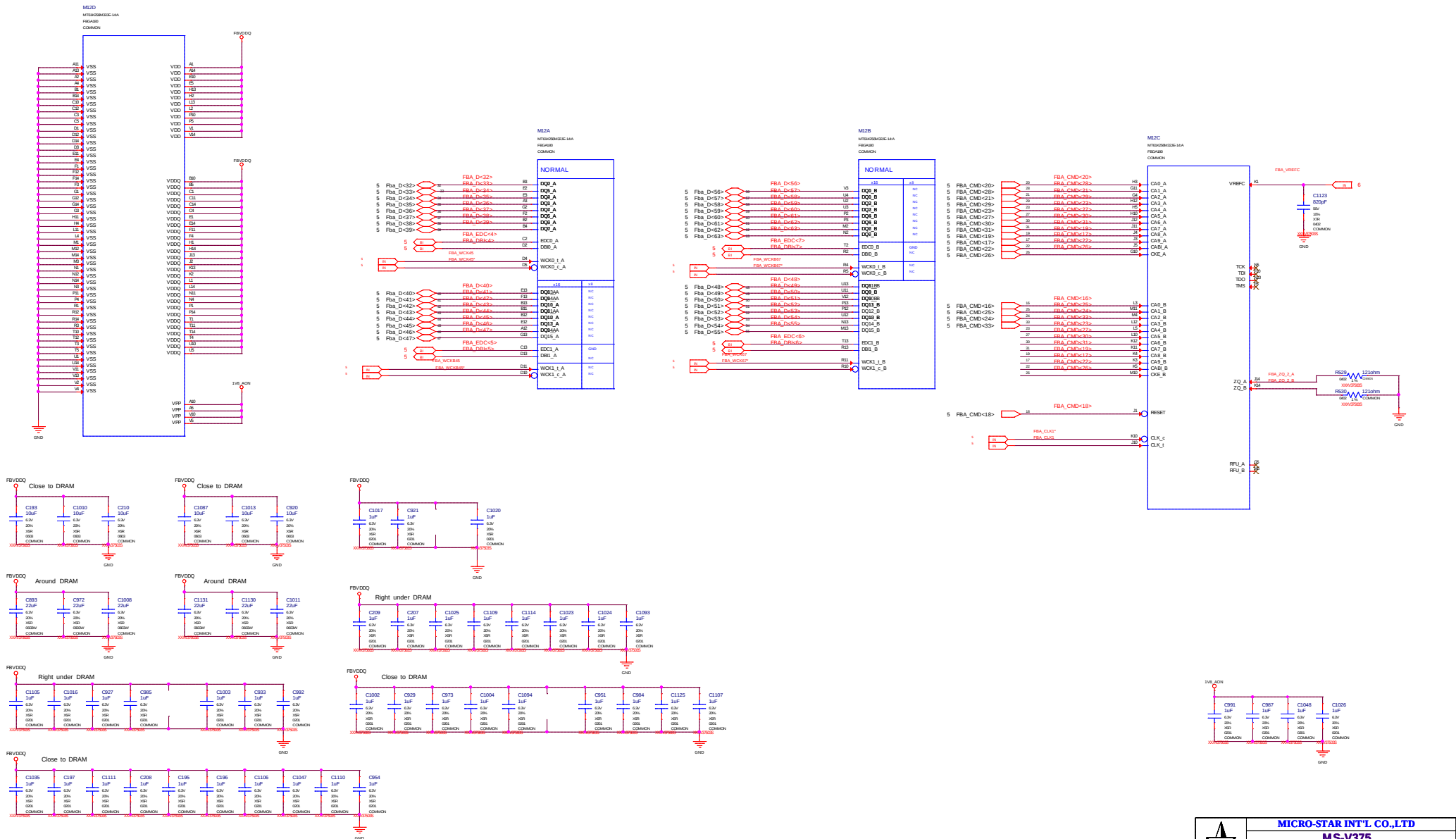
NO PEX GEN4 SUPPORT
DELETE RC TERMINATIONS

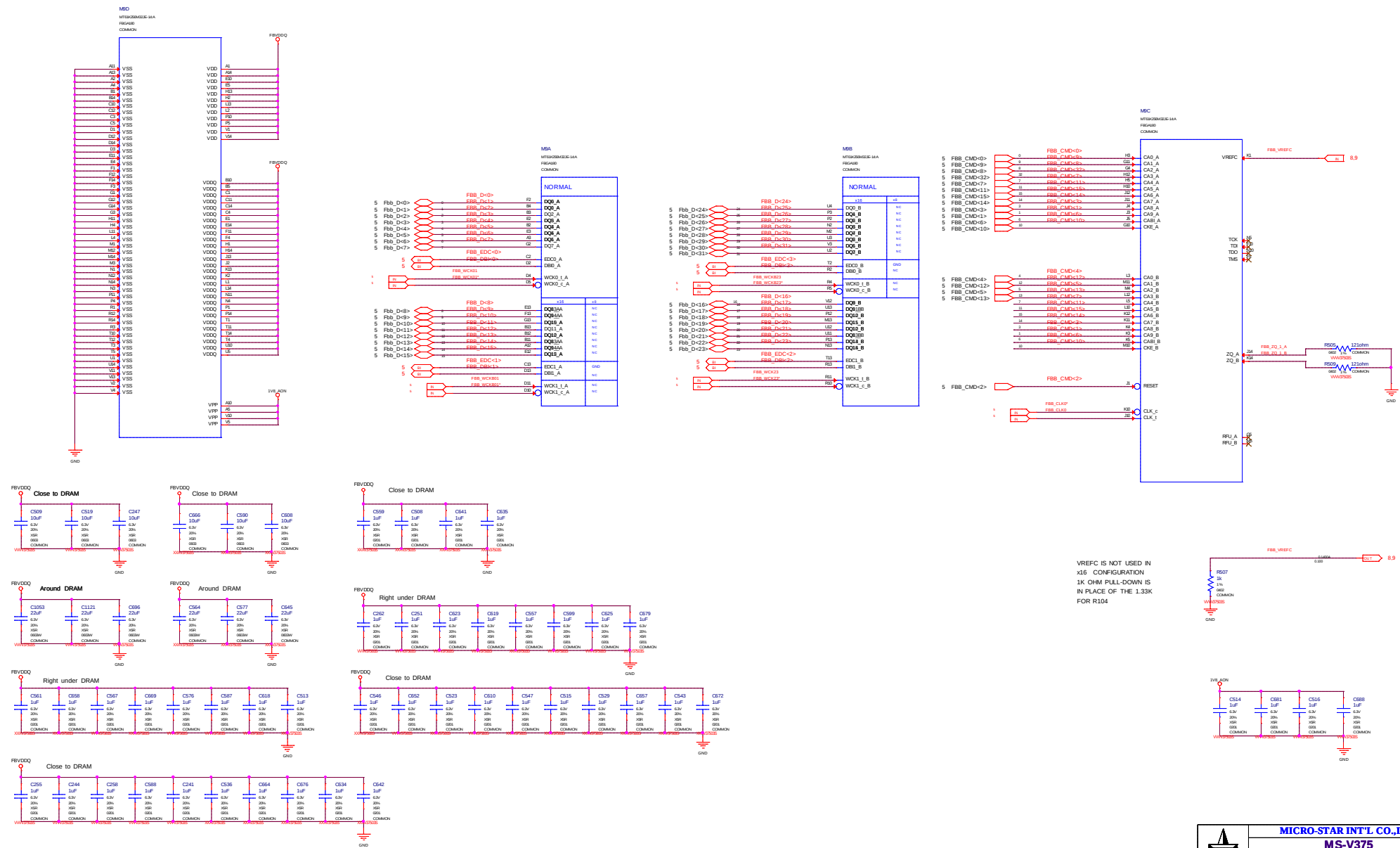




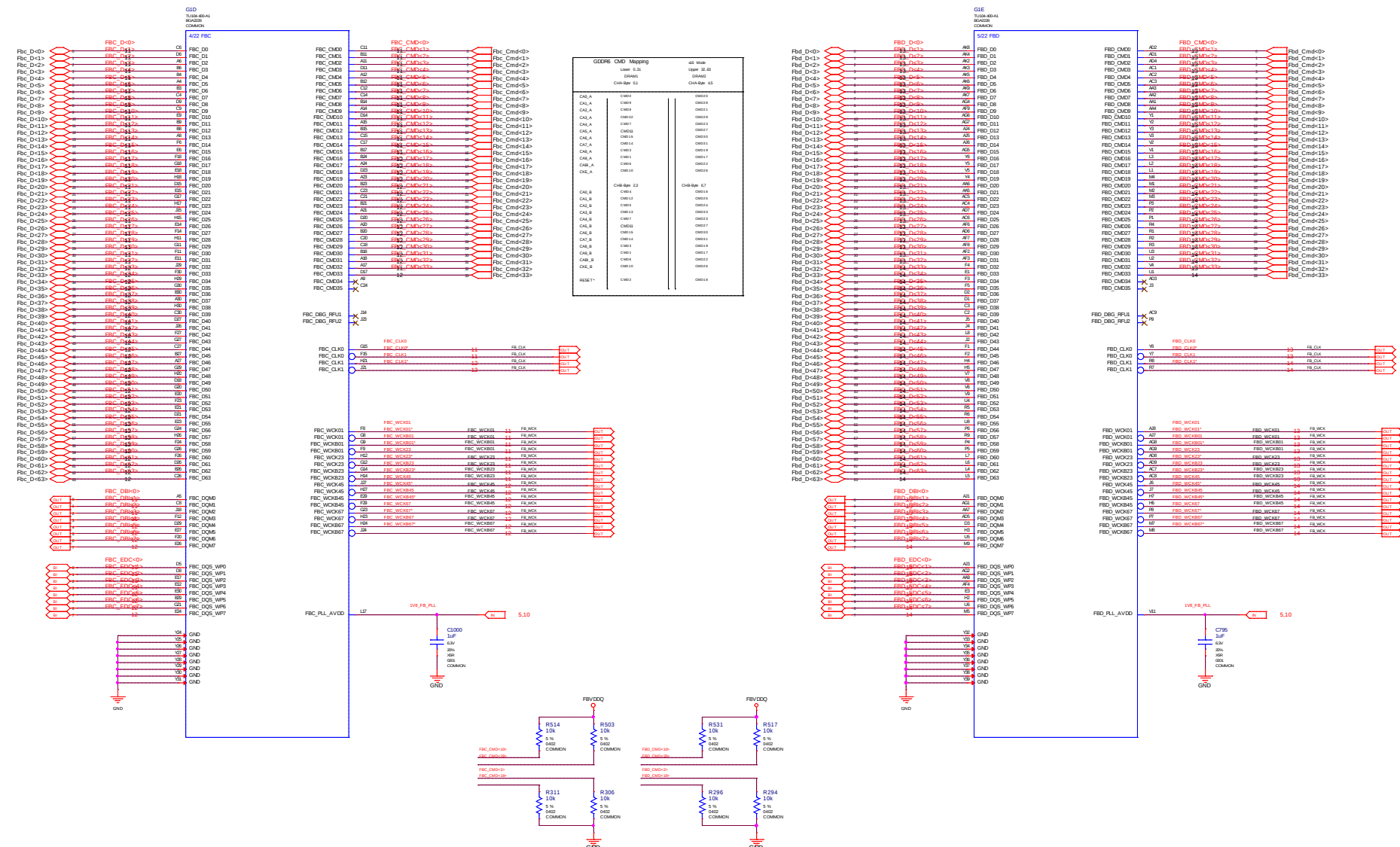
VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R106

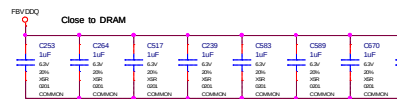
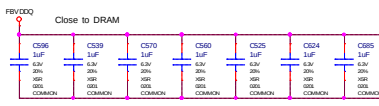
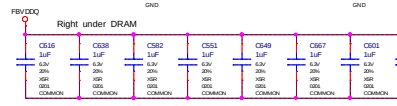
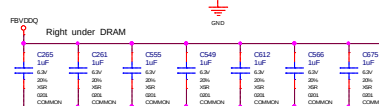
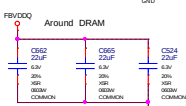
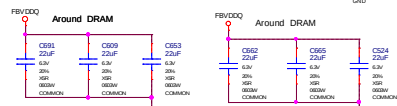
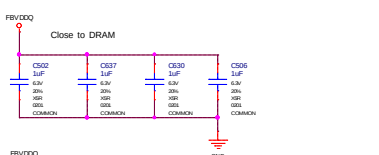
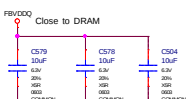
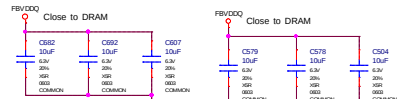
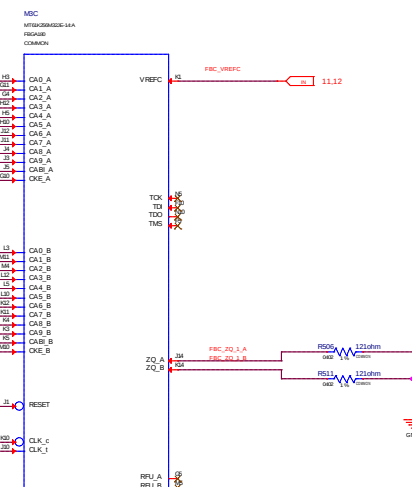
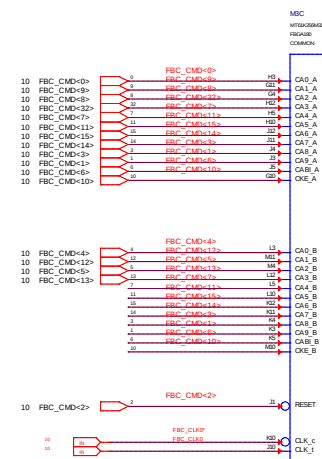
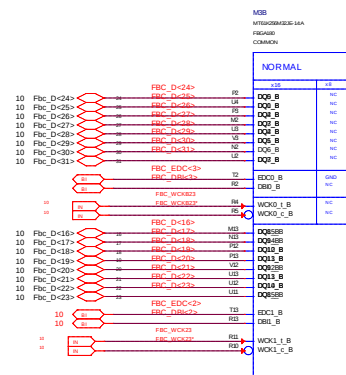
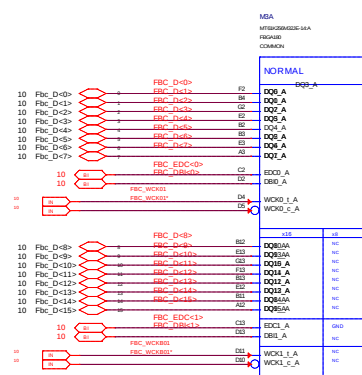
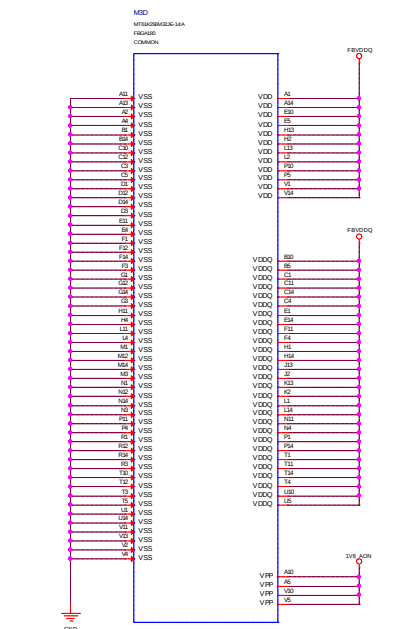




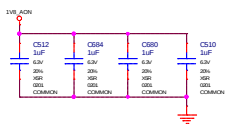


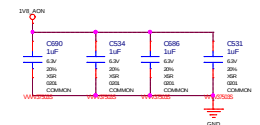
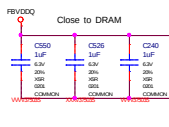
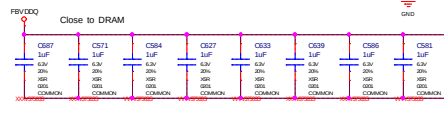
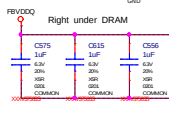
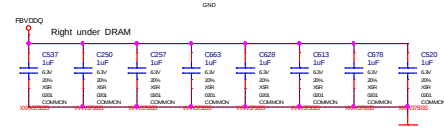
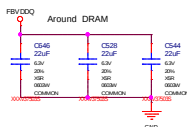
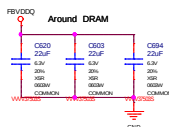
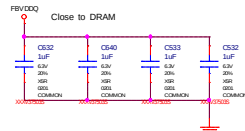
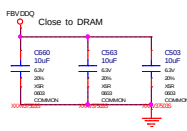
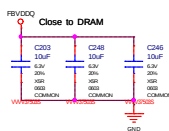
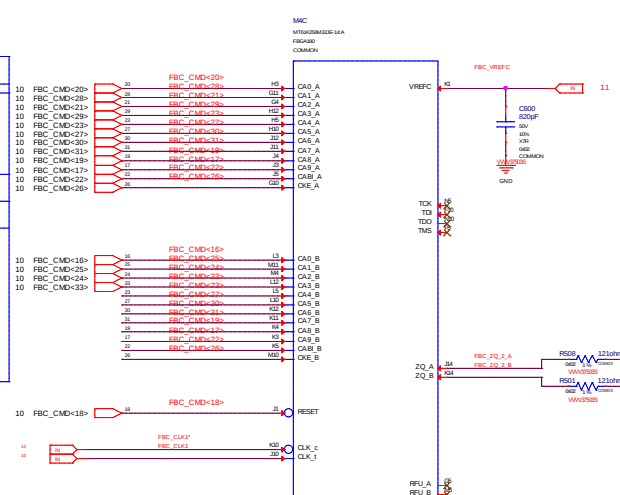
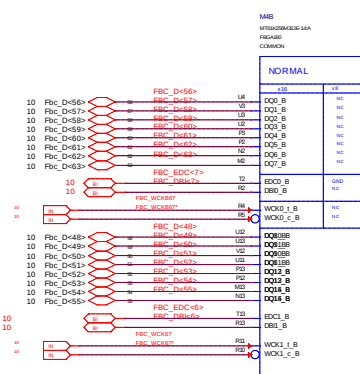
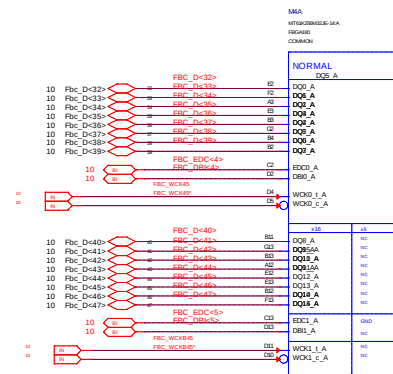
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x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R104

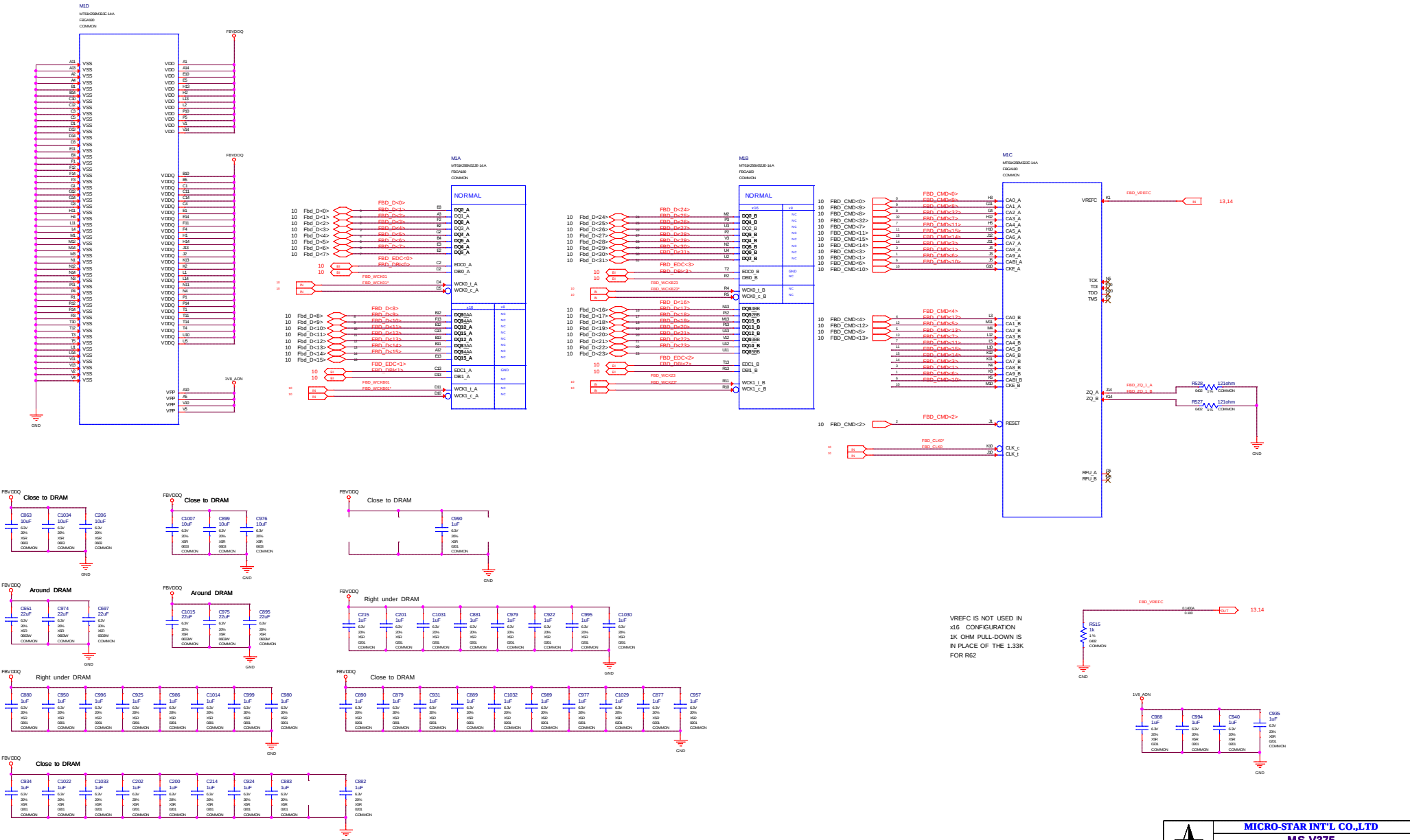


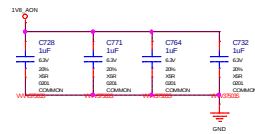
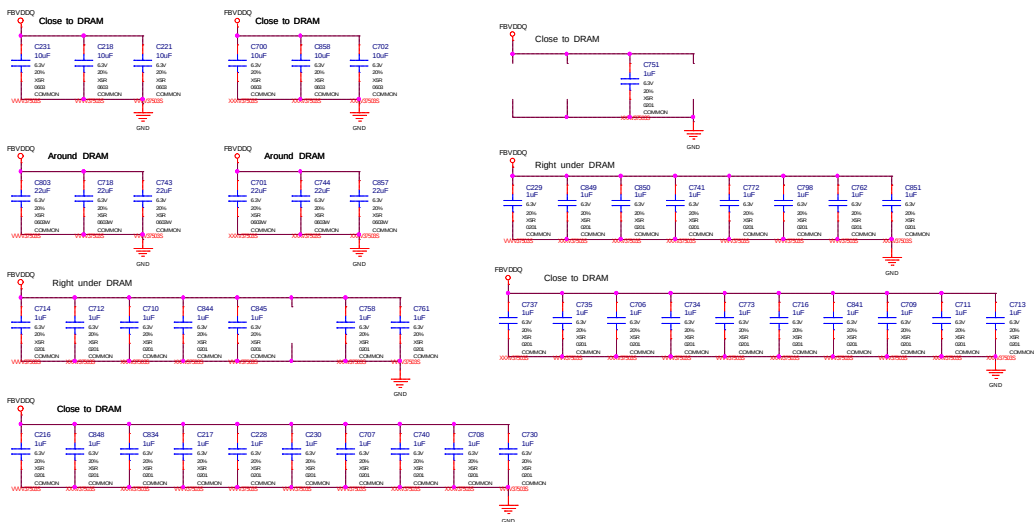
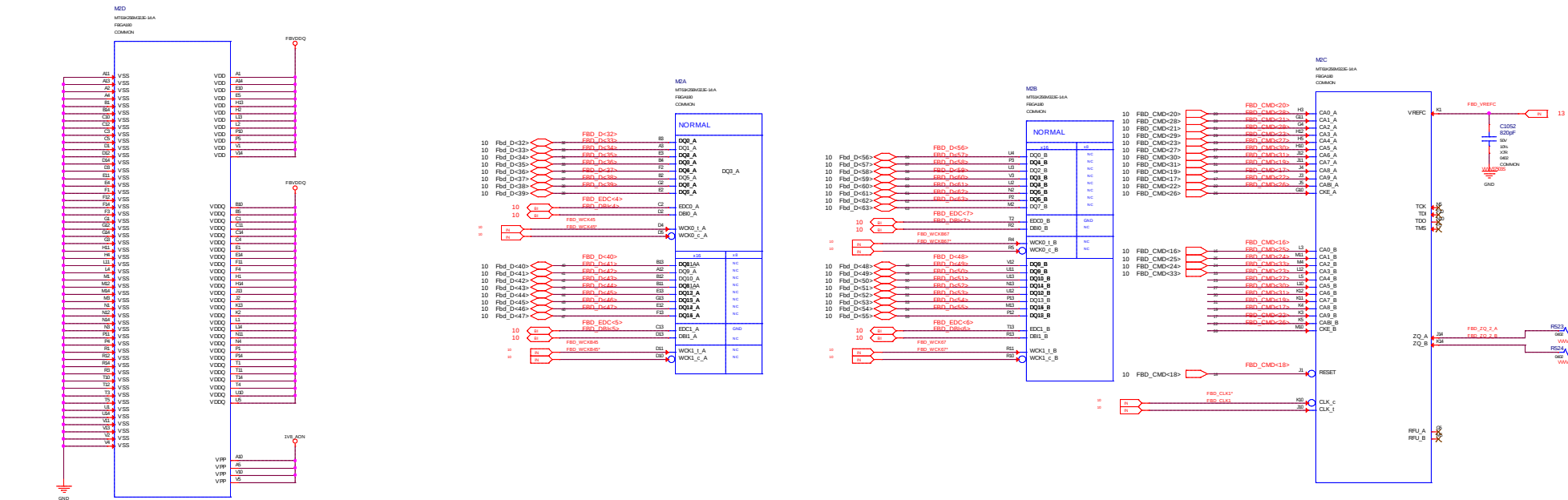


VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R75







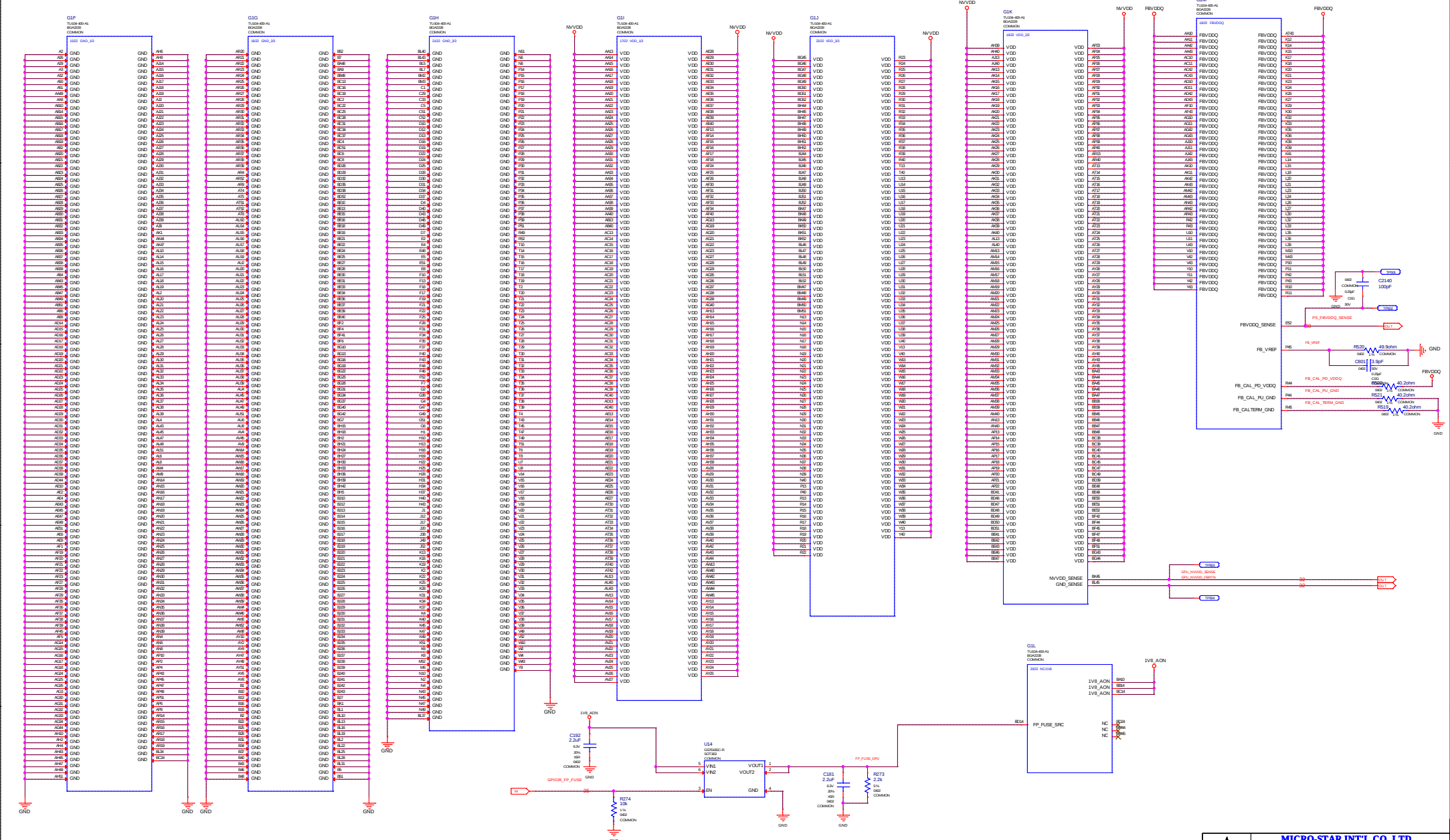


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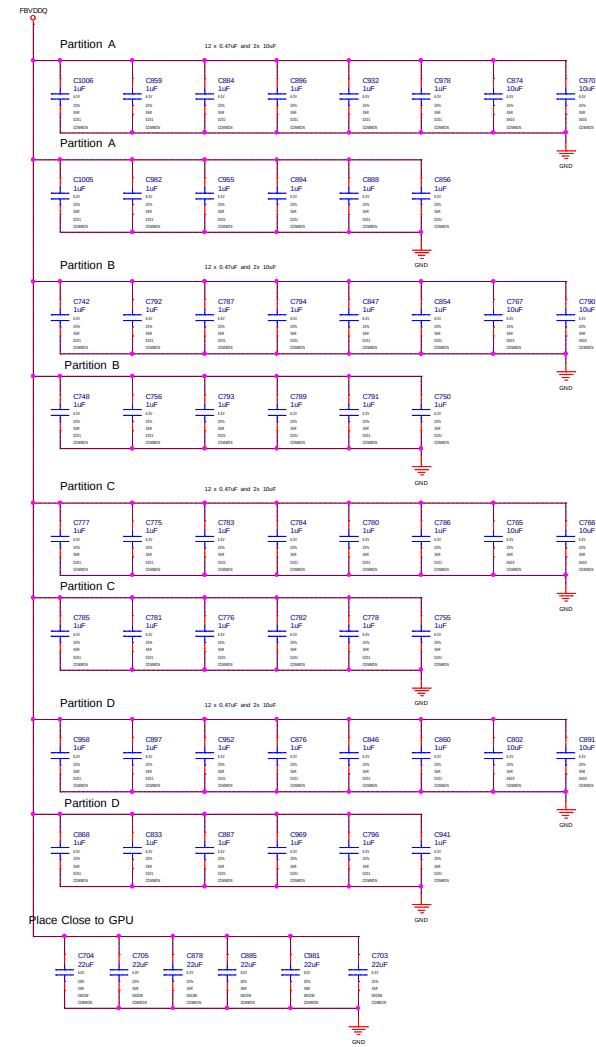
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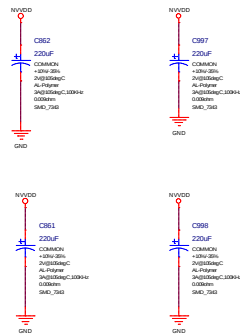
Custom	MEMORY: FBD Partition 63..32	2.0
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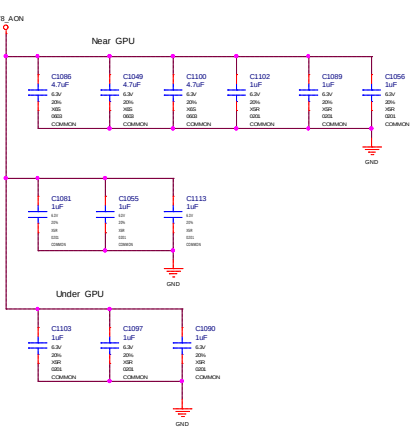
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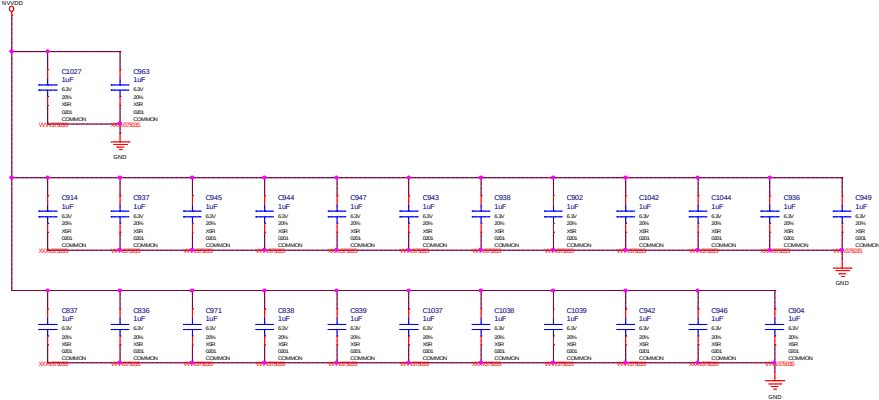
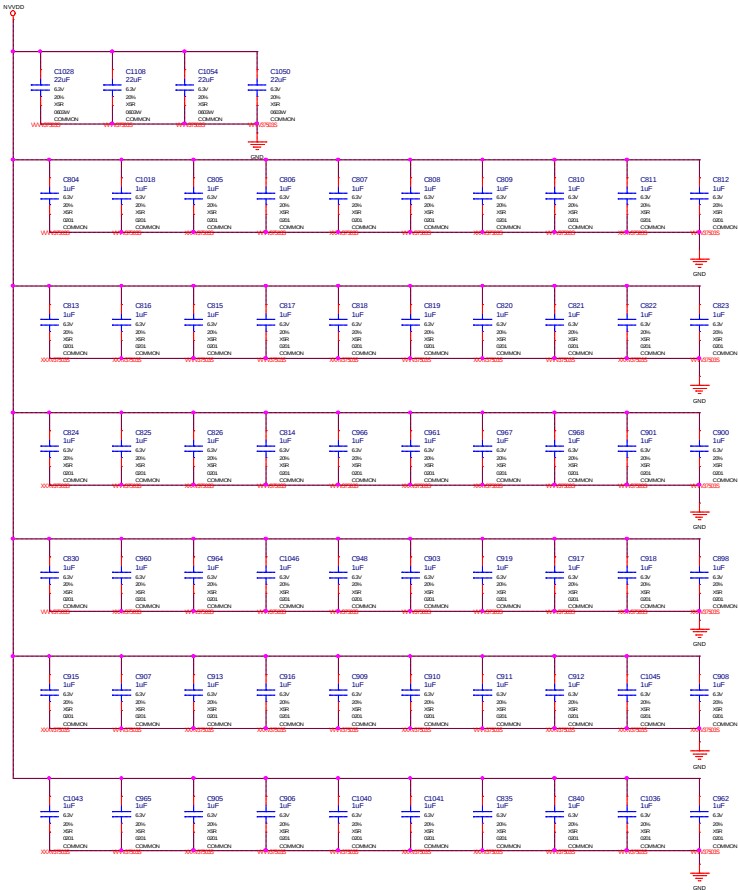
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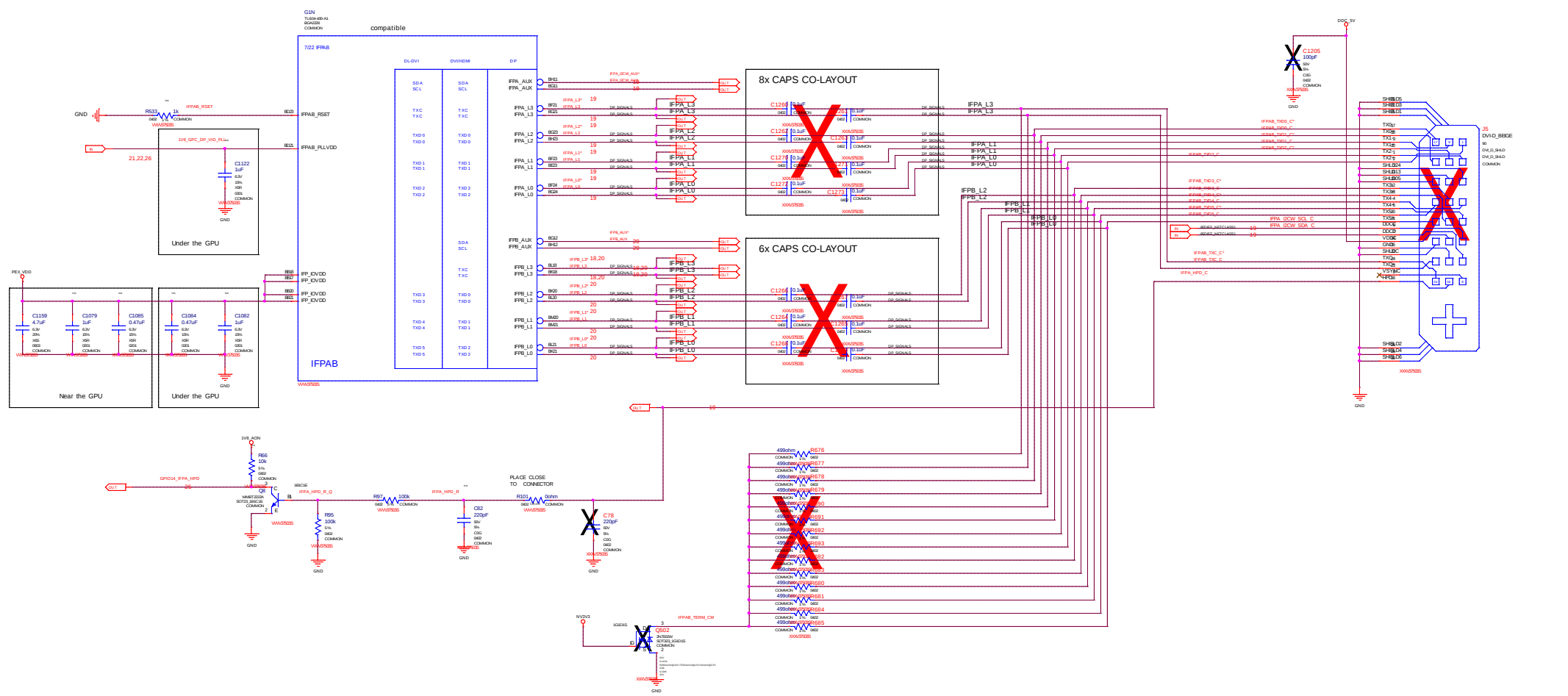
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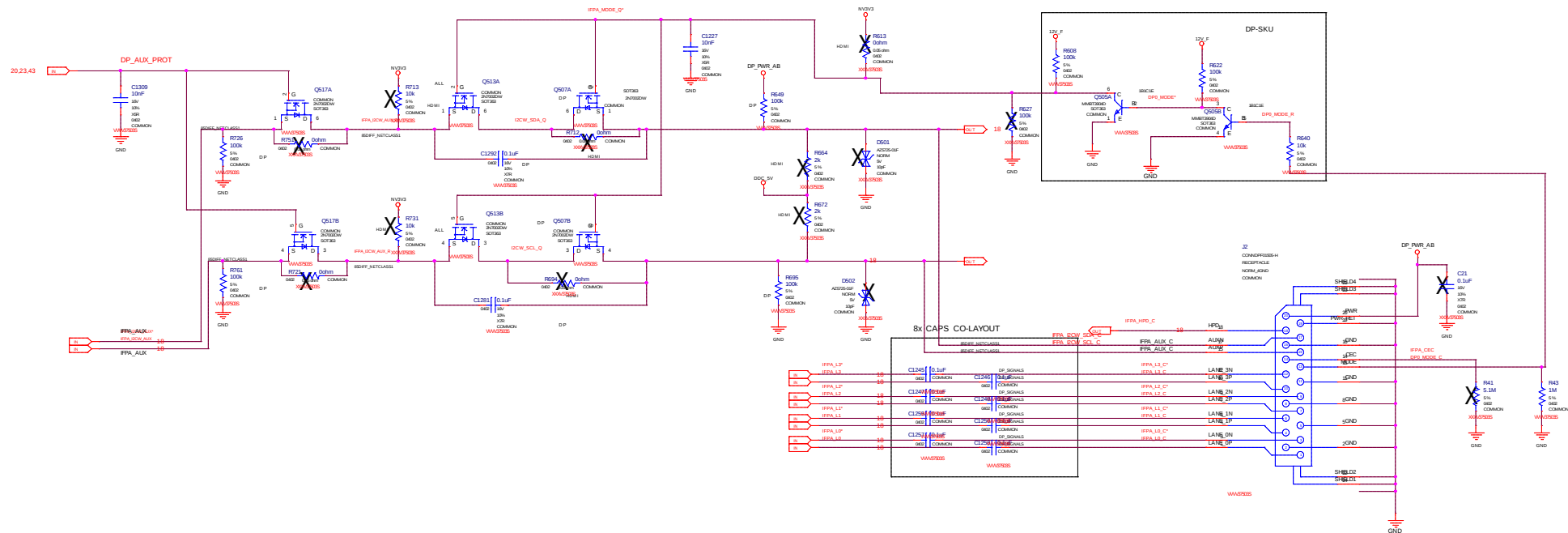


NVDD



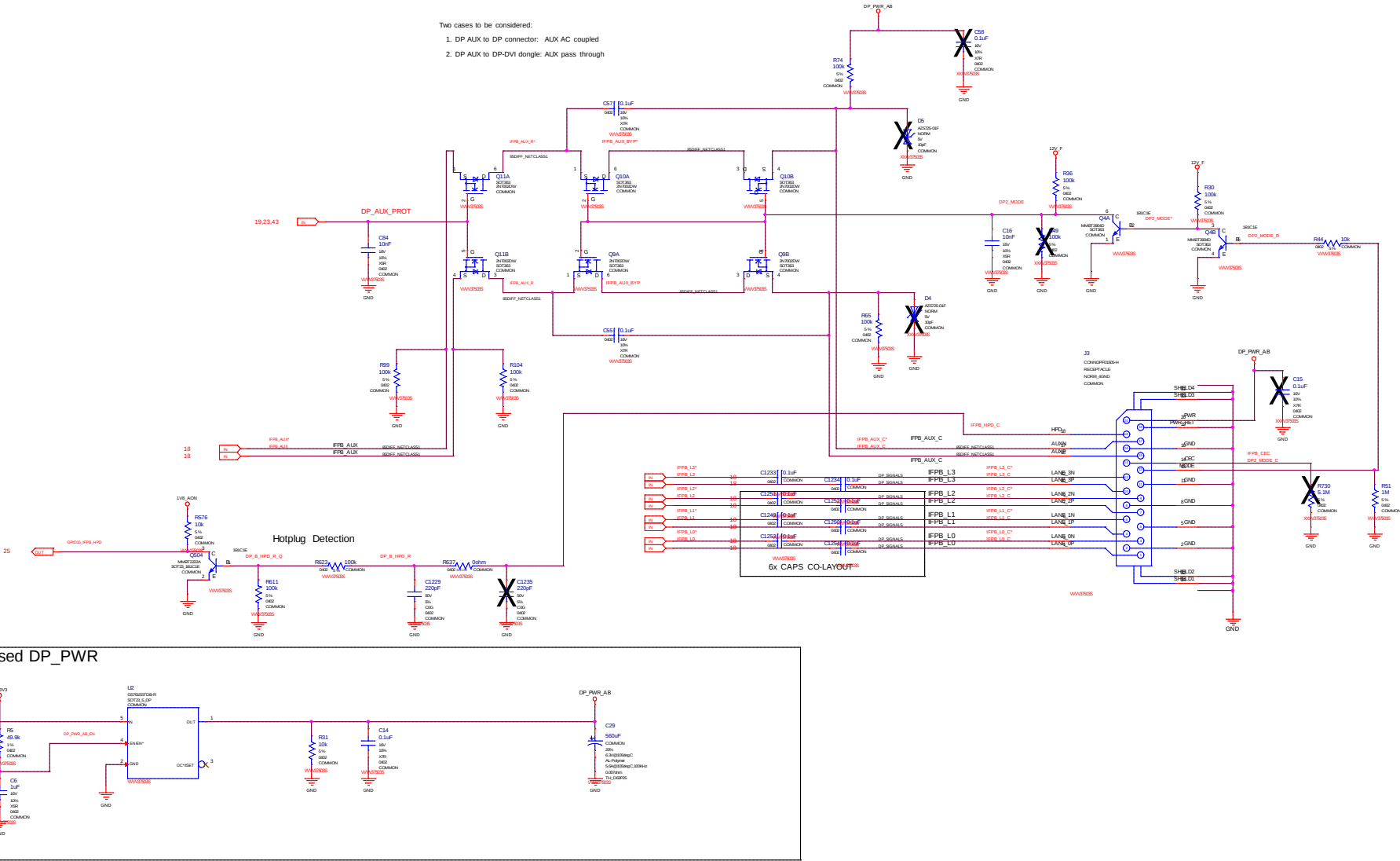
IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP





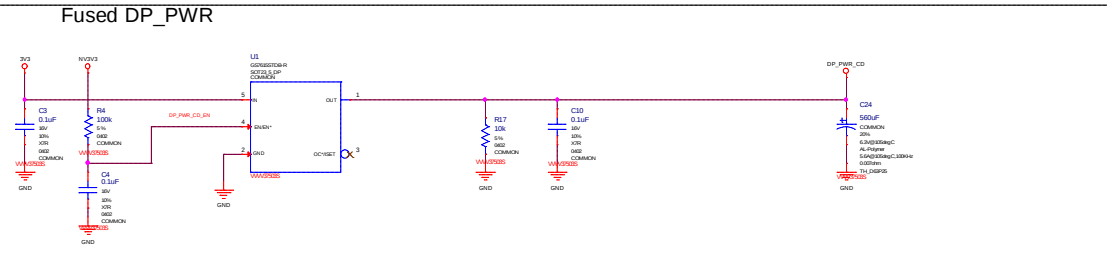
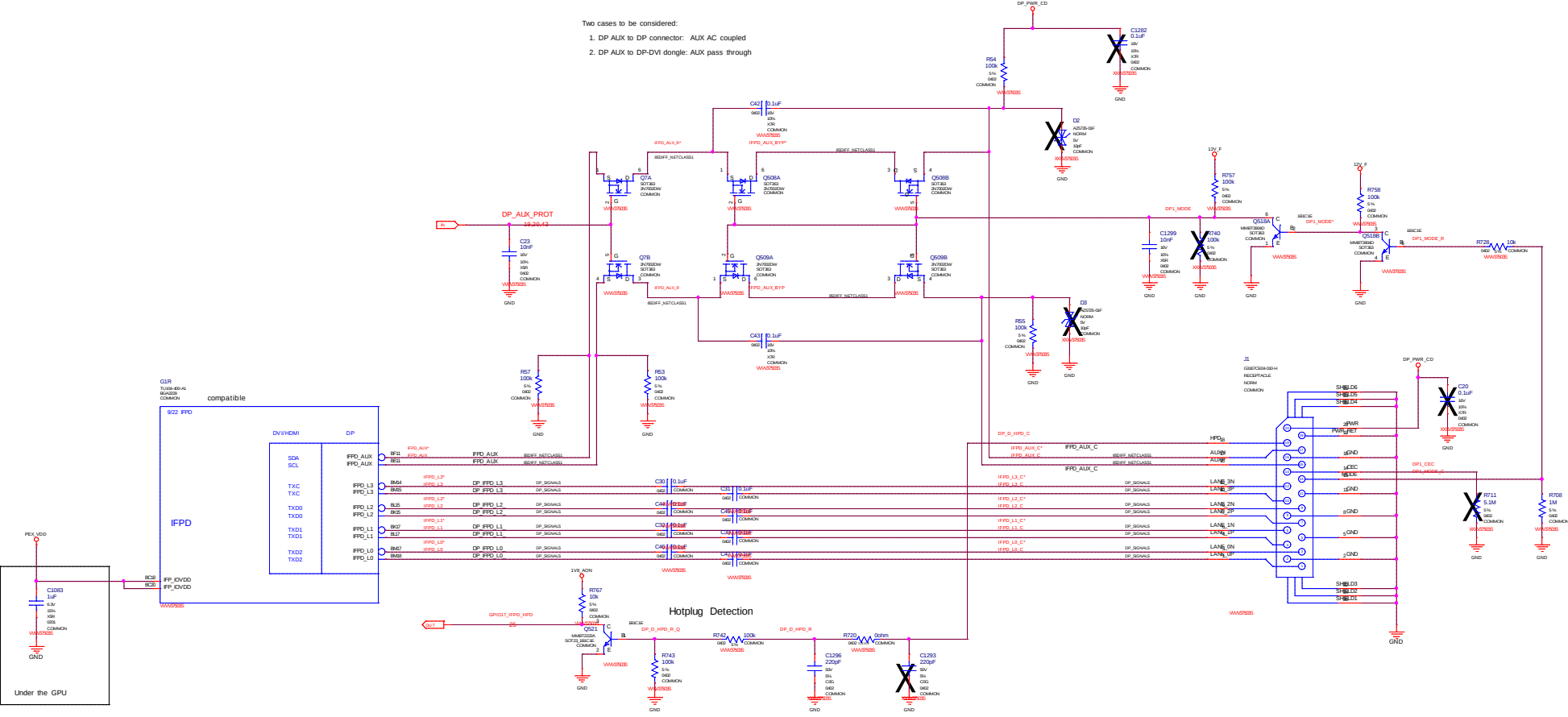
IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL

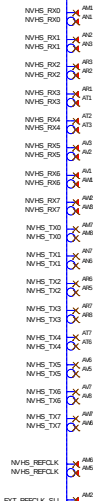
- Two cases to be considered:
- 1. DP AUX to DP connector: AUX AC coupled
 - 2. DP AUX to DP-VI dongle: AUX pass through

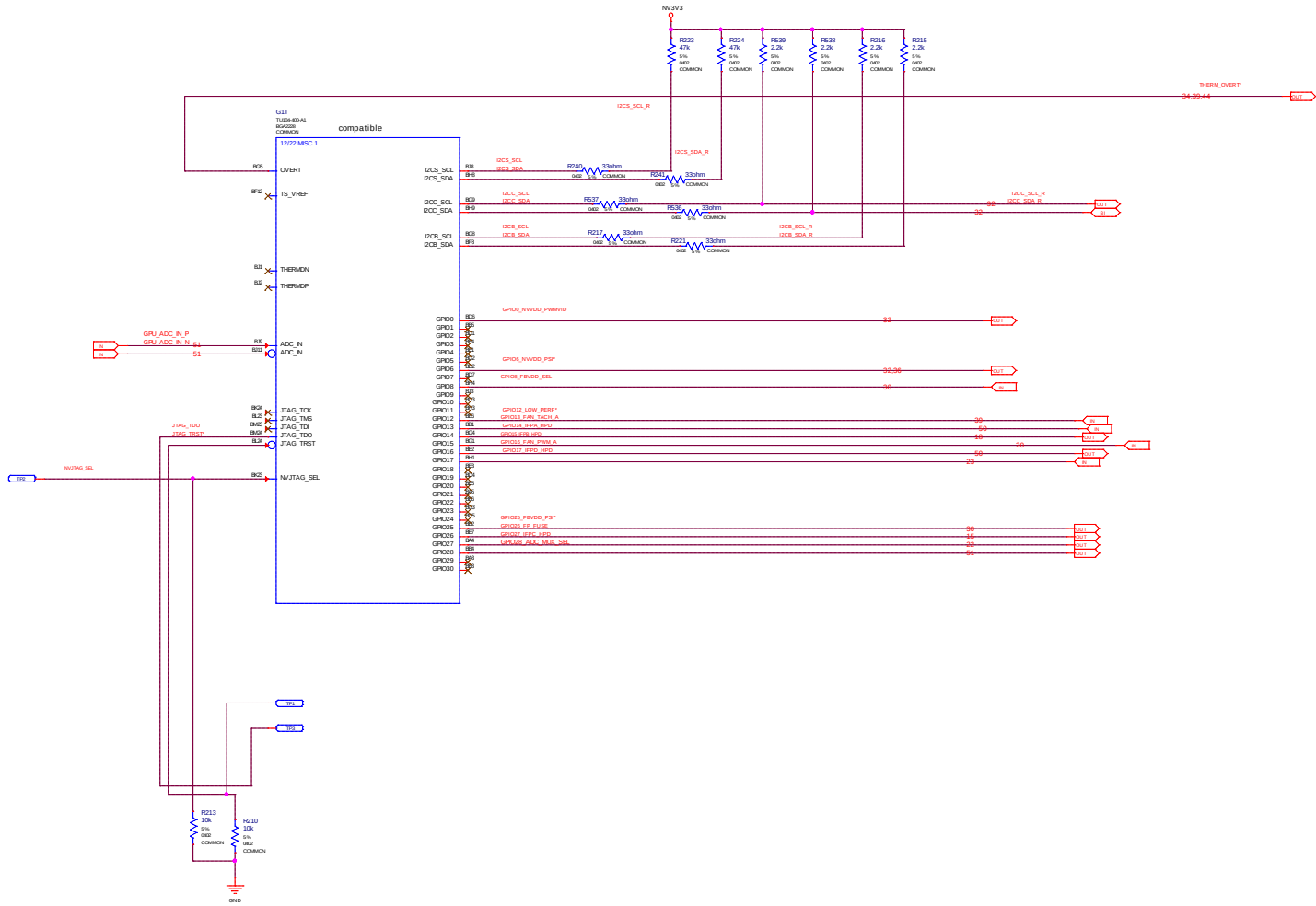




Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through







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Doc	Document	Description	Rev
Custom	MISC1: Fan, Thermal, JTAG, GPIO		2.0
Date: Tuesday, December 04, 2018		Sheet	25 of 53

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00110	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]FS_OVERT	1ENABLE 0DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

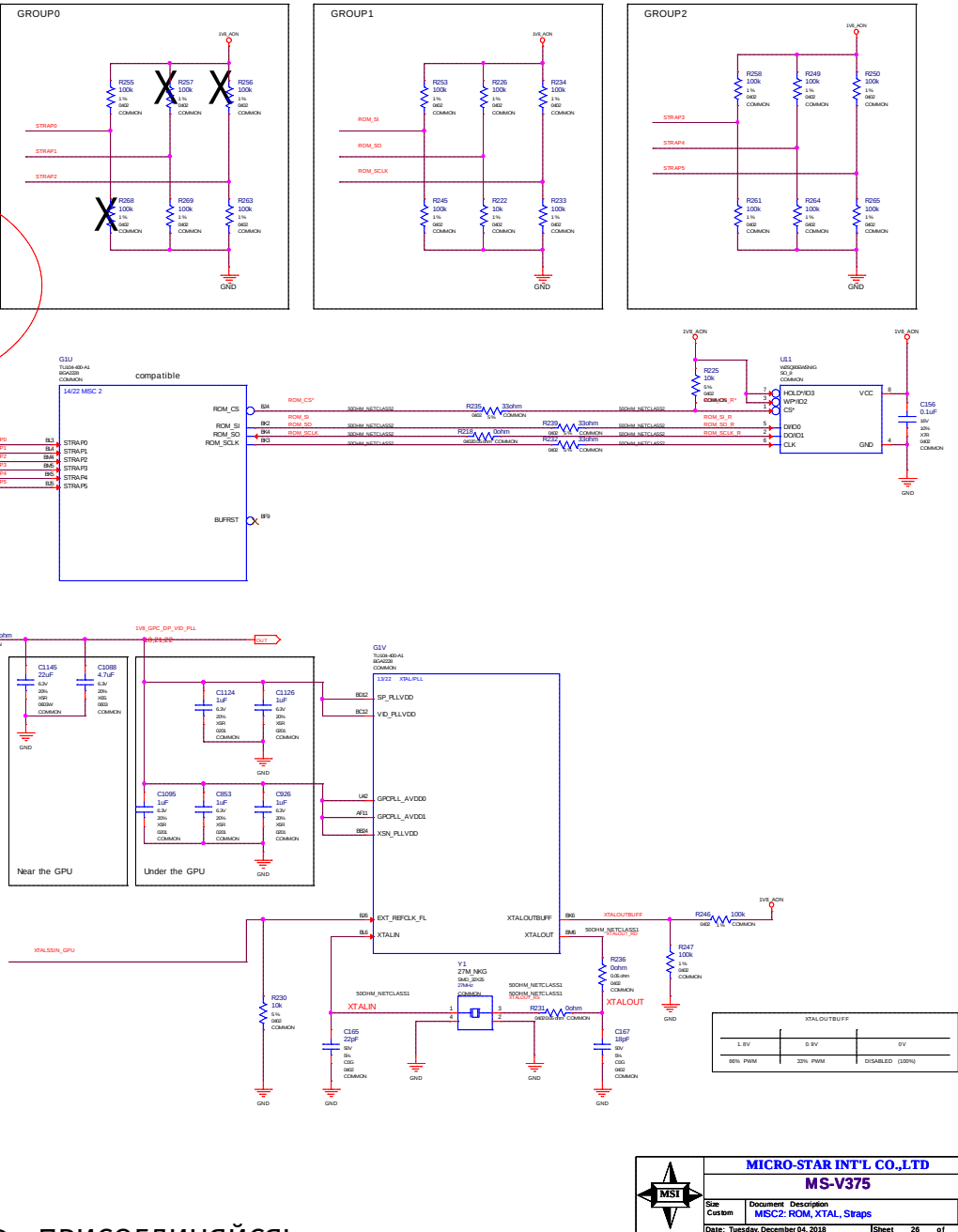
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

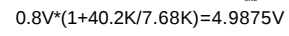
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCE_CFG LOW POWER
0:PCE_CFG HIGH POWER

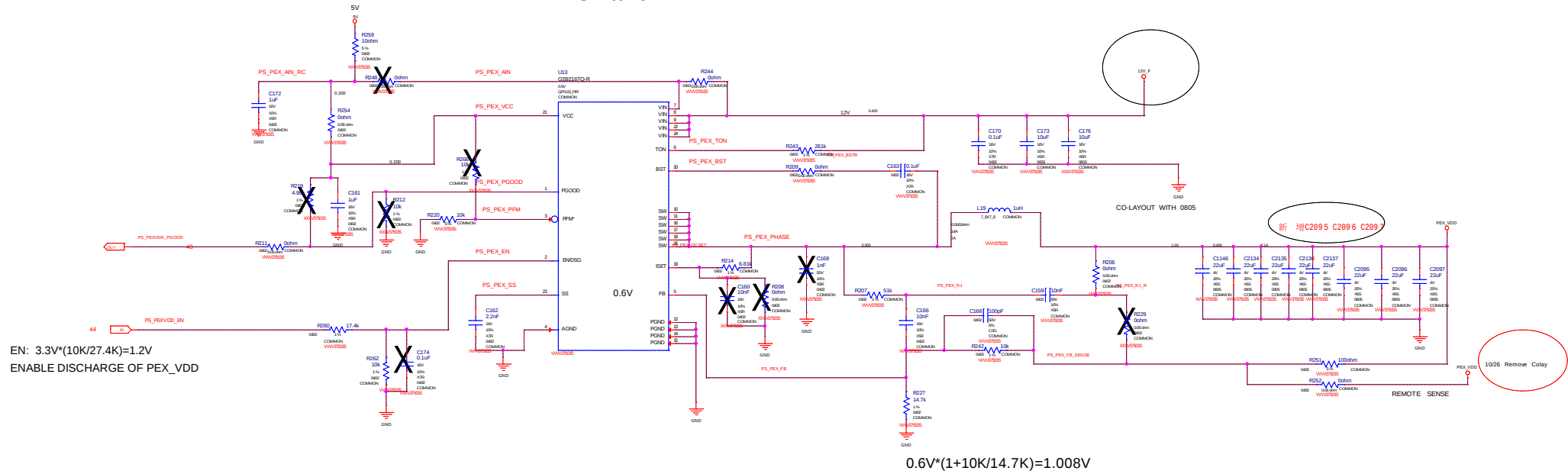
1:VGA_DEVICE ENABLE
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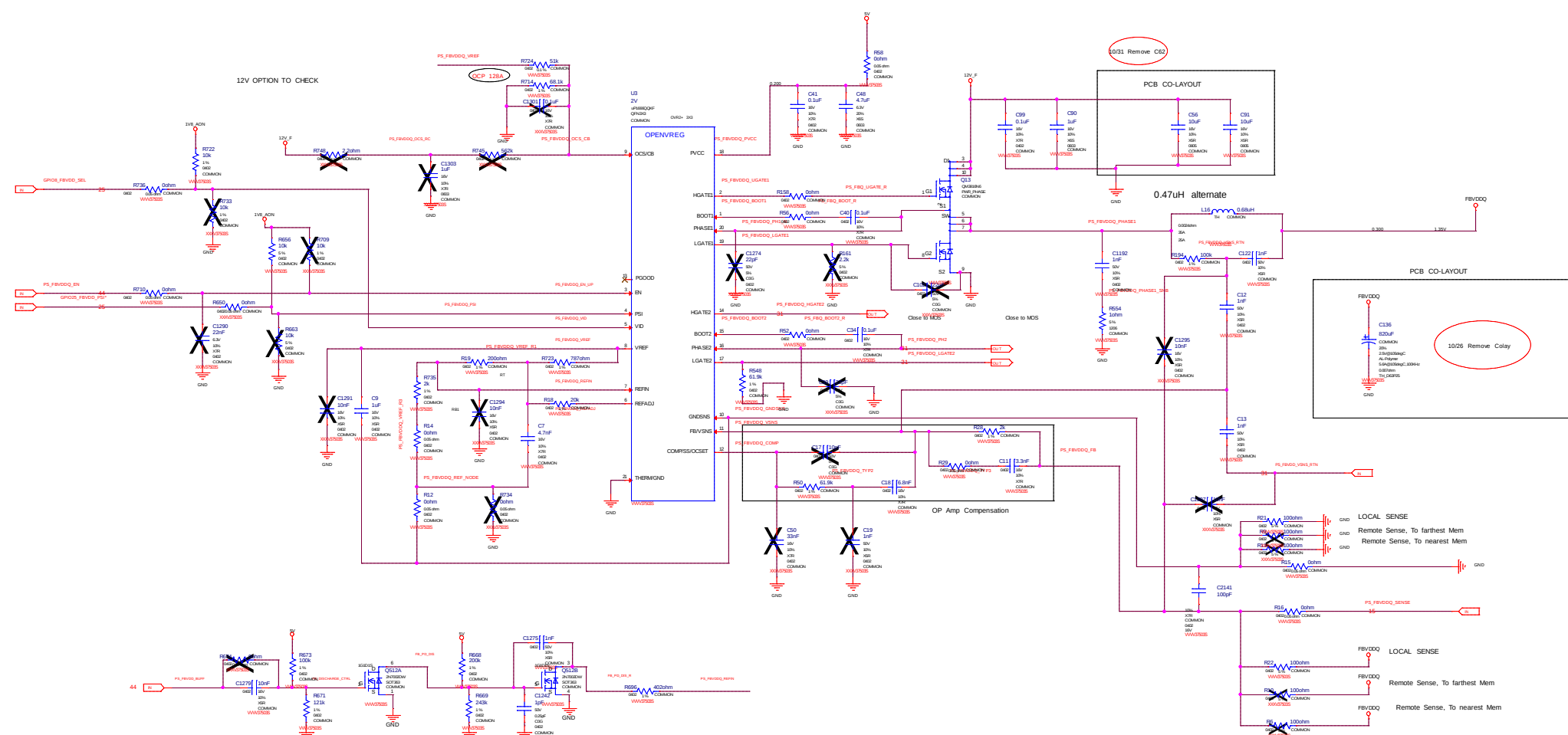
注意 上 件 的 MEM Straps

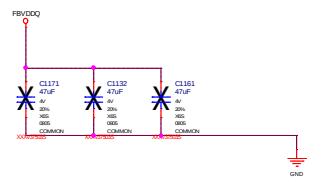
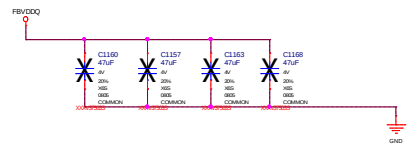
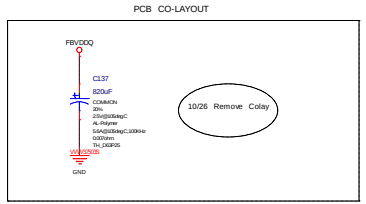
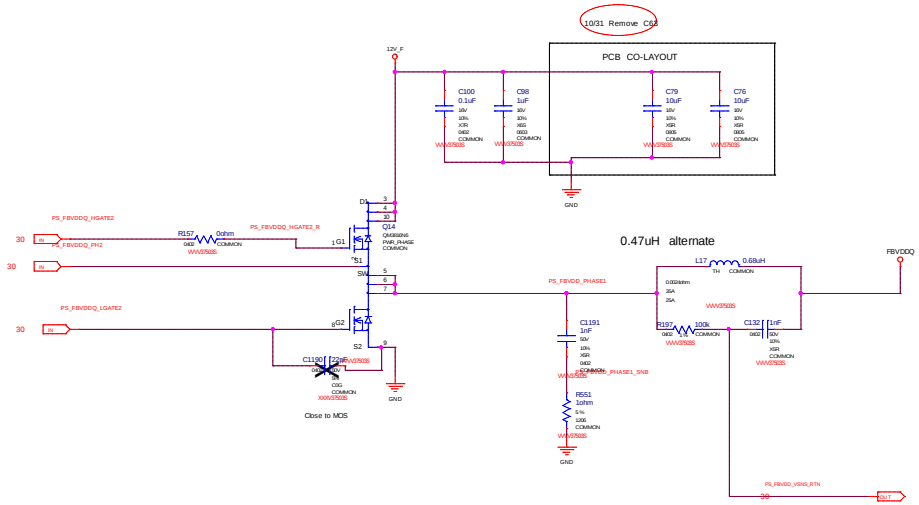


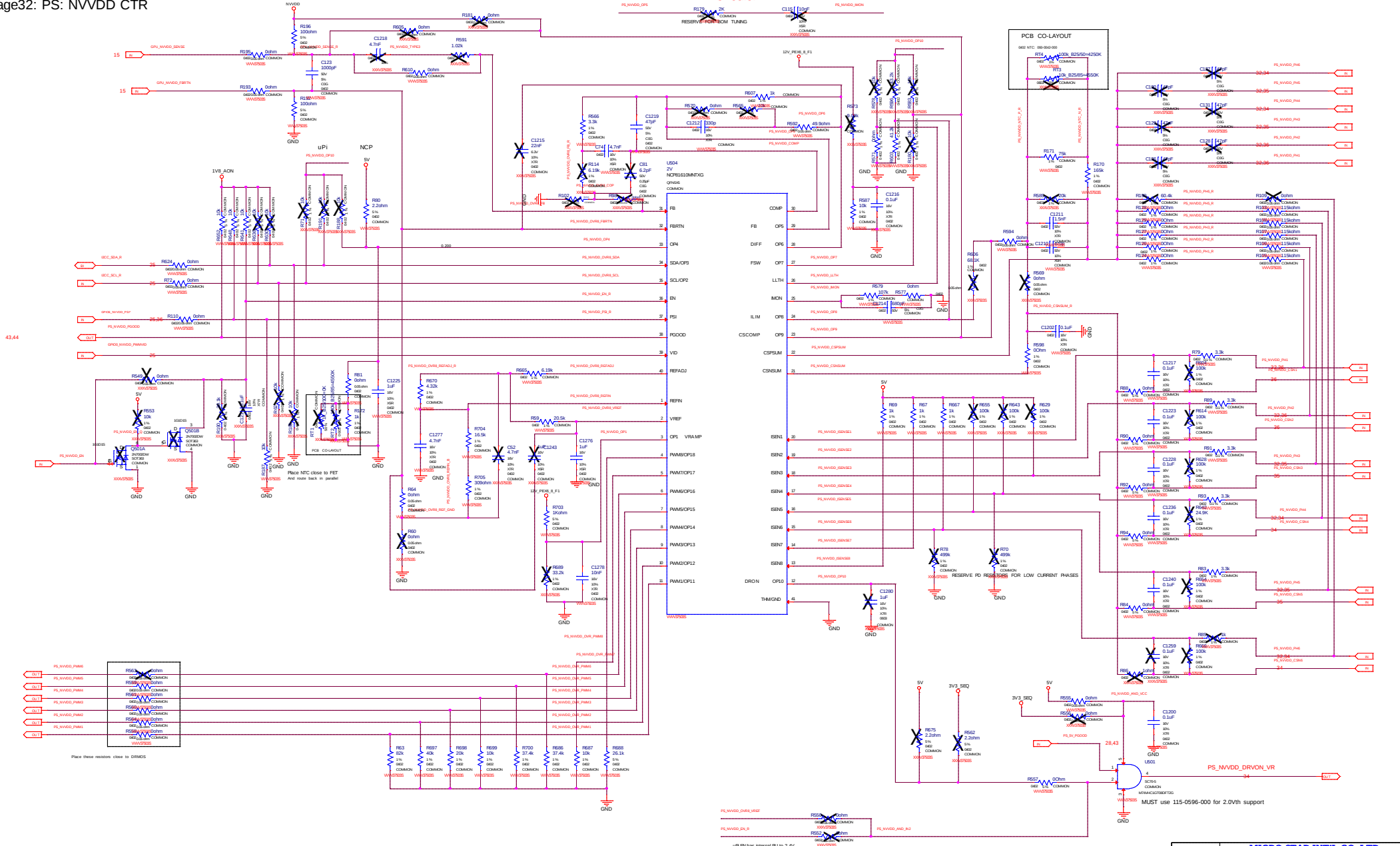


PEX Switcher


$$0.6V \cdot (1 + 10K/14.7K) = 1.008V$$







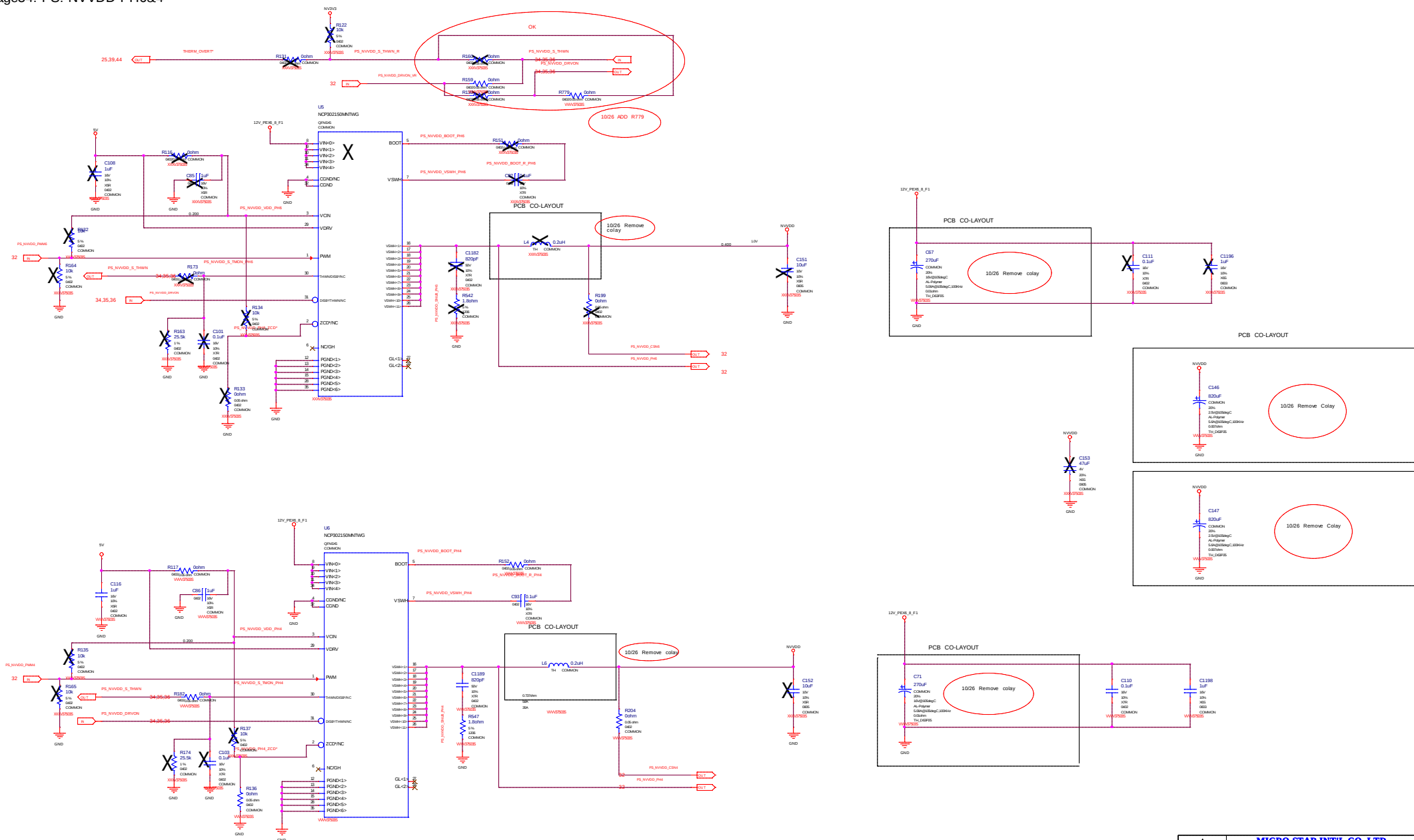
DROP OVR3i SOLUTION

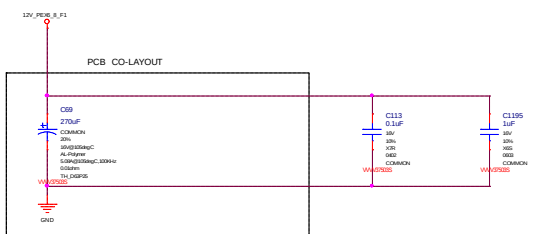
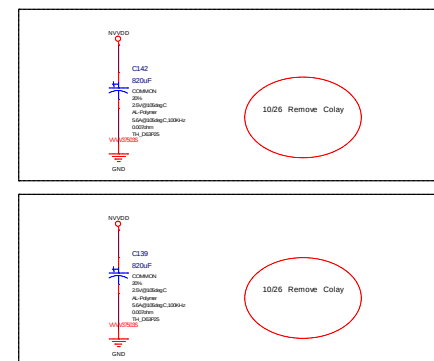
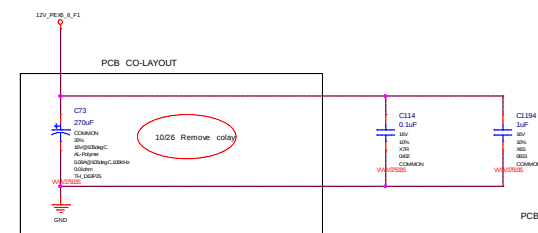
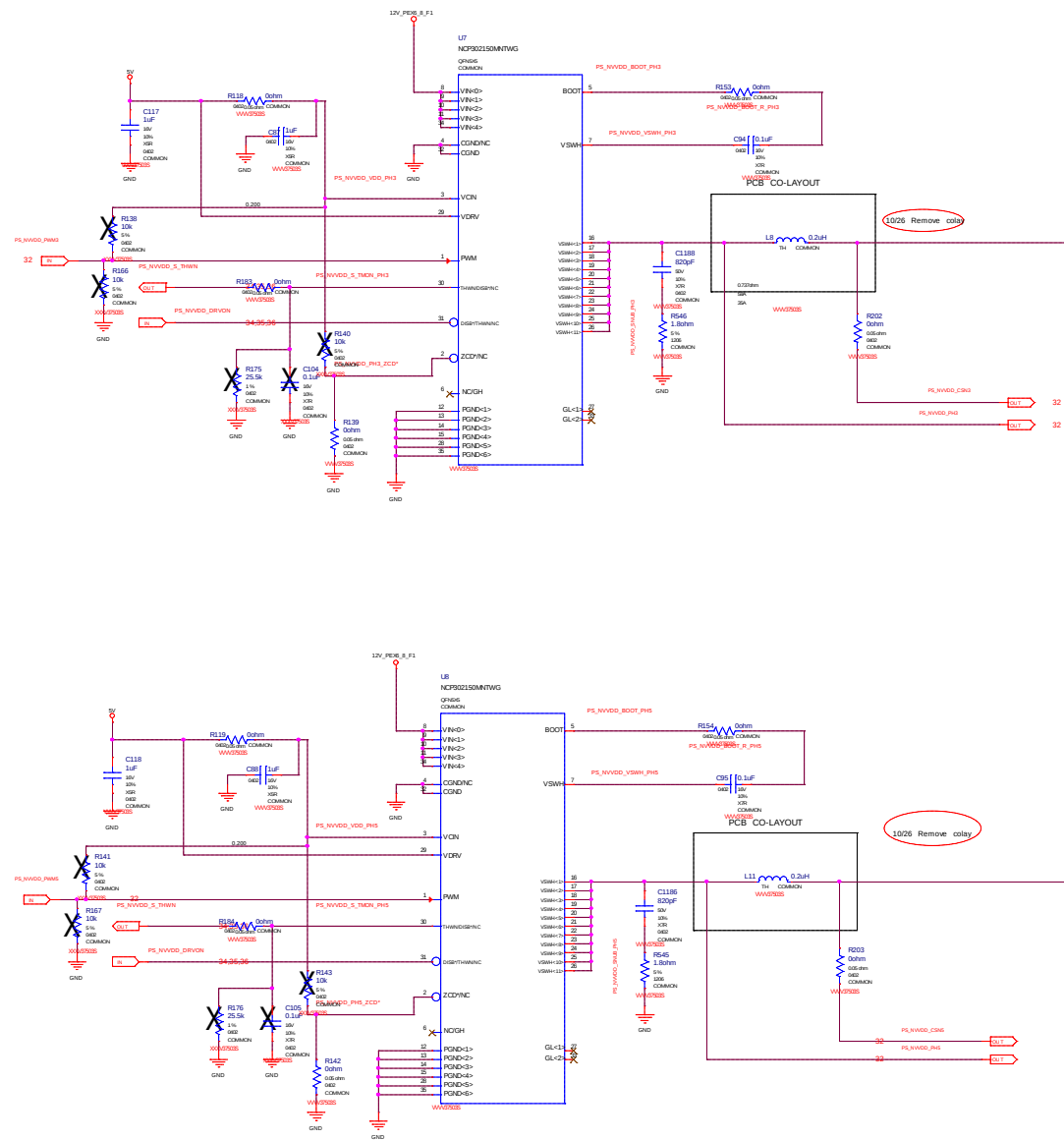


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Size	Document	Description	Rev
Custom	PS: NVVDD CTR	OVR3i	2.0
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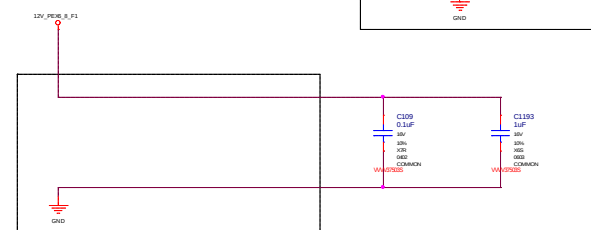
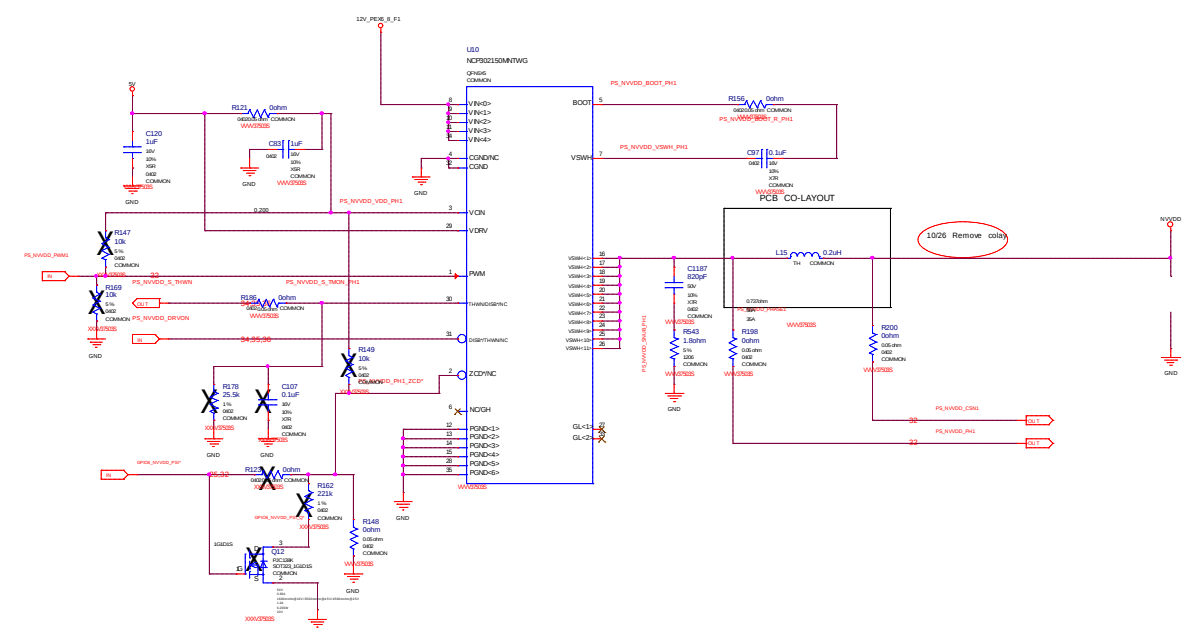
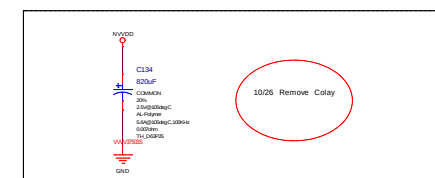
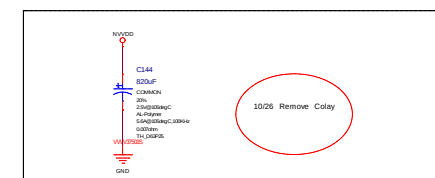
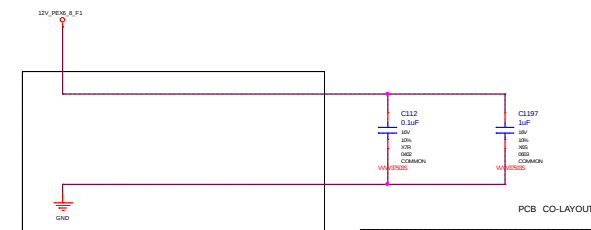
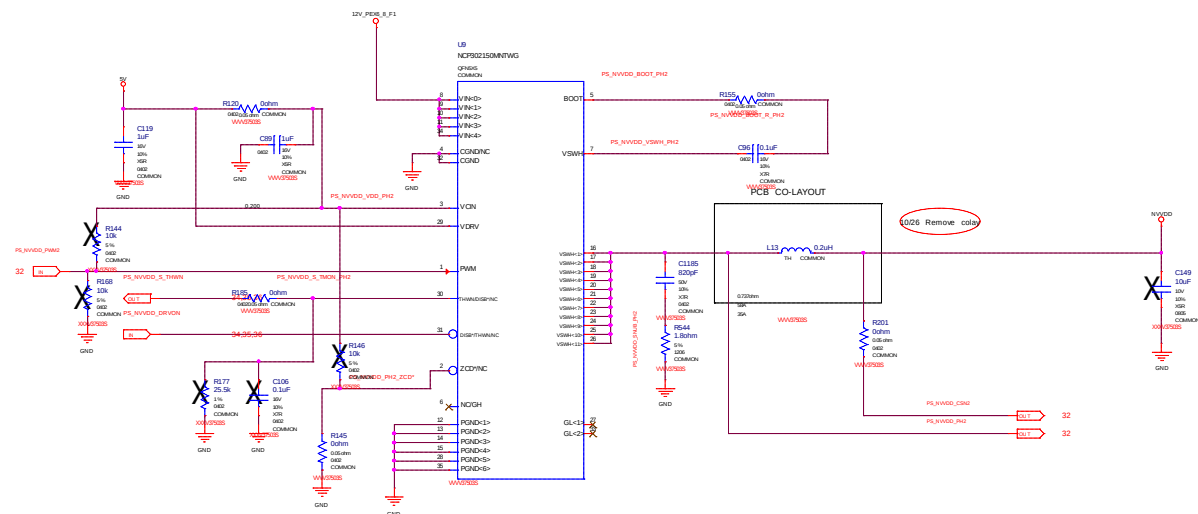


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35m	PS: NVVDD PH3&5		2.0

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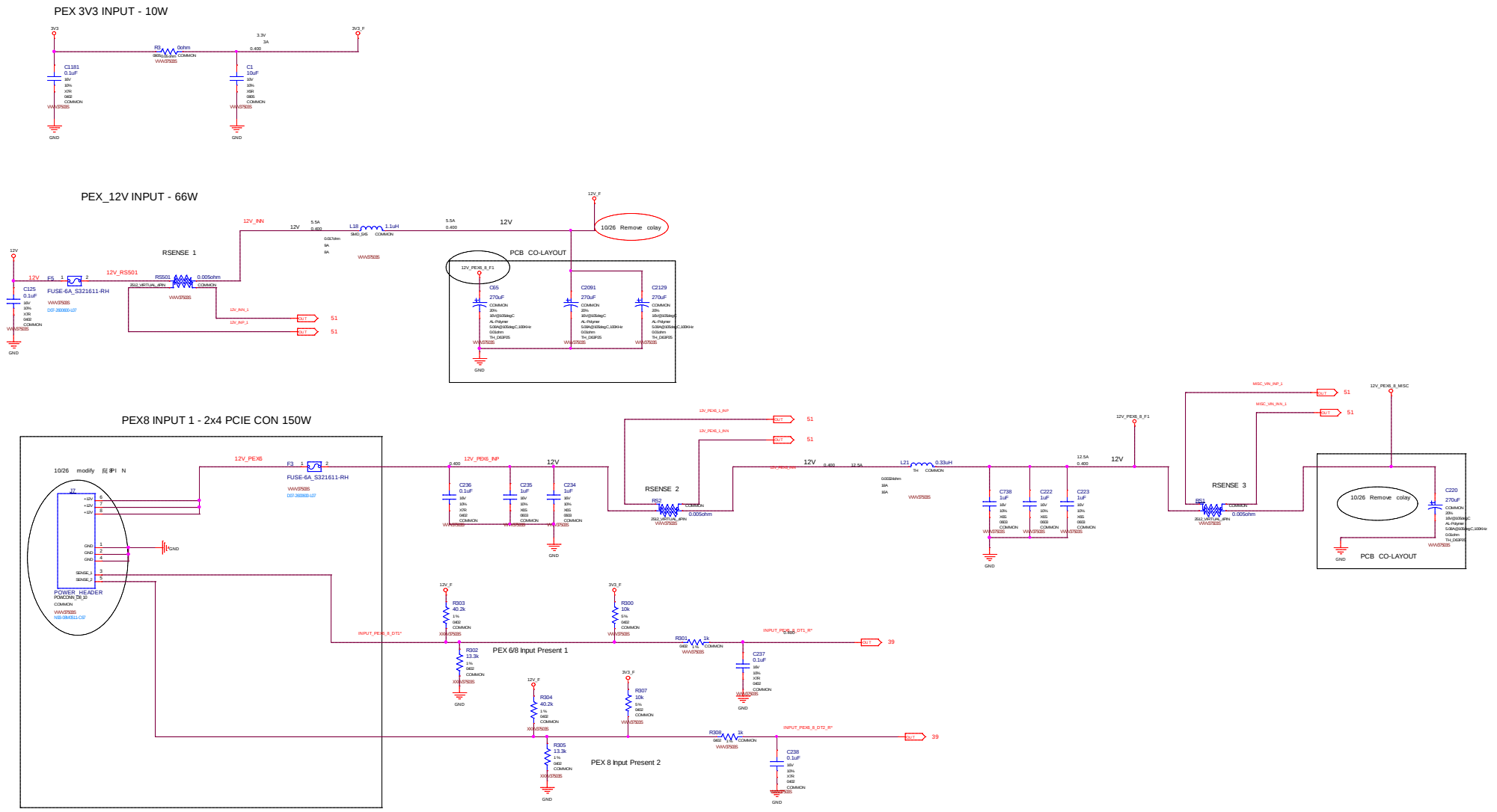
DELETE RAIL BALANCE CIRCUIT

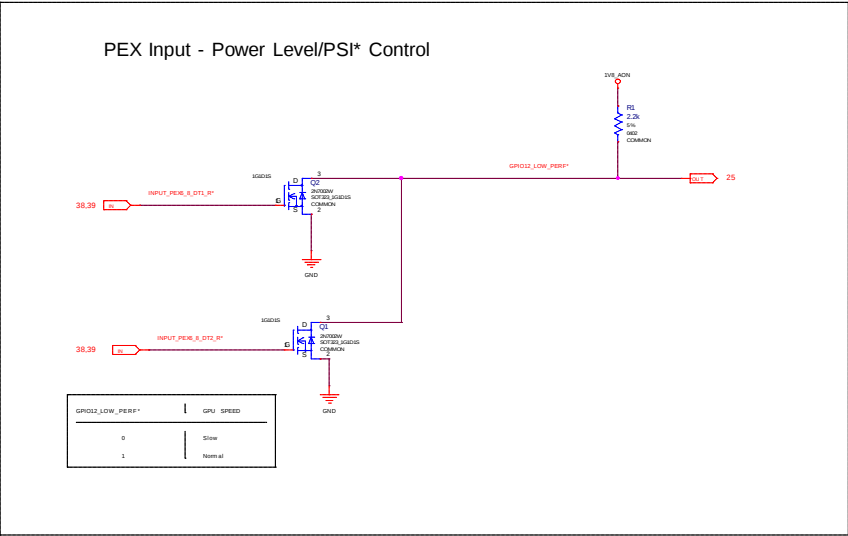
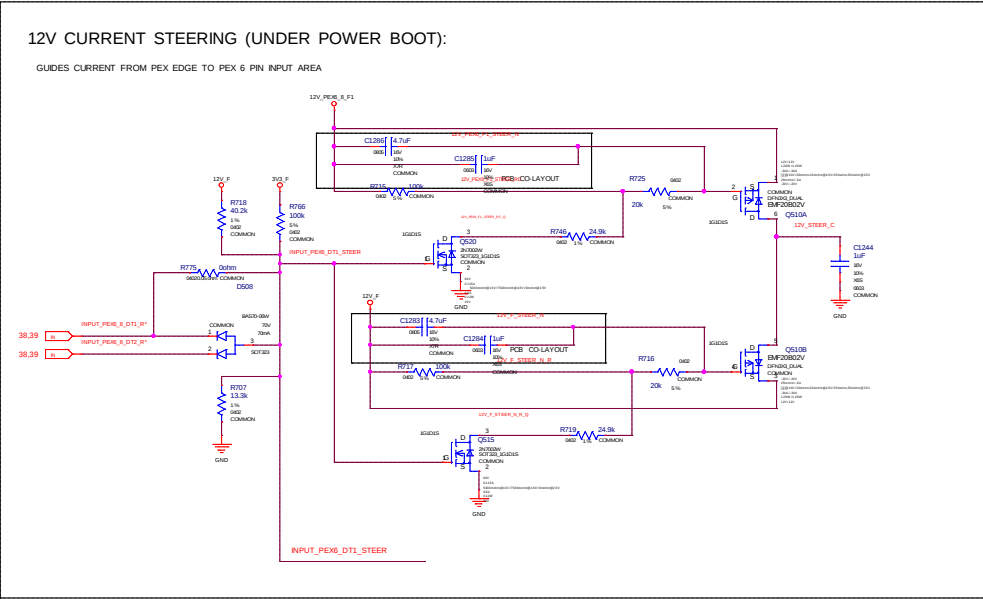
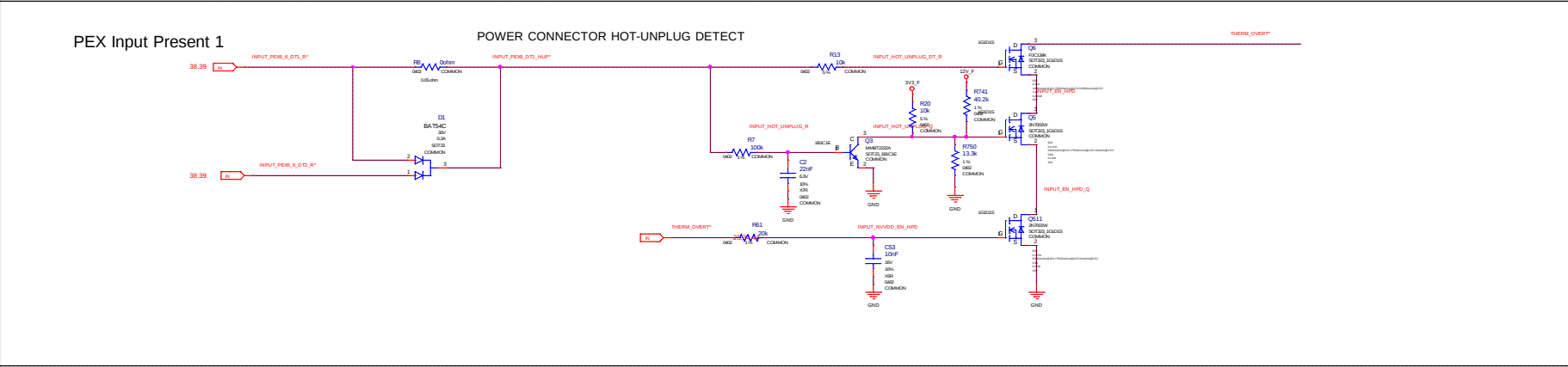


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Site	Document	Description	Rev
Custom	Input Power Balancing Switcher		2.0
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Size	Document	Description	Rev
Custom	BUCKBOOST		2.0
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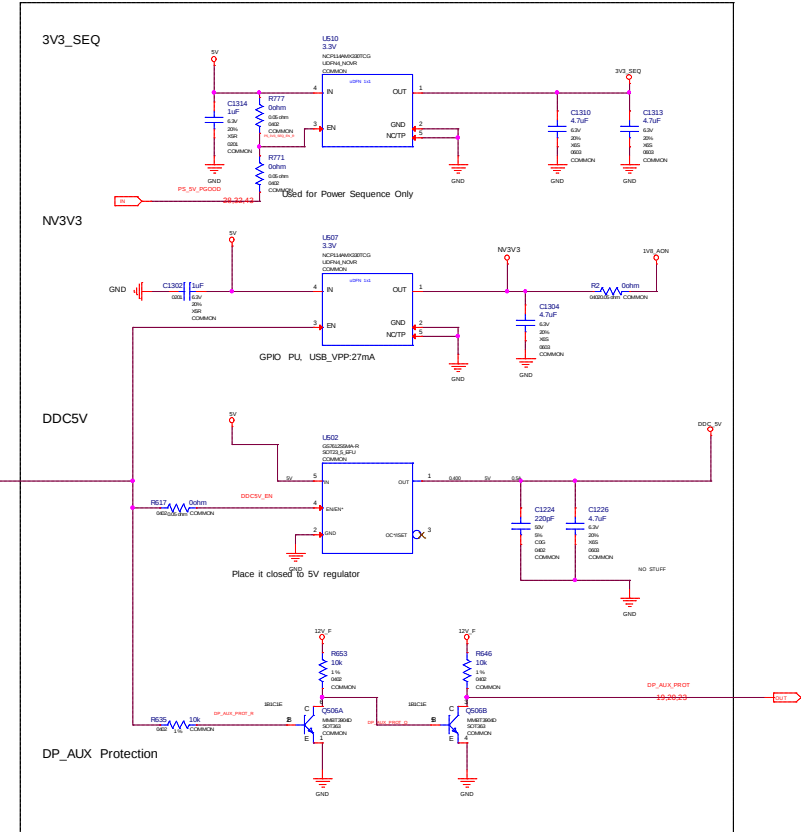
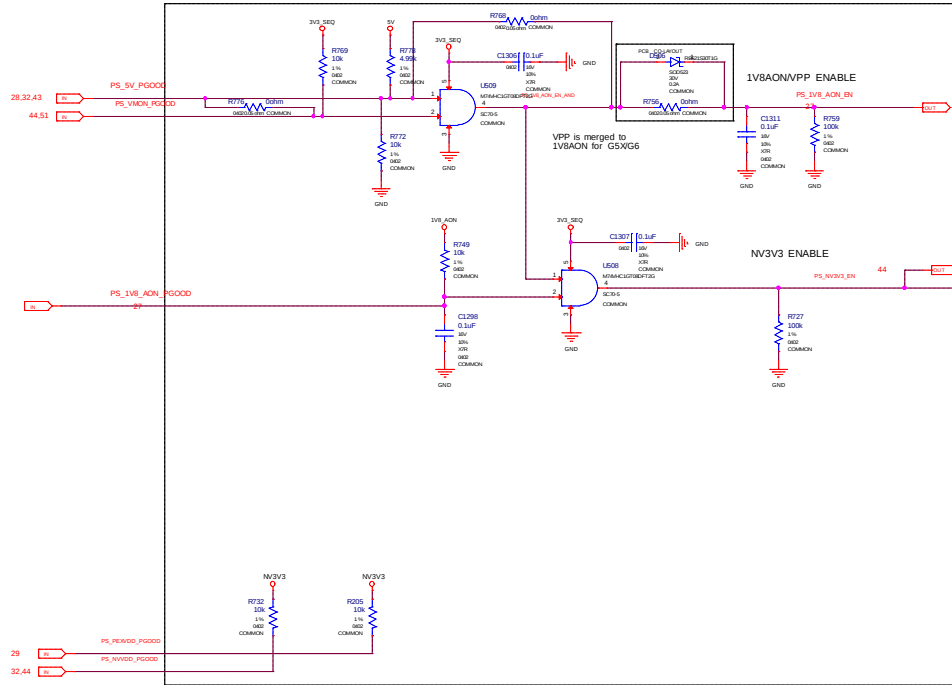
Site	Document	Description	Rev
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Date: Tuesday, December 04, 2018		Sheet	41 of 52

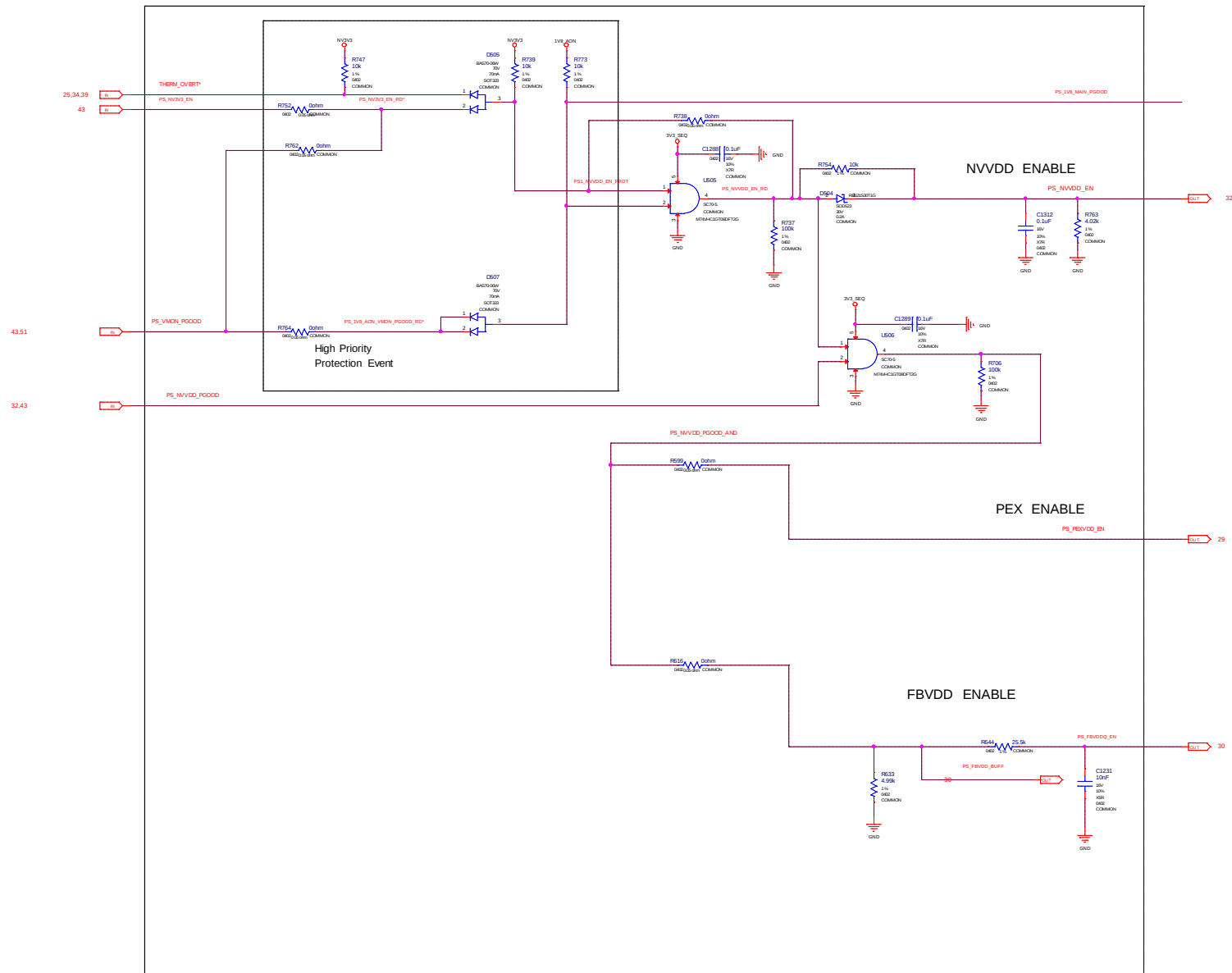


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Size	Document	Description	Rev
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Date: Tuesday, December 24, 2018			Sheet 42 of 52







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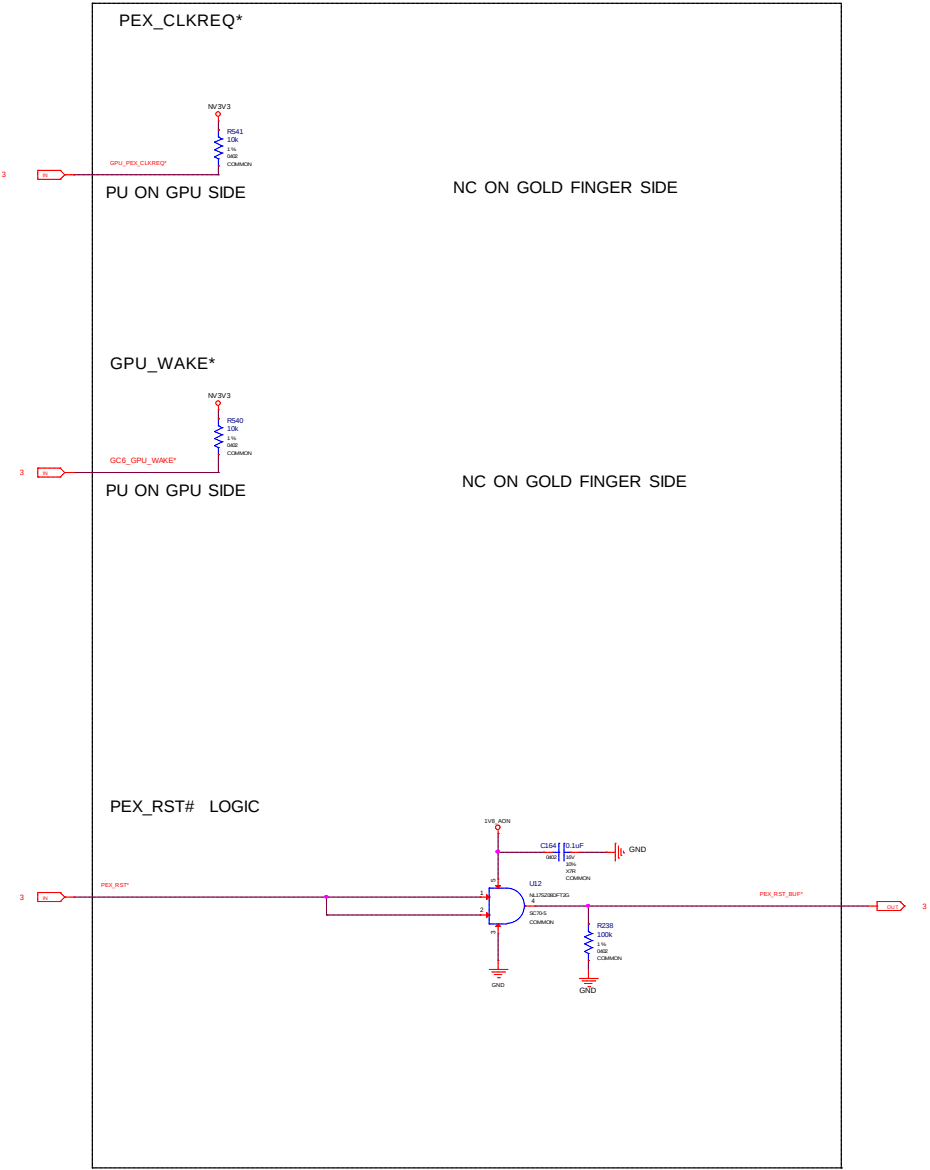
Site	Document	Description	Rev
Custom	SEQUENCE:Voltage Monitor		2.0
Date: Tuesday, December 24, 2018			Sheet 45 of 52



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Size	Document	Description	Rev
Custom	SEQUENCE:Discharge		2.0
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Doc	Document Description	Rev
Custom	SEQUENCE:MISC	2.0
Date:	Tuesday, December 24, 2016	Sheet 47 of 53

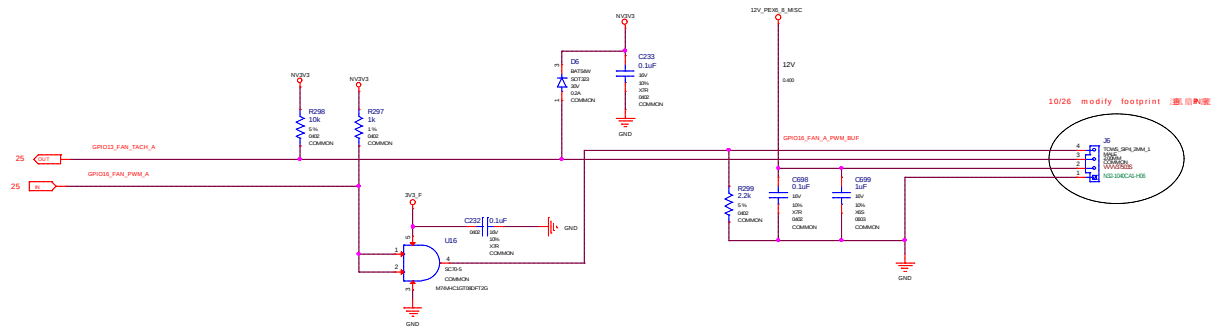


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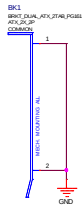
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Site	Document	Description	Rev
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Date: Tuesday, December 24, 2018			Sheet 48 of 52

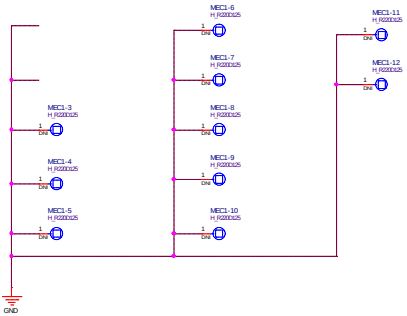




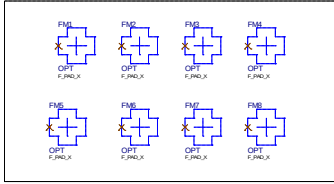
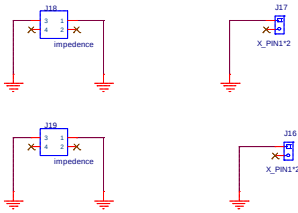
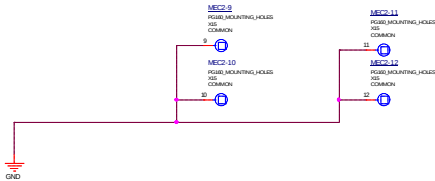
Bracket:



MOUNTING HOLES FOR HS:



BACK STIFFENER:





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Custom	PTC		2.0
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