

N18P GDDR5 X32 128BITS PCIE AND MODULAR DISPLAY

TABLE OF CONTENTS

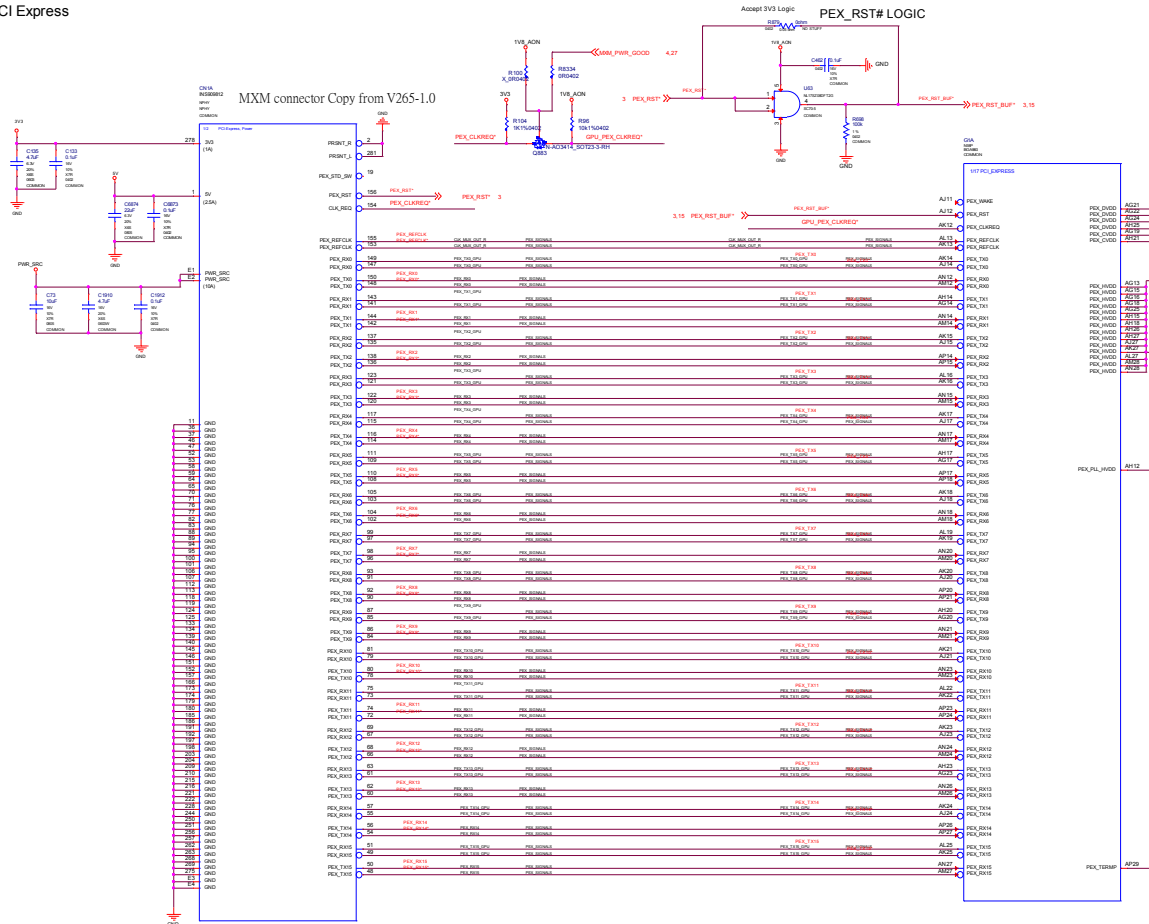
Page	Description
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1	TABLE OF CONTENTS
2	BLOCK DIAGRAM
3	PCI EXPRESS
4	MXM Connector
5	MEMORY: GPU PARTITION A/B
6	MEMORY: FBA[31:0]
7	MEMORY: FBA[63:32]
8	MEMORY_ FBB[31_0]
9	MEMORY_ FBB[63_32]
10	GPU PWR. GND and NCs
11	GPU DECOUPLING
12	GPU IFPAB DPIIM
13	GPU IFPCD DPIIM
14	GPU IFPE MICTOR
15	GPU_ ROM, STRAPS
16	GPU_ ROM, STRAPS
17	GPU_ XTAL, PLL
18	PS_ 1V8_AON
19	PS_PEXVDD
20	PS_ NV3V3
21	PS_ FBVDD CONTROLLER
22	PS_ NVVDD CONTROLLER
23	PS_ NVVDD 2 PHASE
24	GPIO Functional Description
25	INPUT PREFILTER

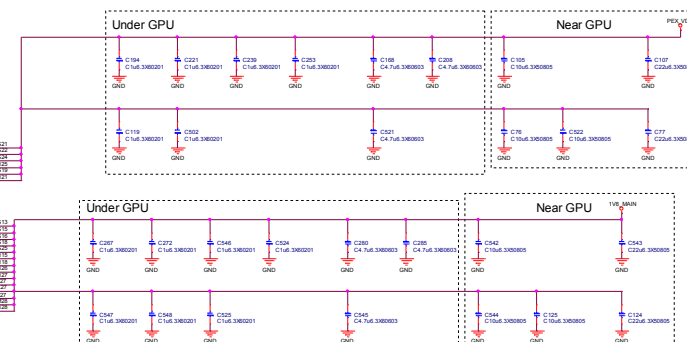
Page	Description
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26	DP_AUX Protection
27	Sequence
28	SEQUENCE_ DISCHARGE
29	MECH

			MICRO-STAR INT'L CO.,LTD MS-V378	
Size	Document Description			Rev
Custom	BLOCK DIAGRAM			1.1
Date: Thursday, October 24, 2019		Sheet	2	of 28

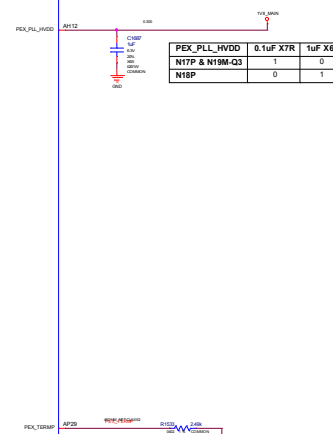


PEX_DVDD	1uF X6S	4.7uF X6S	10uF X6S	22uF X5
N18P	6	3	3	2



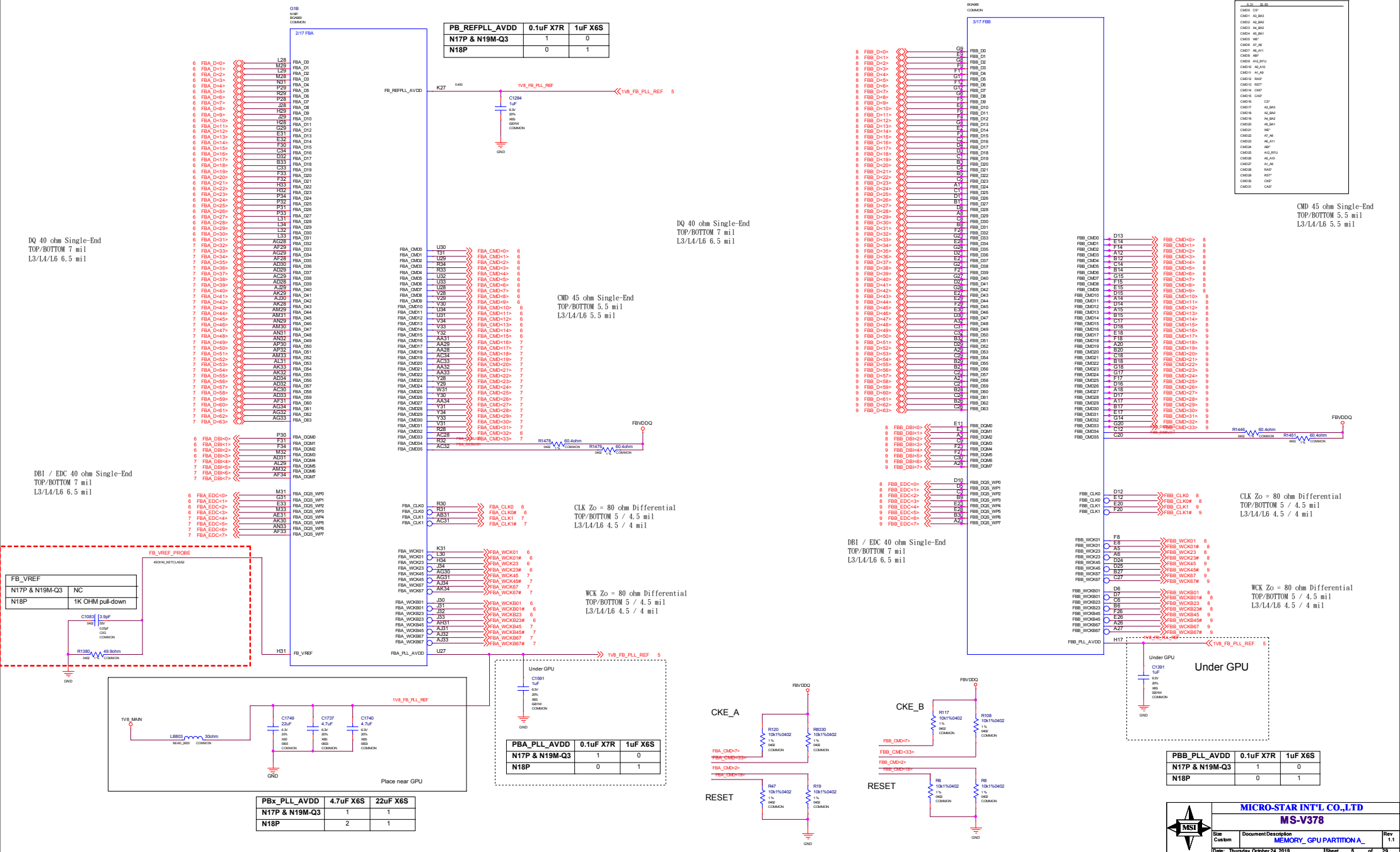
PEX_HVDD	1uF X6S	4.7uF X6S	10uF X6S	22uF X6S
N18P	7	3	3	2

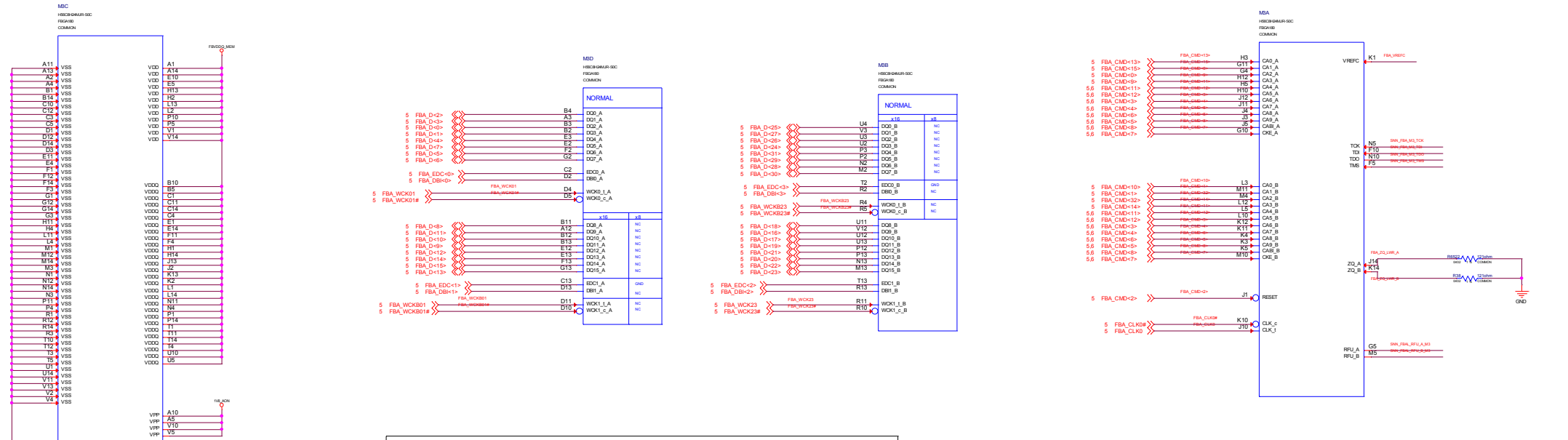
PEX_PLL_HVDD	0.1uF X7R	1uF X6
N17P & N19M-Q3	1	0
N18P	0	1

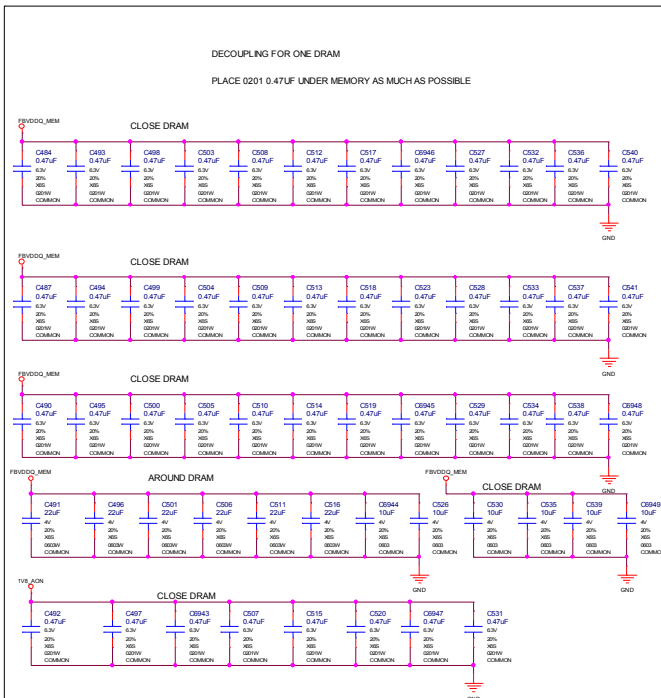
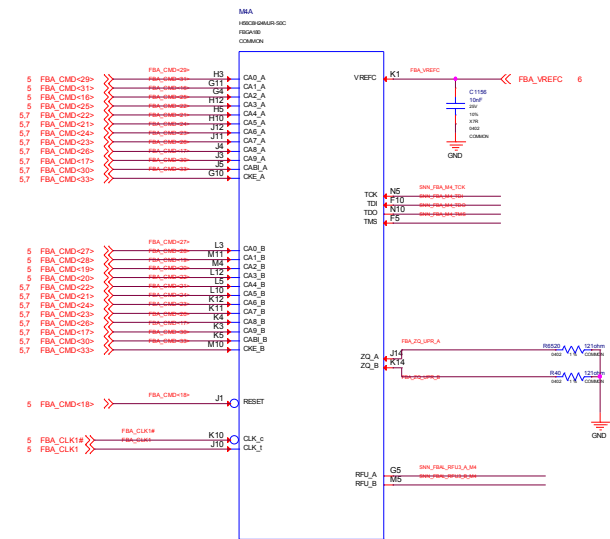
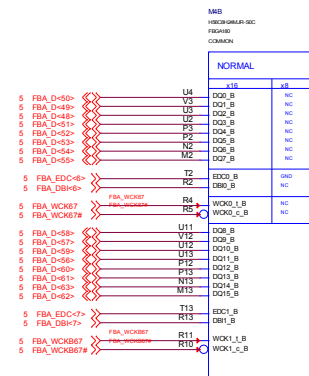
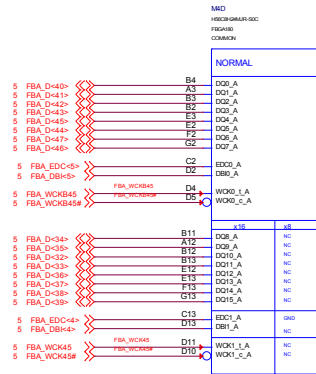
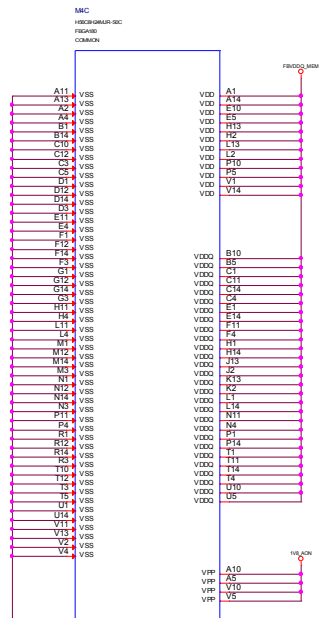


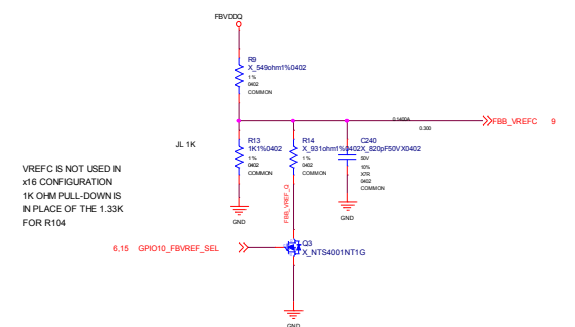
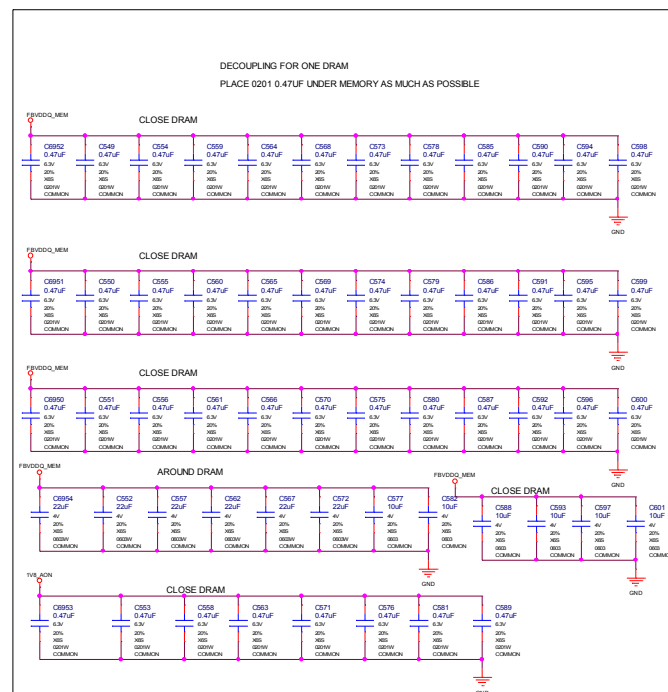


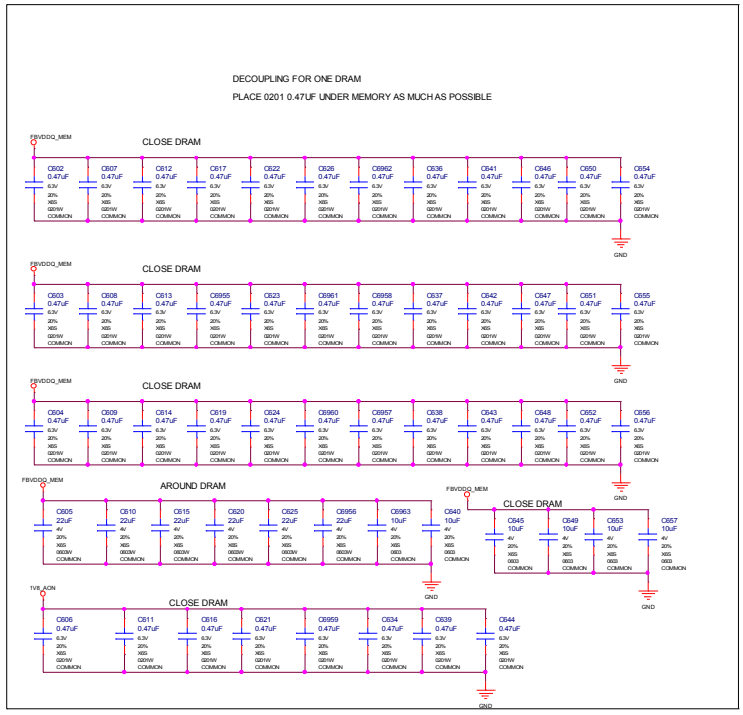
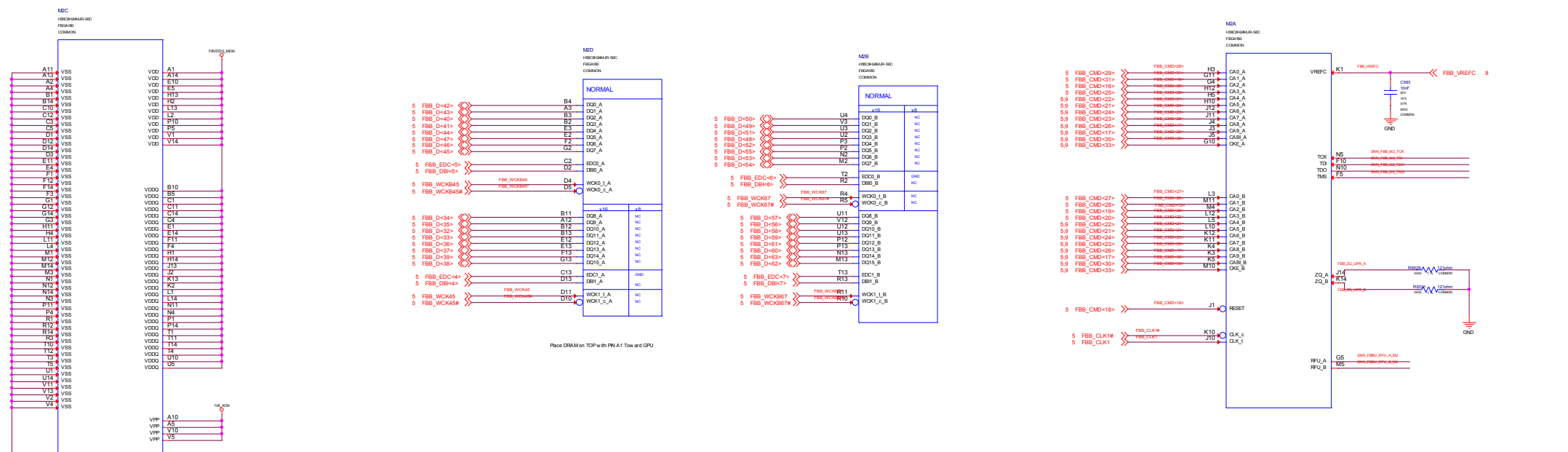
MEMORY: GPU PARTITION A/B



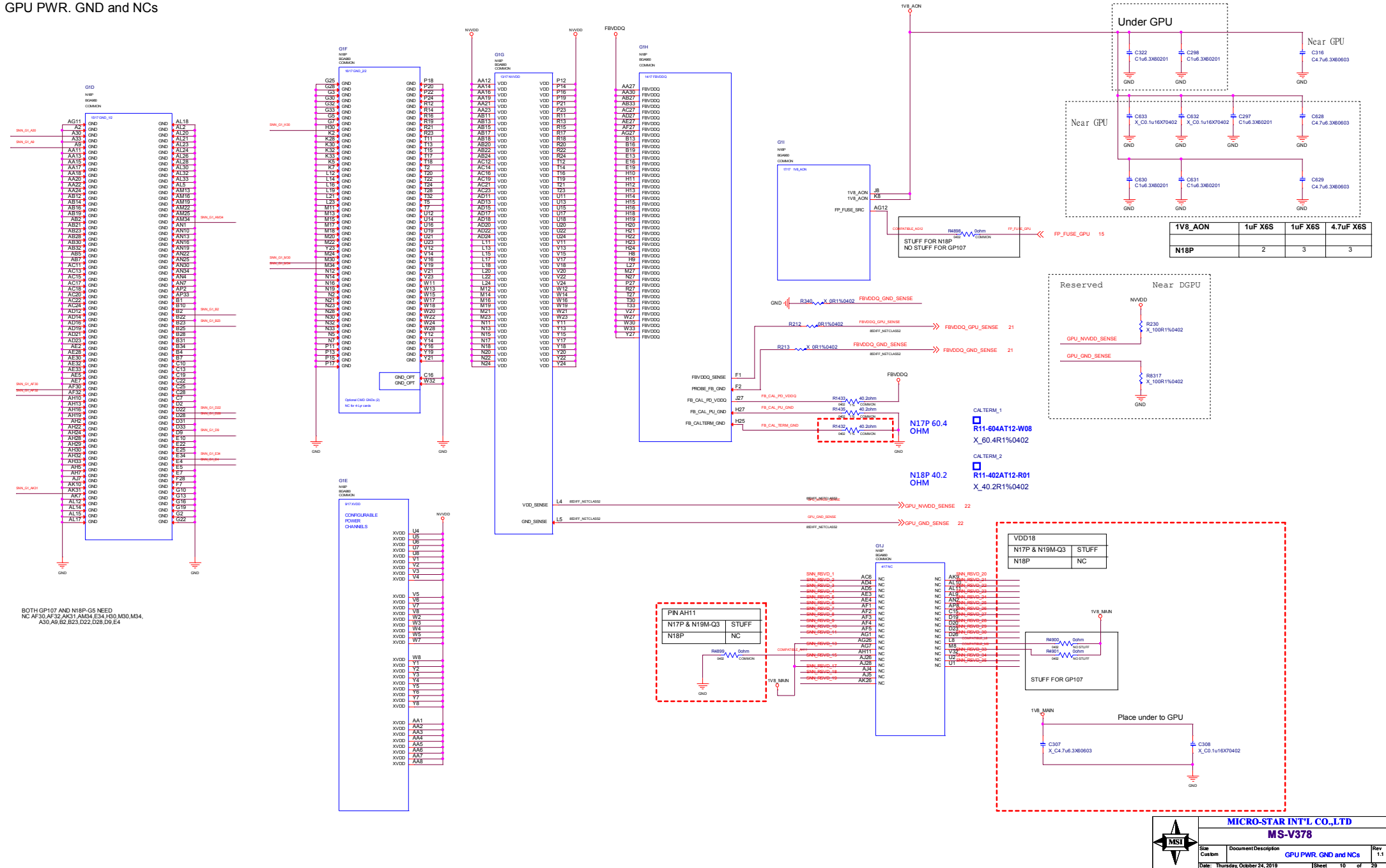








GPU PWR. GND and NCs

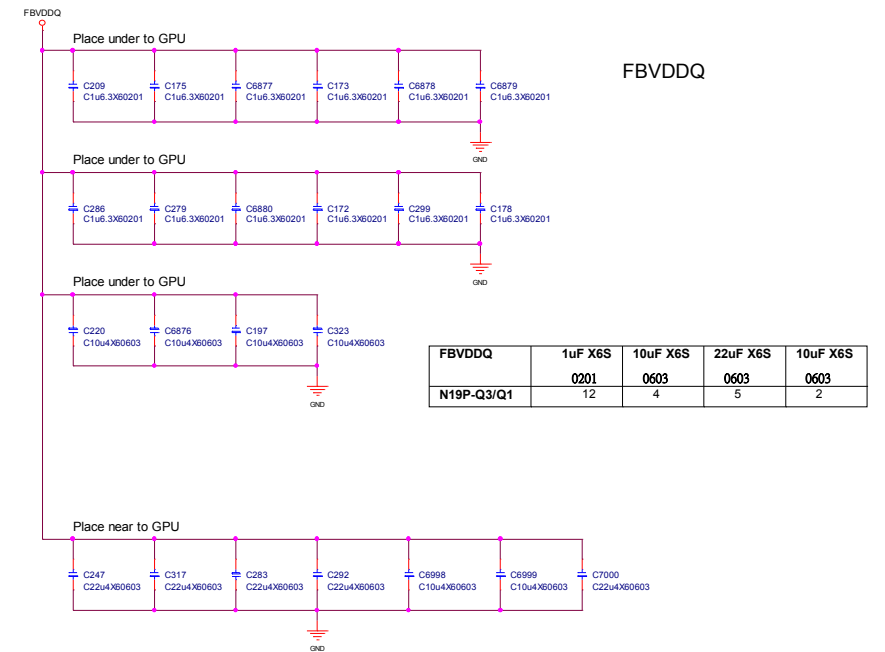


GPU DECOUPLING



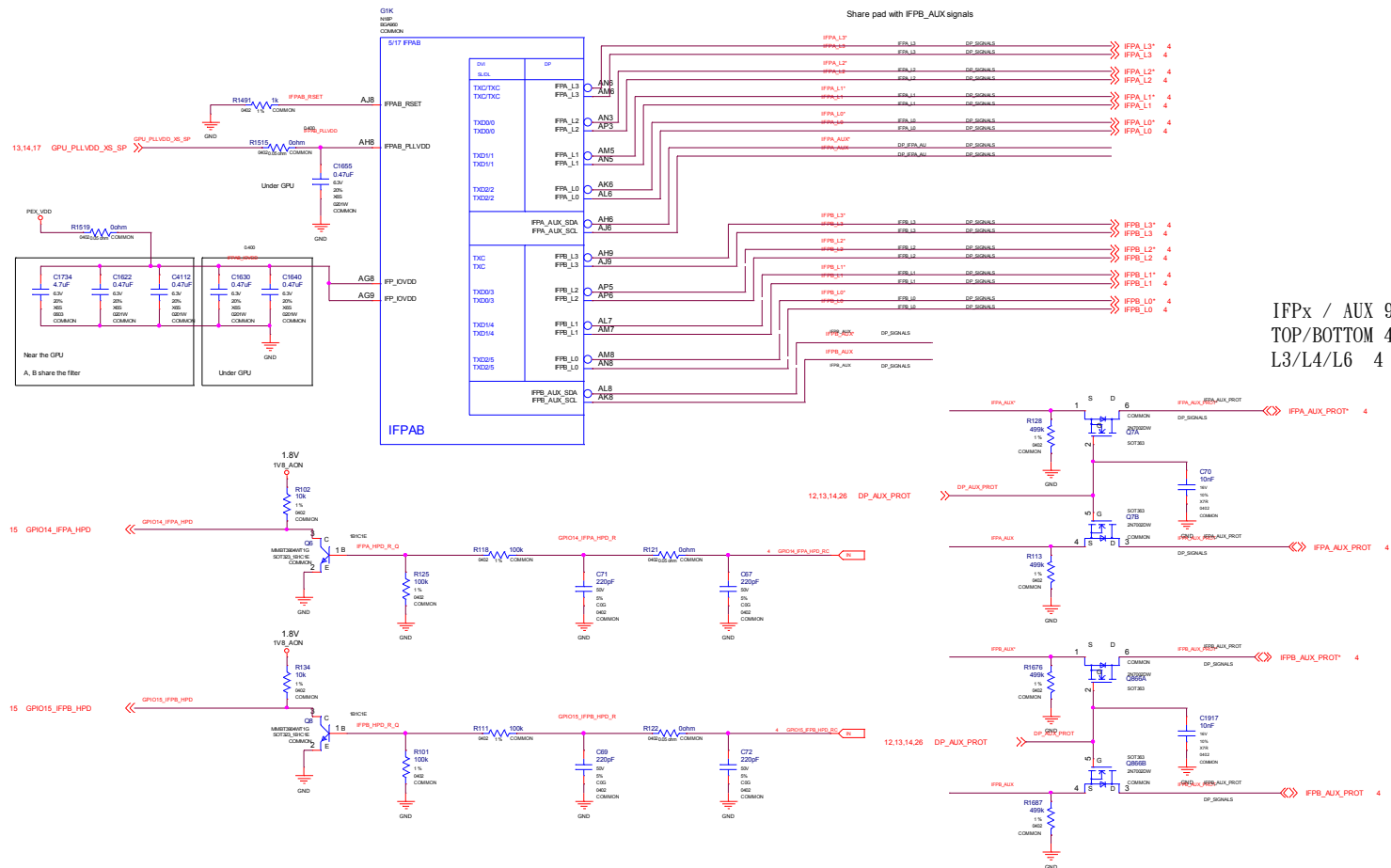
NVVDD

NVVDD	1uF X6S	10uF X6S	22uF X6S
	0201	0603	0805
N19P-Q3/Q1	13	34	15

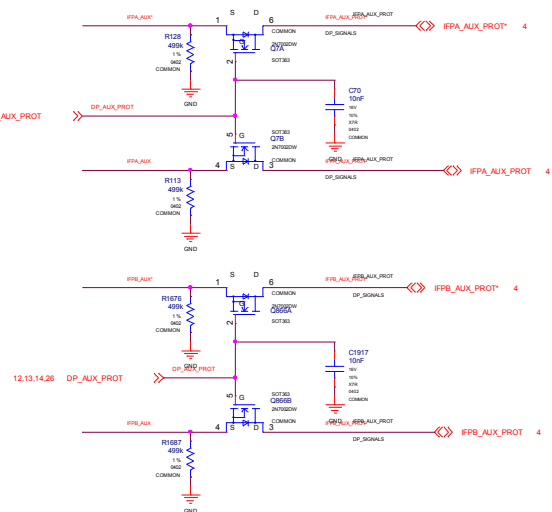


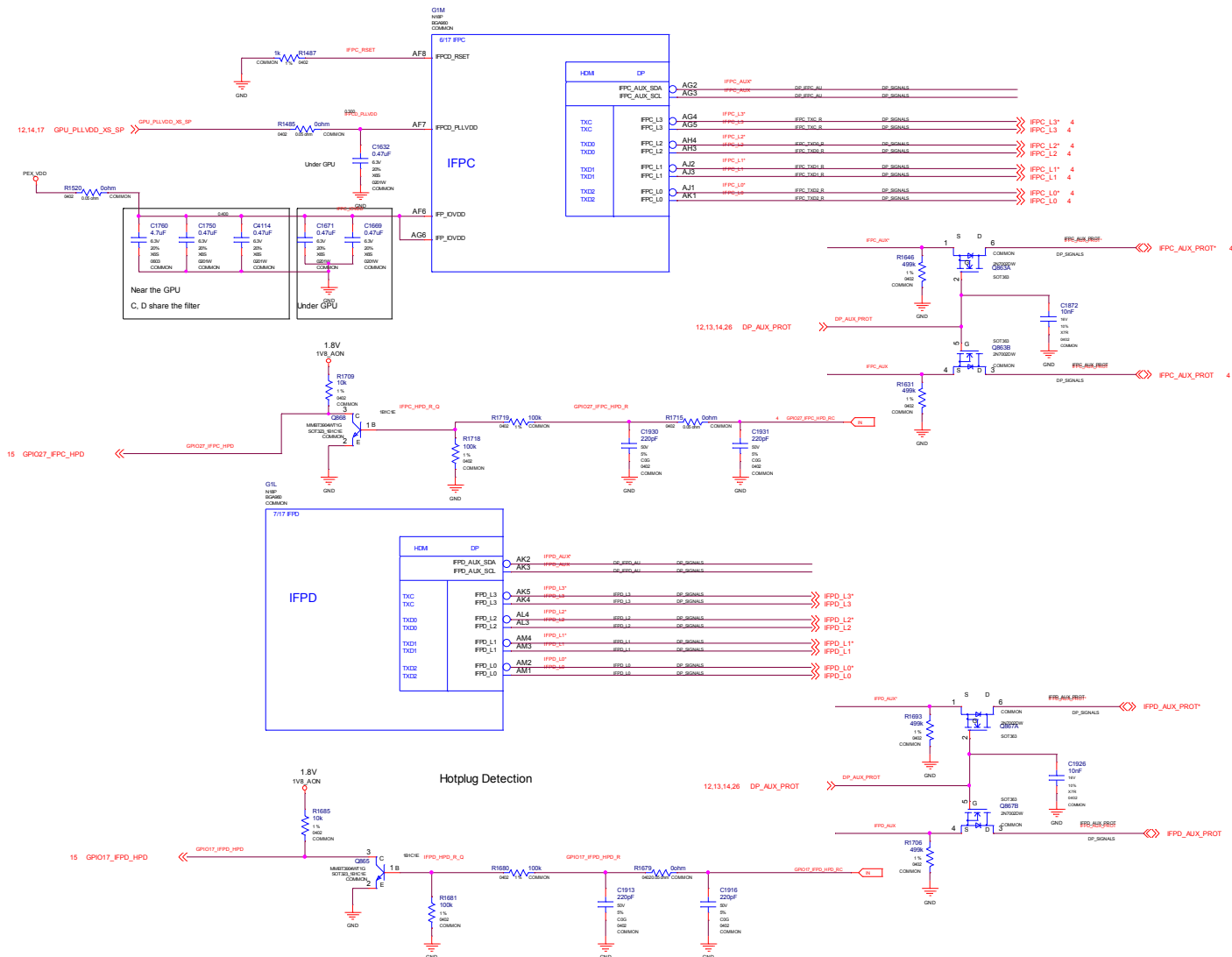
FBVDDQ

FBVDDQ	1uF X6S	10uF X6S	22uF X6S	10uF X6S
	0201	0603	0603	0603
N19P-Q3/Q1	12	4	5	2

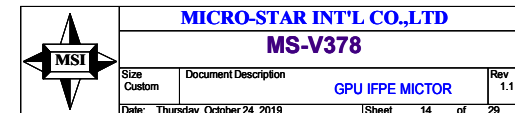
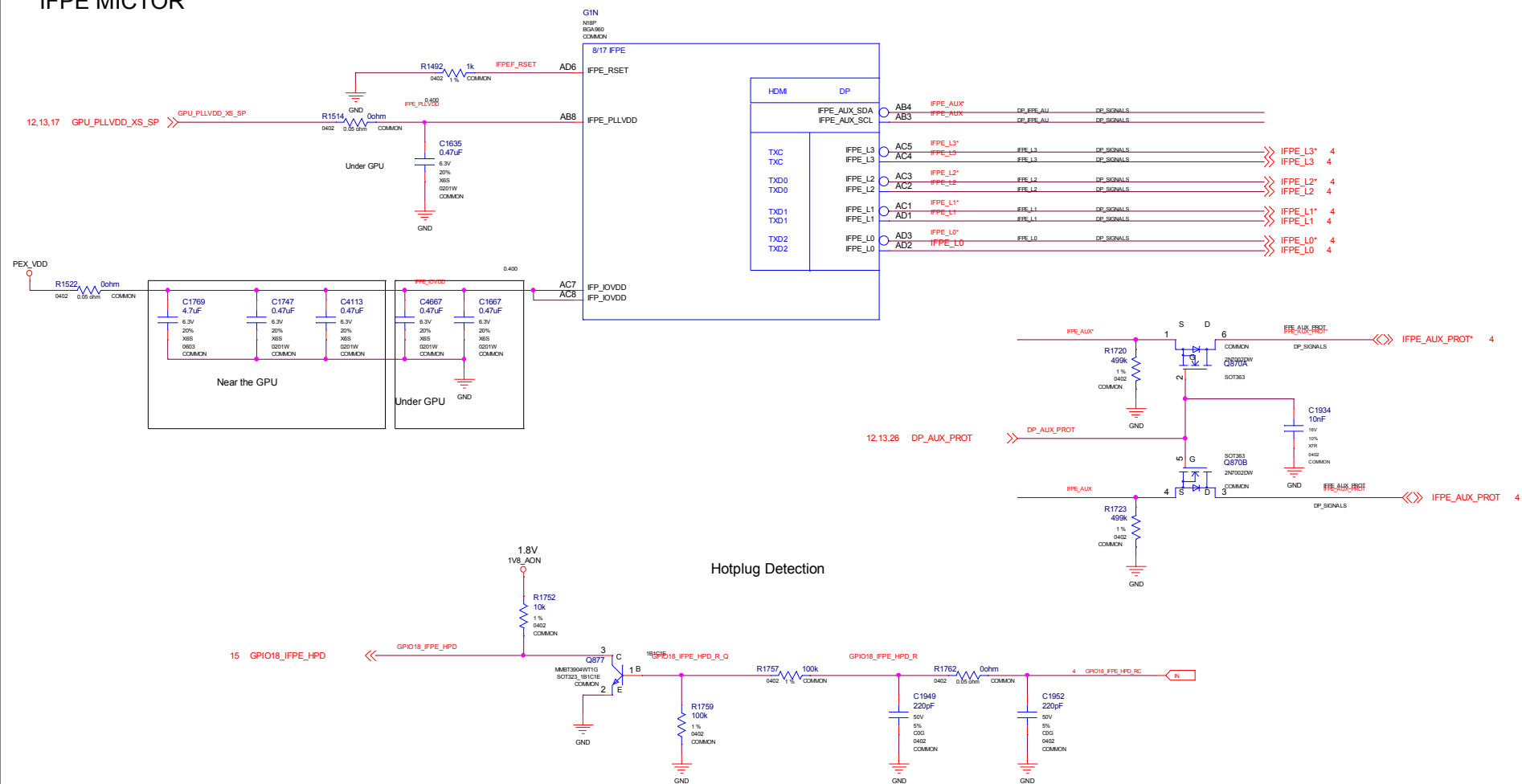


IFPx / AUX 90 ohm Differential
TOP/BOTTOM 4 / 5 mil
L3/L4/L6 4 / 6 mil

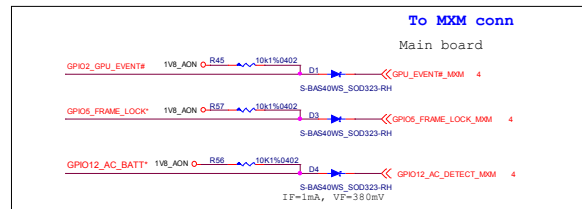
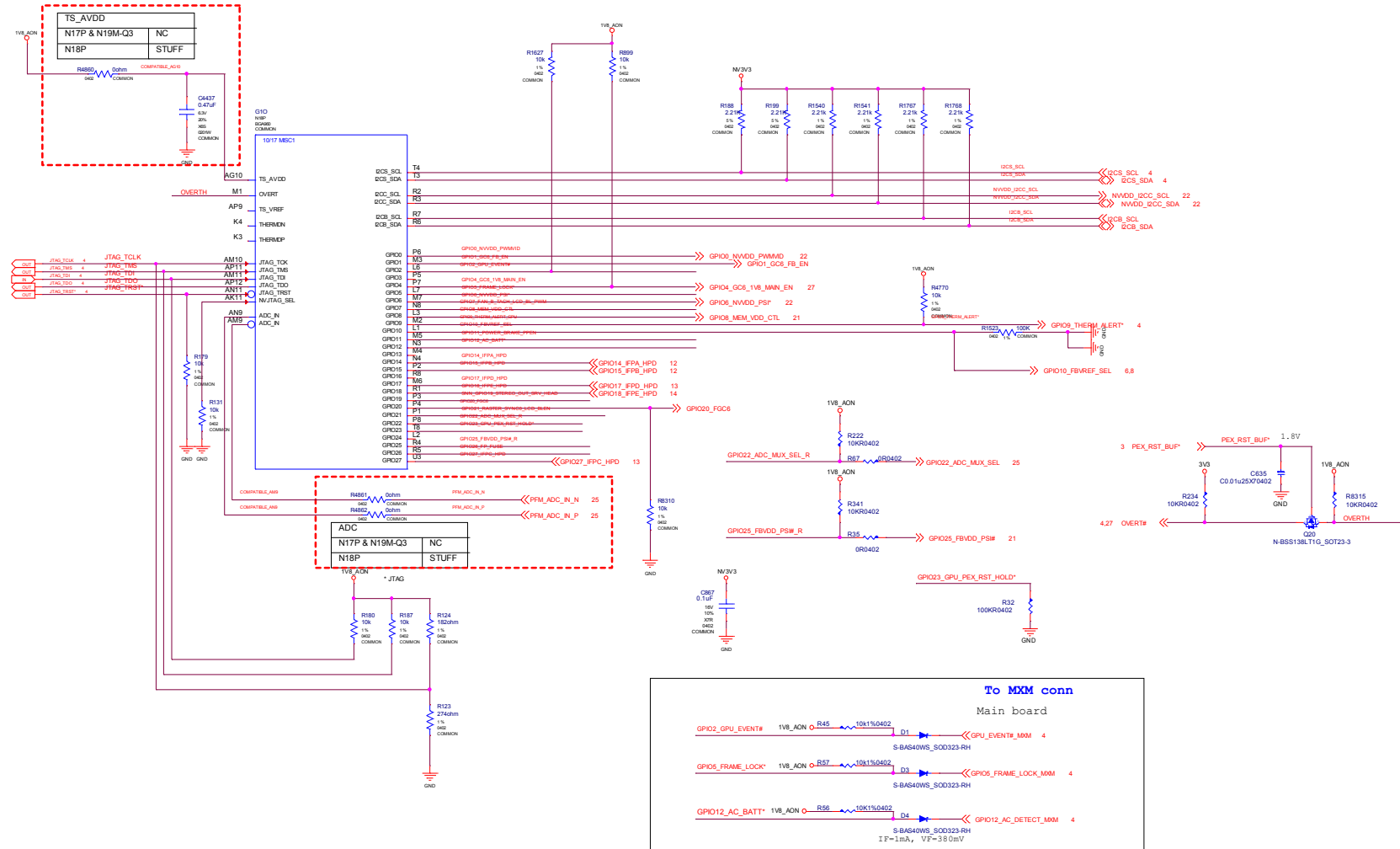
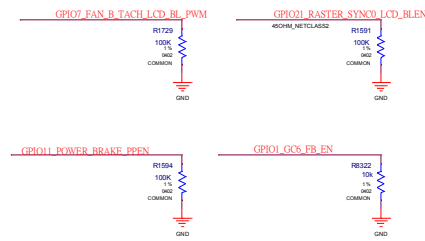
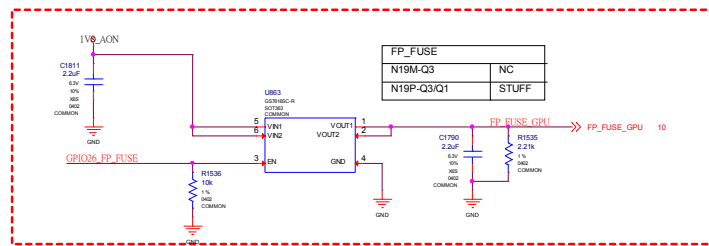




IFPE MICTOR



MISC: Fan, JTAG, GPIO, STEREO



MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0].FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

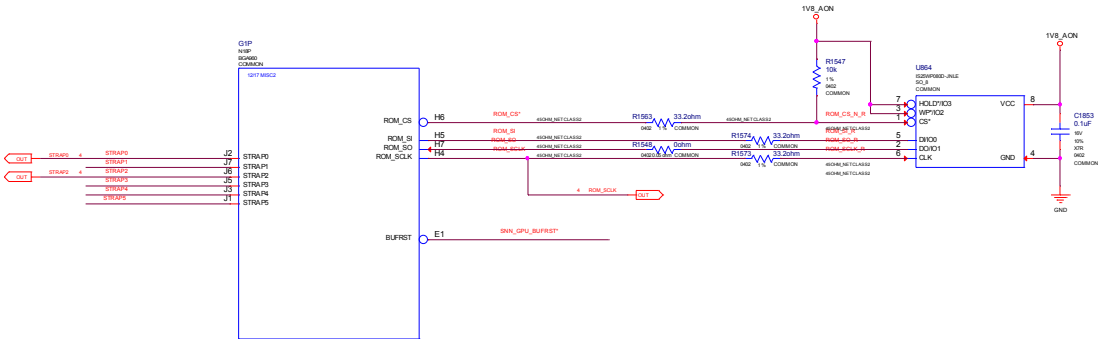
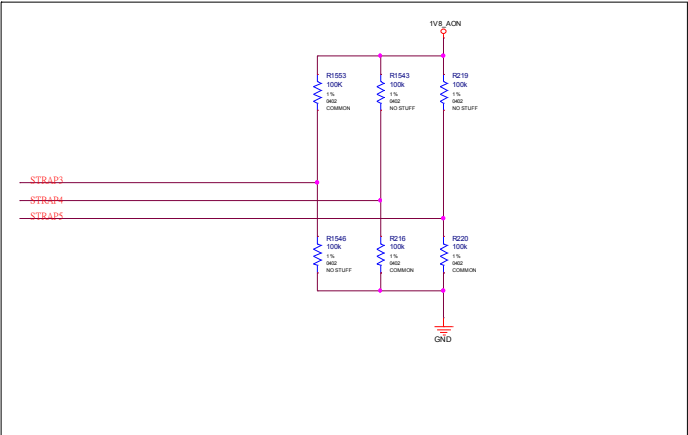
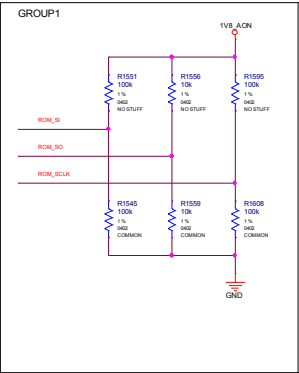
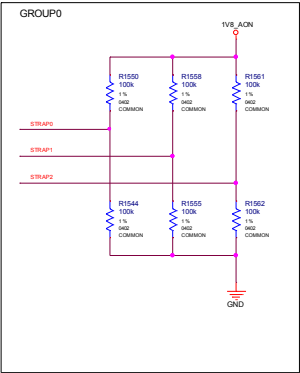
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

DEFAULT

- 1:SMB_ALT_ADDR ENABLE
- 0:SMB_ALT_ADDR DISABLE
- 1:DEVID_SEL REBRAND
- 0:DEVID_SEL ORIGNAL
- 1:PCIE_CFG LOW POWER
- 0:PCIE_CFG HIGH POWER
- 1:VGA_DEVICE ENABLE
- 0:VGA_DEVICE DISABLE

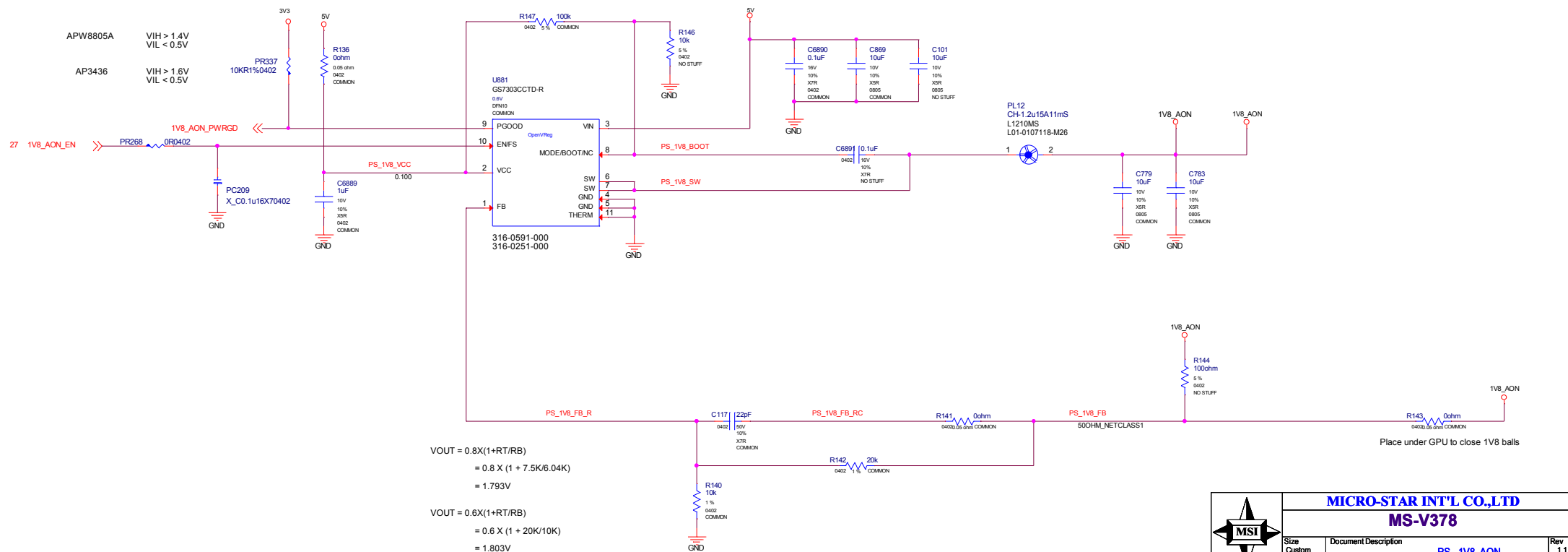
Default



PS: 1V8_AON

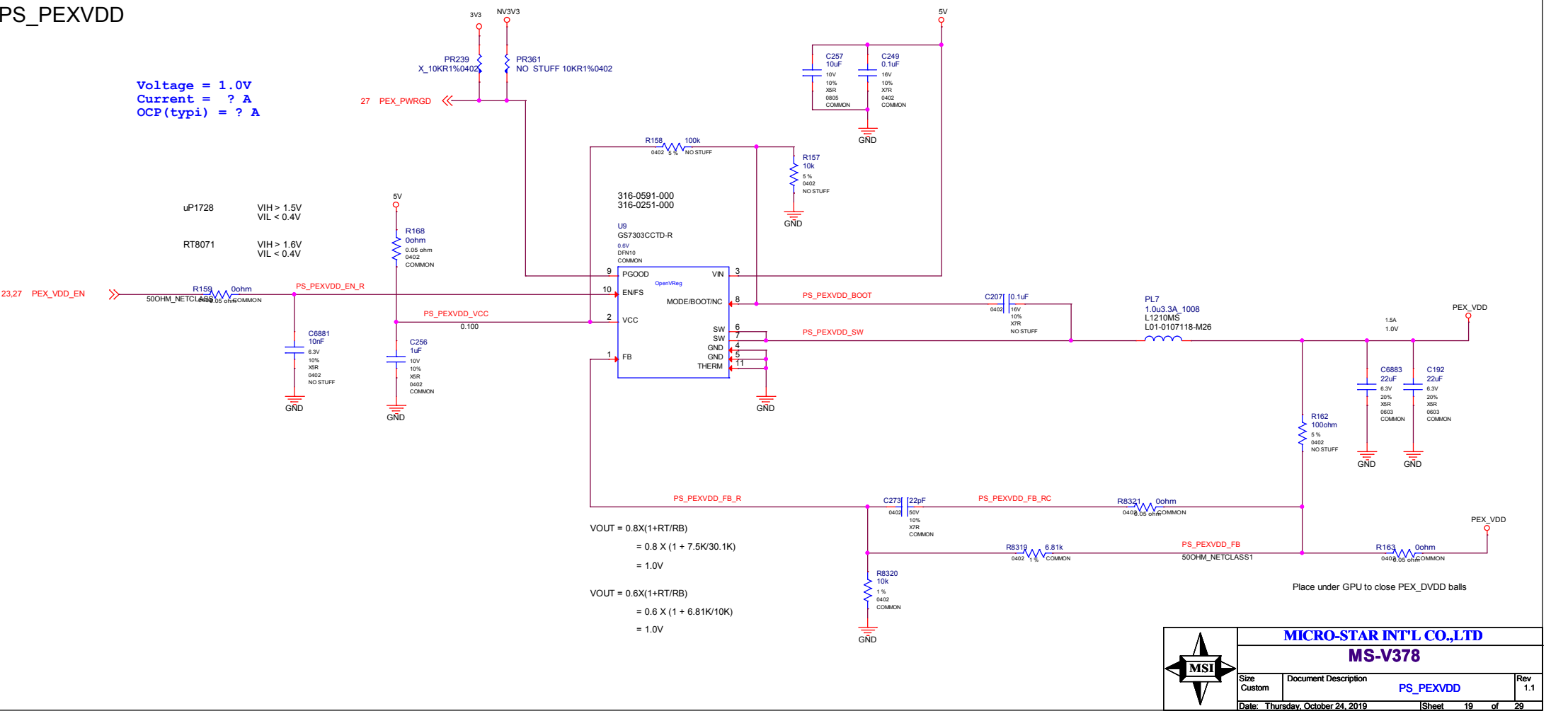
Voltage = 1.8V
Current = ? A
OCP(typi) = ? A

1V8_AON

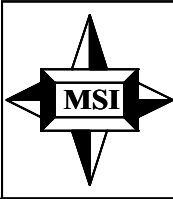


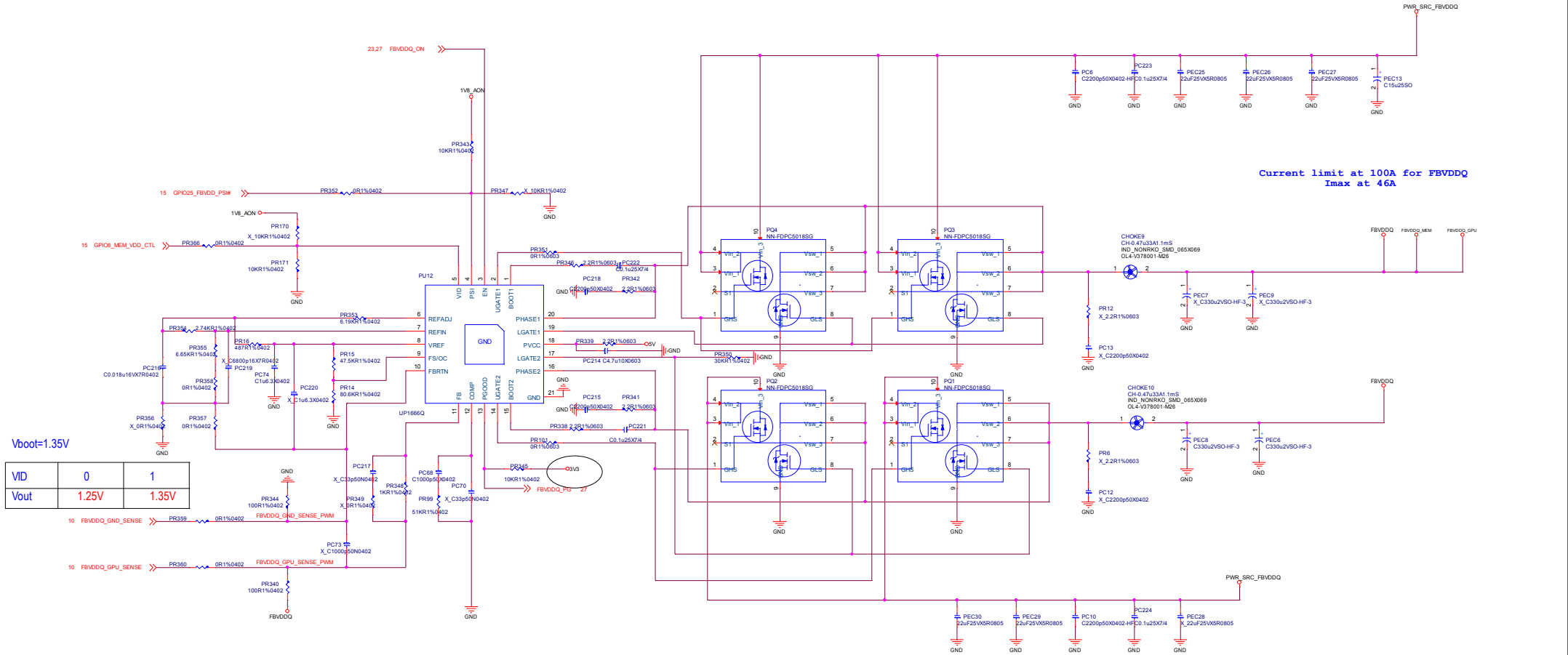
	MICRO-STAR INT'L CO.,LTD				
	MS-V378				
	Size Custom	Document Description PS_1V8_AON			Rev 1.1
	Date: Thursday, October 24, 2019			Sheet 18 of 29	

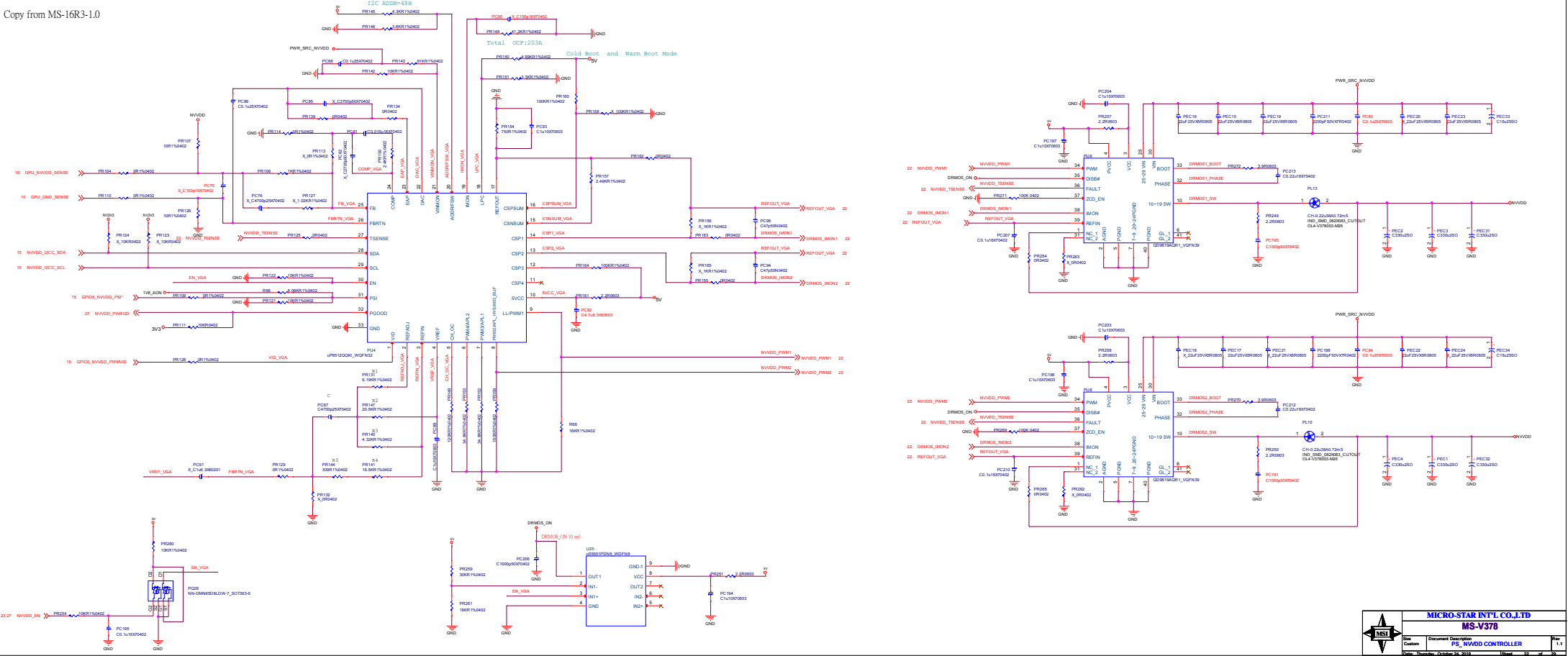
PS_PEXVDD



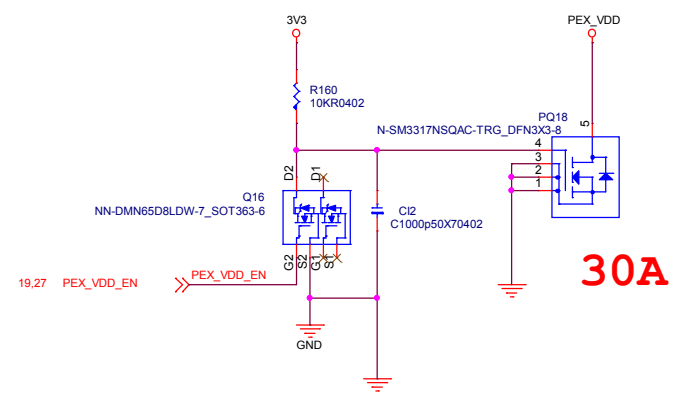
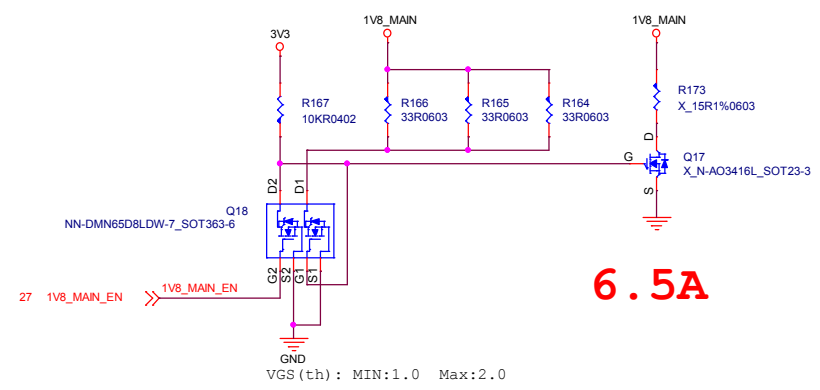
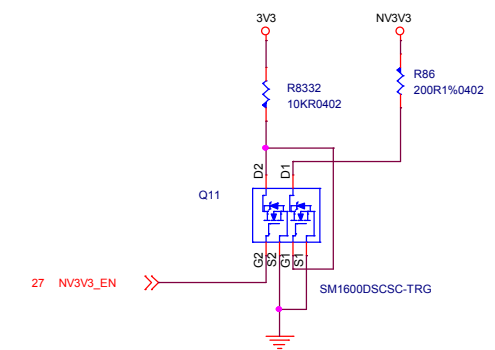
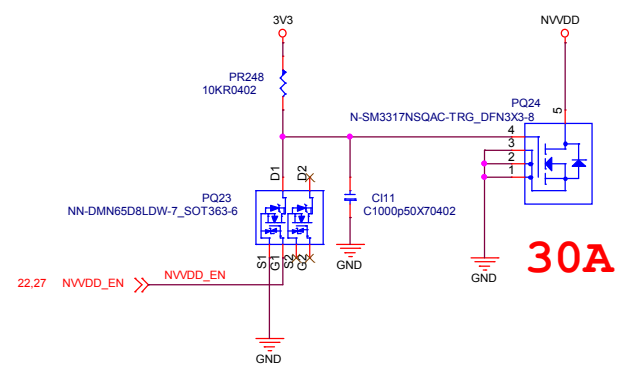
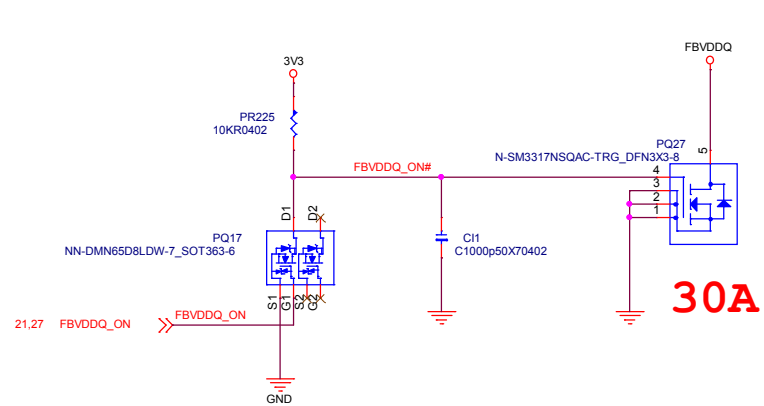
BLANK

	MICRO-STAR INT'L CO.,LTD		
	MS-V378		
	Size A	Document Description PS_ NV3V3	Rev 1.1
	Date: Thursday, October 24, 2019	Sheet 20 of	29



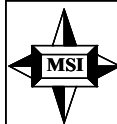


Discharge



	MICRO-STAR INT'L CO.,LTD		
	MS-V378		
	Size Custom	Document Description DISCHARGE	Rev 1.1
	Date: Thursday, October 24, 2019	Sheet 23 of 29	

Pin Name	N17P	N18P	N17P Functional Description	N17P Recommended Default Pull-up or Pull-down	N18P Recommended Default Pull-up or Pull-down
GPIO0	NVVD_PWM	NVVD_PWM_VID	PWM Output to control NVVD	0 to 1V8 PWM output	
GPIO1	GC6_FB_EN	GC6_FB_EN	FB Enable for GC6 2.1	OD, 10K pull-down	OD, 10K pull-down
GPIO2	GPU_EVENT#	GPU_EVENT#	GPU wake signal for GC6 2.1	10K pull-up to 1V8 _AON	10K pull-up to 1V8 _AON
GPIO3	NVVD_PWM	UNUSED	PWM output to control the NVVD power supply	0 to 1V8 output	
GPIO4	1V8_MAIN_EN	1V8_MAIN_EN	GPU POWER Sequencing for GC6 2.1	OD, 10K pull-up to 1V8 _AON	OD, 10K pull-up to 1V8 _AON
GPIO5	FRM_LCK#	FRM_LCK#	Active low Frame Lock	OD, 10K pull-up to 1V8 _AON	OD, 10K pull-up to 1V8 _AON
GPIO6	NVVD_PSI	NVVD_PSI	Phase shedding	10K pull-up to 1V8 _AON	10K pull-up to 1V8 _AON
GPIO7	LCD_BL_PWM	LCD_BL_PWM	Panel Backlight PWM Brightness Control	100K pull-down	100K pull-down
GPIO8	MEM_VDD_CTL	MEM_VDD_CTL	Memory Voltage Control	pull-up/pull-down to set the FBVDD/Q power-on voltage	pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	THERM_ALERT	Active Low Thermal Alert	OD, 10K pull-up to 1V8_AON	OD, 10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	MEM_VREF_CTL	Memory VREF Control	100K pull-down	100K pull-down
GPIO11	LCD_VCC	LCD_VCC	Panel Power Enable	100K pull-down	100K pull-down
GPIO12	PWR_LEVEL	PWR_LEVEL	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON	10K pull-up to 1V8_AON
GPIO13	LCD_BLEN	UNUSED	Panel Backlight Enable	100K pull-down	
GPIO14	HPD_A	HPD_A	Hot Plug Detect for IFPA		10K pull-up to 1V8_AON
GPIO15	HPD_B	HPD_B	Hot Plug Detect for IFPB		10K pull-up to 1V8_AON
GPIO16	SYS_PEX_RST_MON#	UNUSED	System side PCIe reset monitor	10K pull-up to 1V8 _AON	
GPIO17	HPD_D	HPD_D	Hot Plug Detect for IFPD		10K pull-up to 1V8_AON
GPIO18	HPD_E	HPD_E	Hot Plug Detect for IFPE		10K pull-up to 1V8_AON
GPIO19	3DVision	UNUSED	3D Vision L/R signal	100K pull-down	
GPIO20	GC5_MODE	NB_GC6			10K pull-down
GPIO21	UNUSED	LCD_BLEN			100K pull-down
GPIO22	UNUSED	ADC_MUX_SEL			2.2K pull-up See Circuit
GPIO23	GPU_PEX_RST_HOLD#	RESERVED	GPU PCIe self-reset control	OD, 10K pull-up to a gated 3V3	100K pull-down
GPIO24	HPD_F	UNUSED	Hot Plug Detect for IFPF		
GPIO25	UNUSED	FBVDD_PSI#			
GPIO26	UNUSED	FP_FUSE			10K pull-down
GPIO27	HPD_C	HPD_C	Hot Plug Detect for IFPC		10K pull-up to 1V8_AON

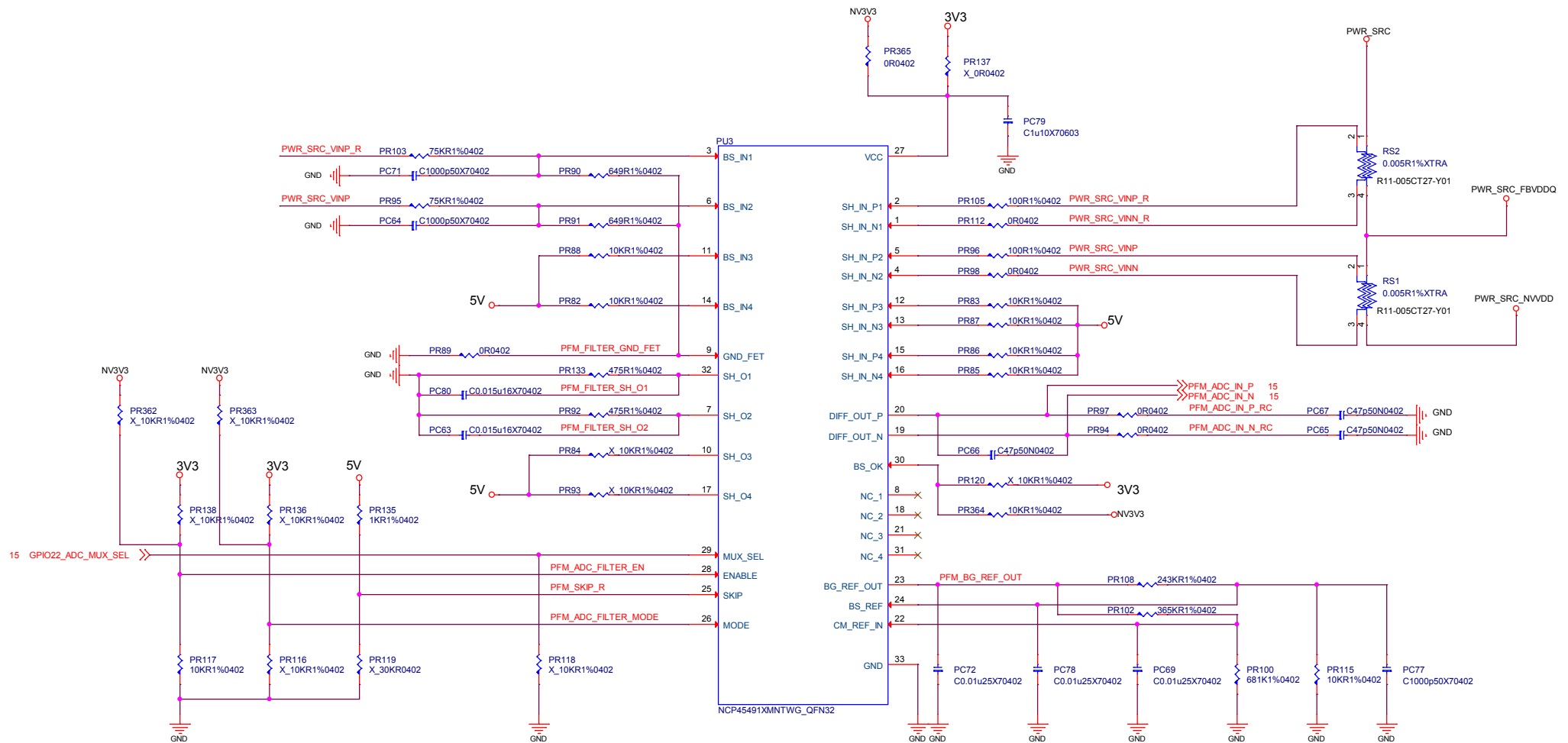


MICRO-STAR INT'L CO.,LTD
MS-V378

Size B	Document Description GPIO Functional Description	Rev 1.1
Date: Thursday, October 24, 2019		Sheet 24 of 29

INPUT PREFILTER

On Semi	PR90, PR91	PR92, PR133	PR108	PR95, PR103	PC64, PC71
CONFIG	R954, R924	R977, R923	R950	R953, R952	C841, C836
N18P-G0	649R	475R	243K	75K	1.0nF

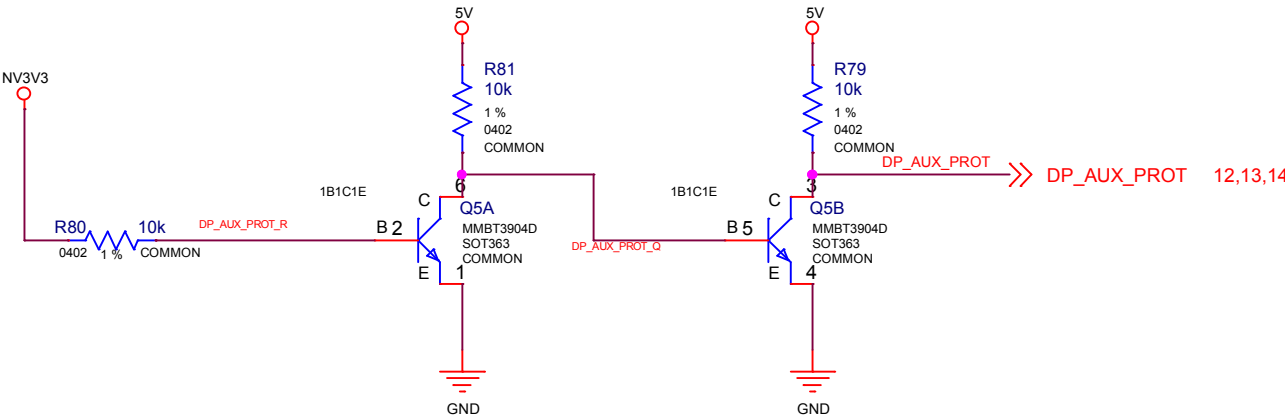


MICRO-STAR INT'L CO.,LTD
MS-V378

Size Custom	Document Description INPUT PREFILTER	Rev 1.1
Date: Thursday, October 24, 2019		Sheet 25 of 29

SEQUENCE:5V,1V8,NV3V3 ENABLE

DP_AUX Protection

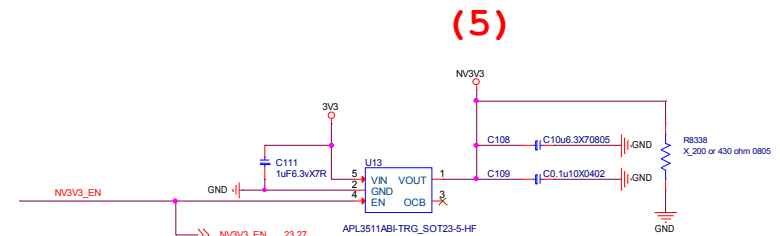
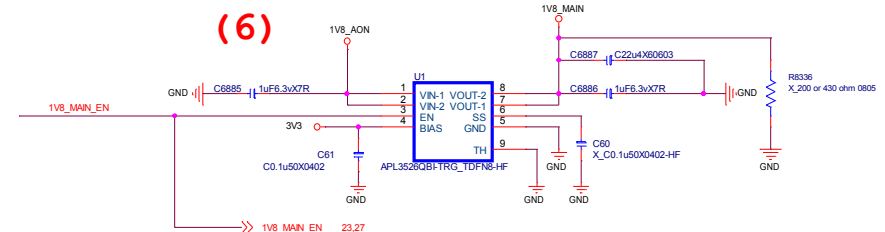
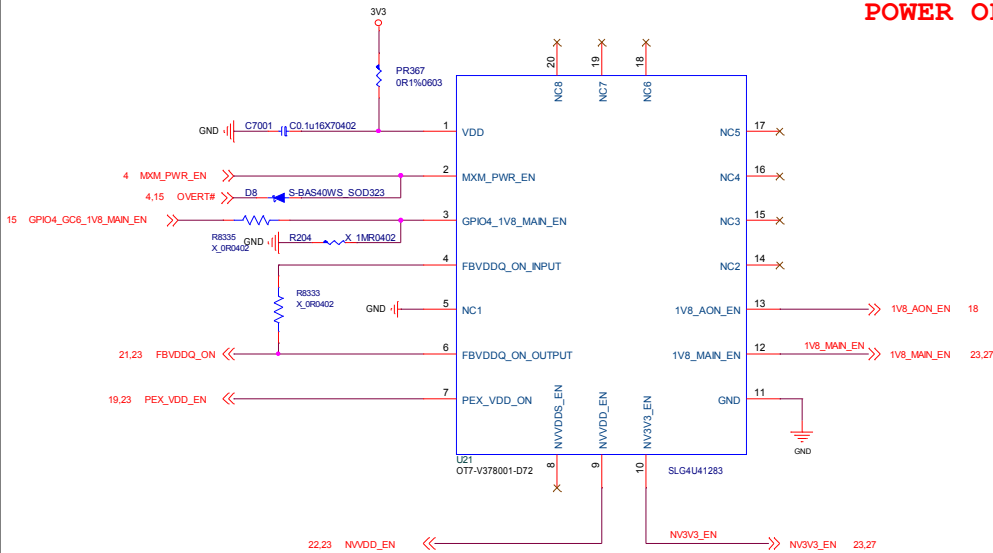


	MICRO-STAR INT'L CO.,LTD			
	MS-V378			
	Size A	Document Description DP_AUX Protection		Rev 1.1
	Date: Thursday, October 24, 2019		Sheet 26 of 29	

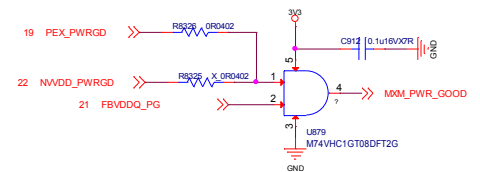
Power Sequence Control

POWER ON= 1V8_AON->1V8_MAIN->NV3V3->NVVDD->PEX_VDD->FBVDDQ->DGPU_PWRGD

POWER OFF= PEX_VDD/FBVDDQ->NVVDD->NV3V3->1V8_MAIN->1V8_AON



SOFTSTRAT=400us



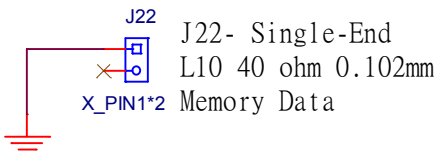
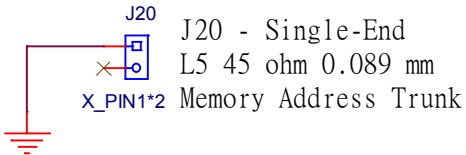
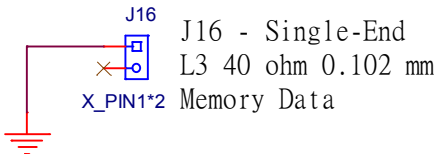
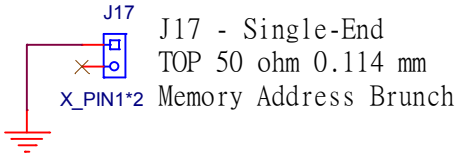
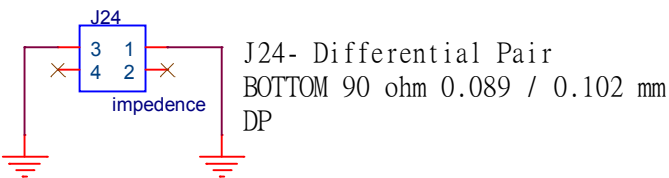
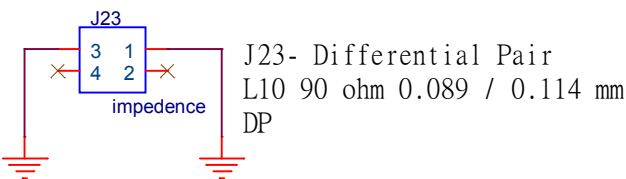
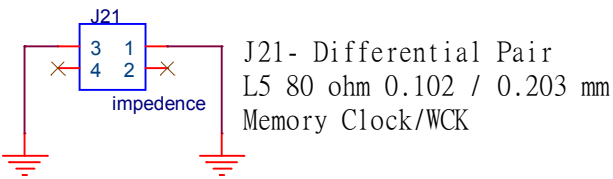
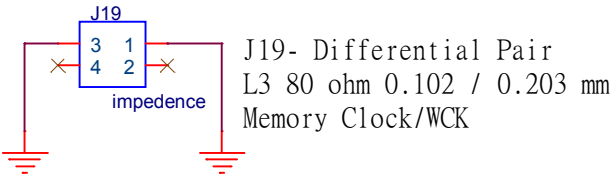
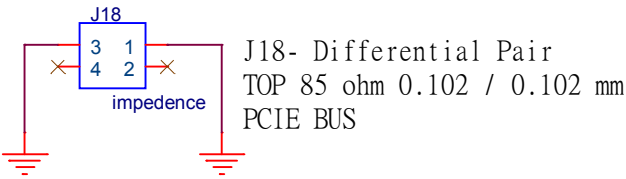
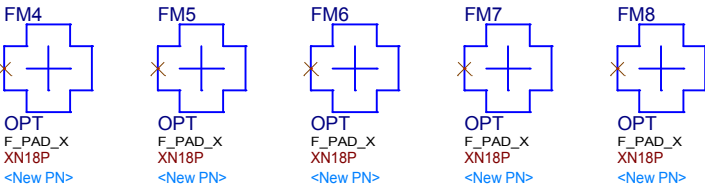
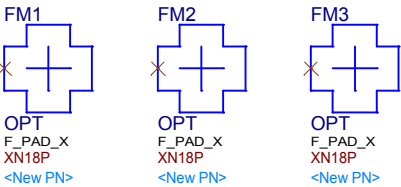
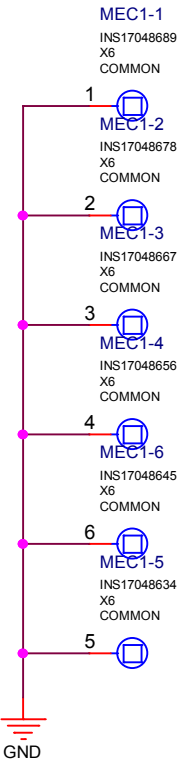
			
MICRO-STAR INT'L CO.,LTD MS-V378			
Size Custom	Document Description Sequence	Rev 1.1	
Date: Thursday, October 24, 2019	Sheet 27	of 29	

SEQUENCE:DISCHARGE

			MICRO-STAR INT'L CO.,LTD	
			MS-V378	
Size	Document Description			Rev
B	SEQUENCE_ DISCHARGE			1.1
Date: Thursday, October 24, 2019			Sheet	28 of 29

MECH

Mounting Holes



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Date: Thursday, October 24, 2019	Sheet 29 of 29	