

PG165-A00

TU116 6GB GDDR5, 192b, X32

DVI-D + DP + HDMI

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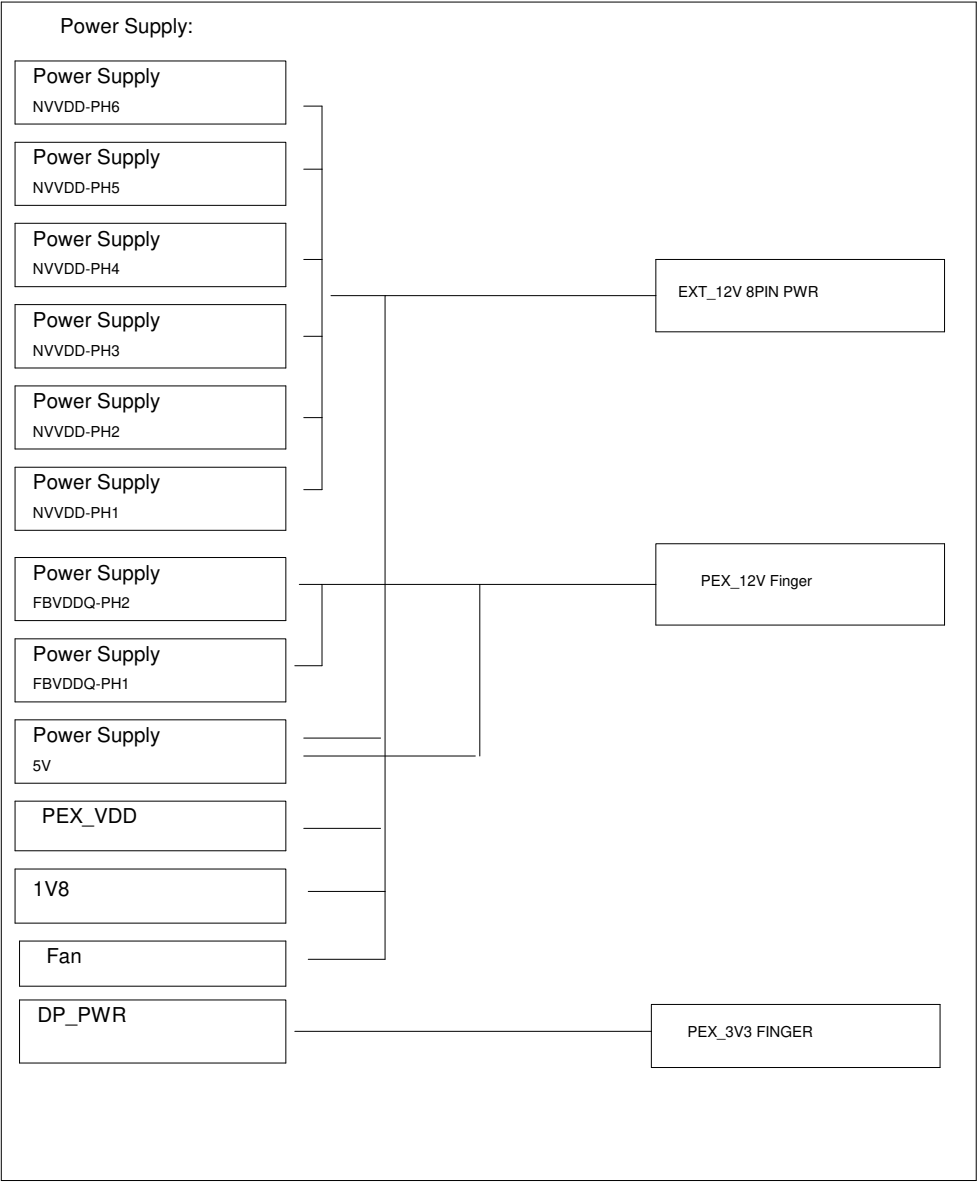
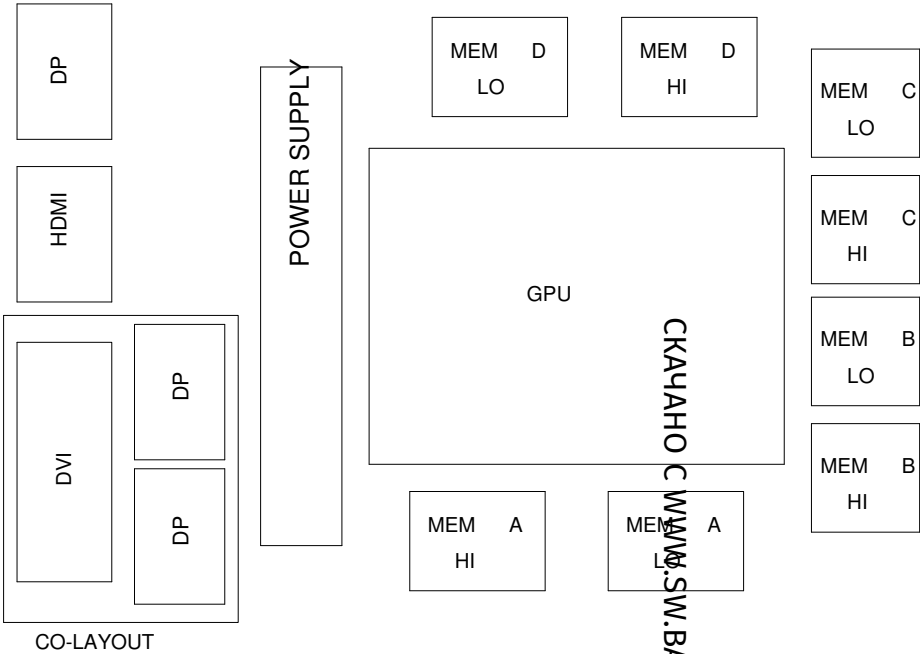
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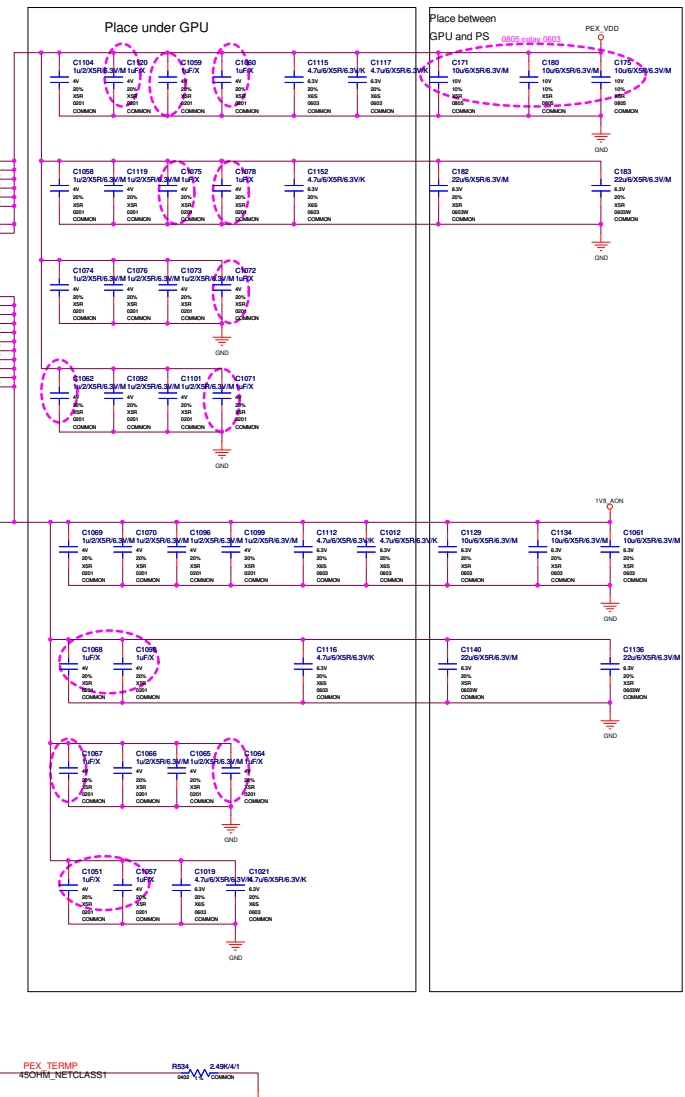
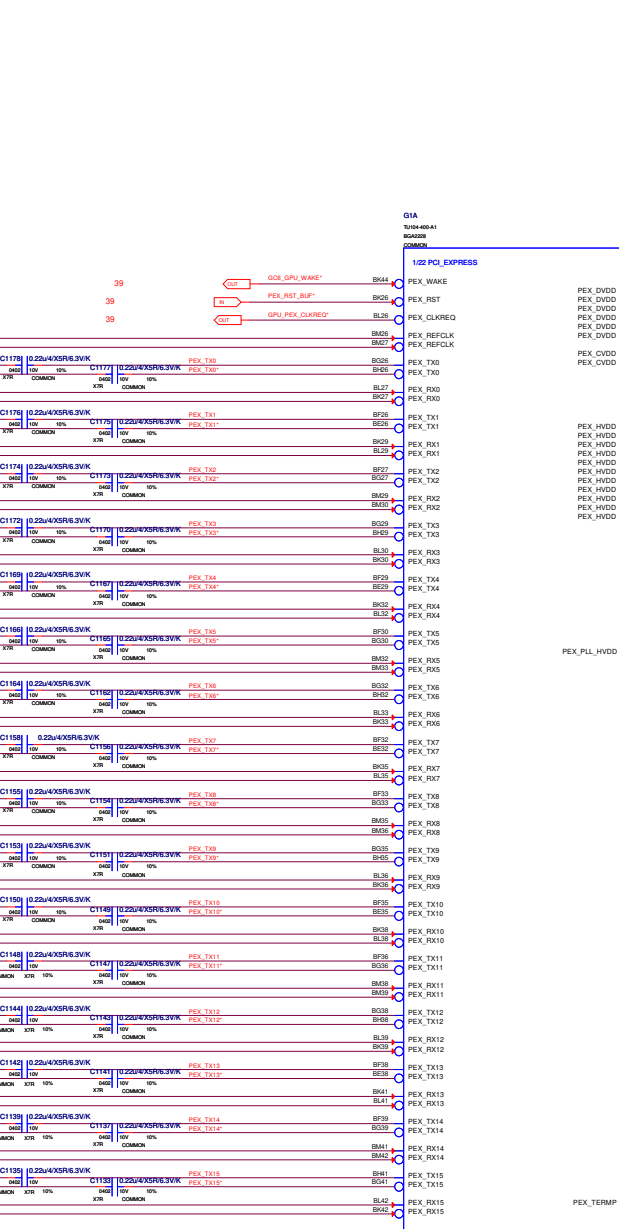
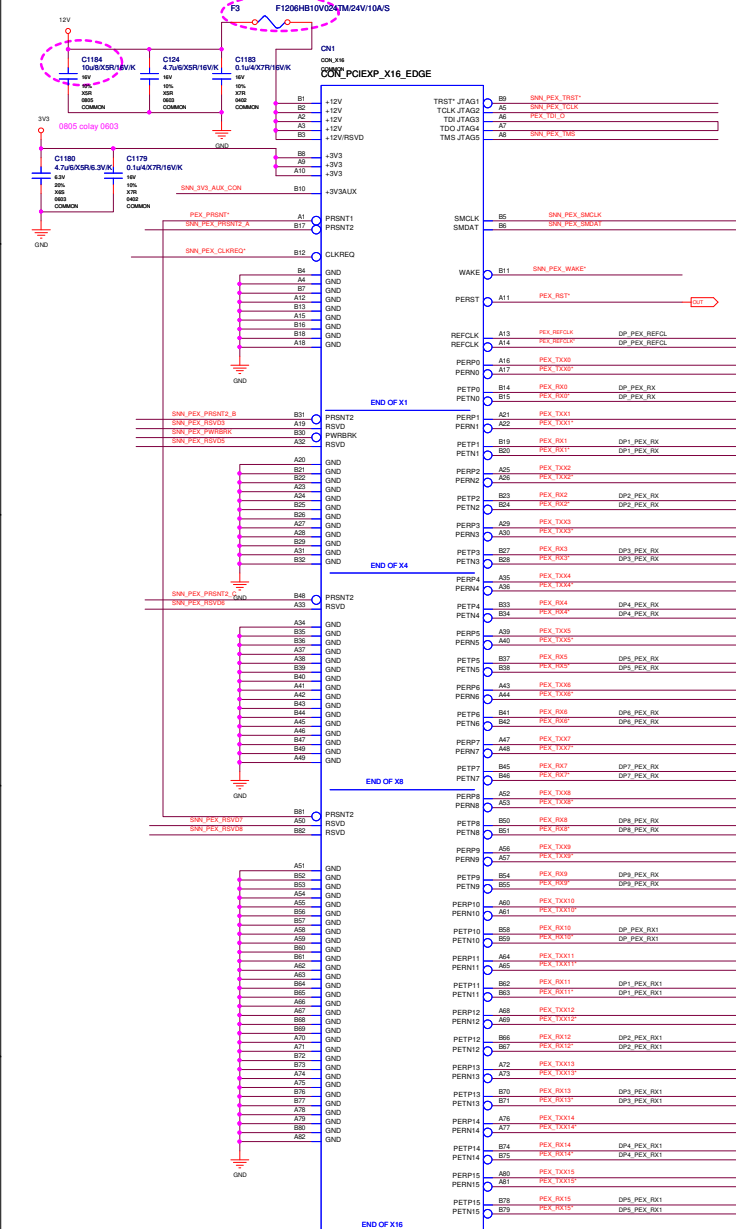
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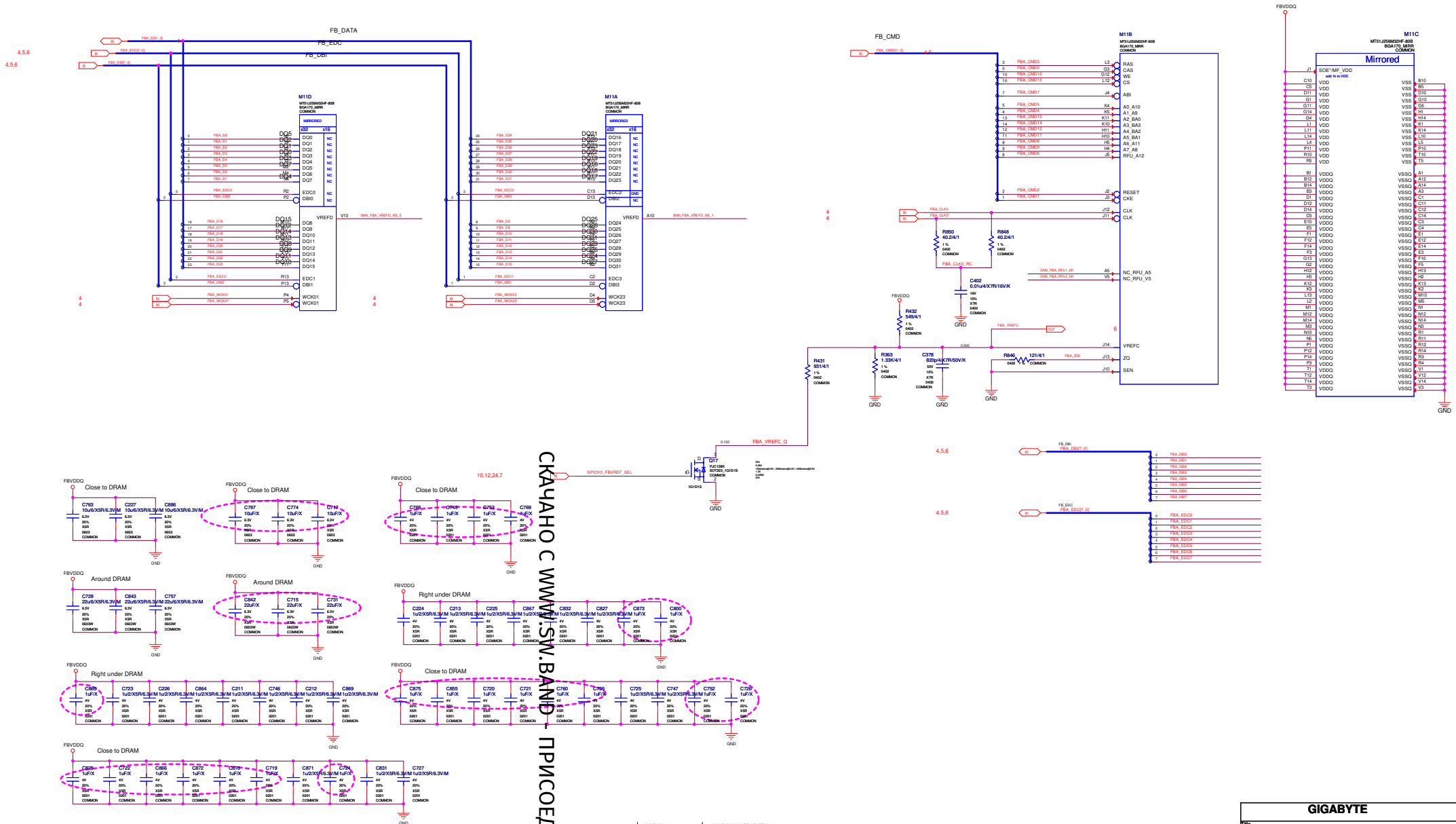
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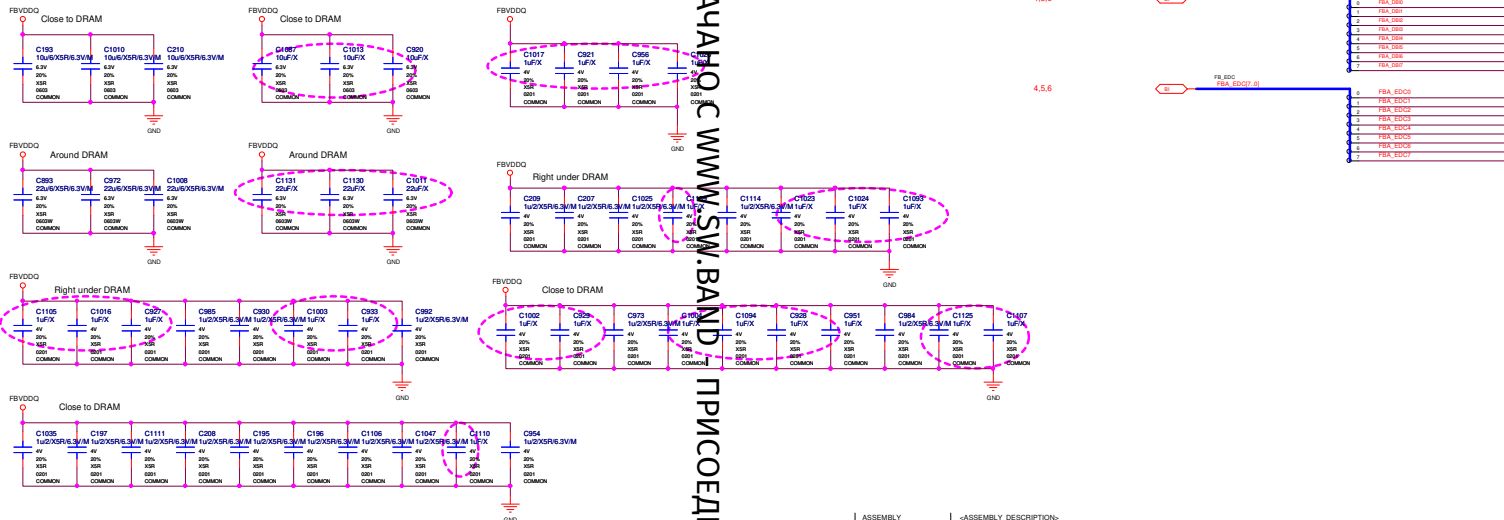
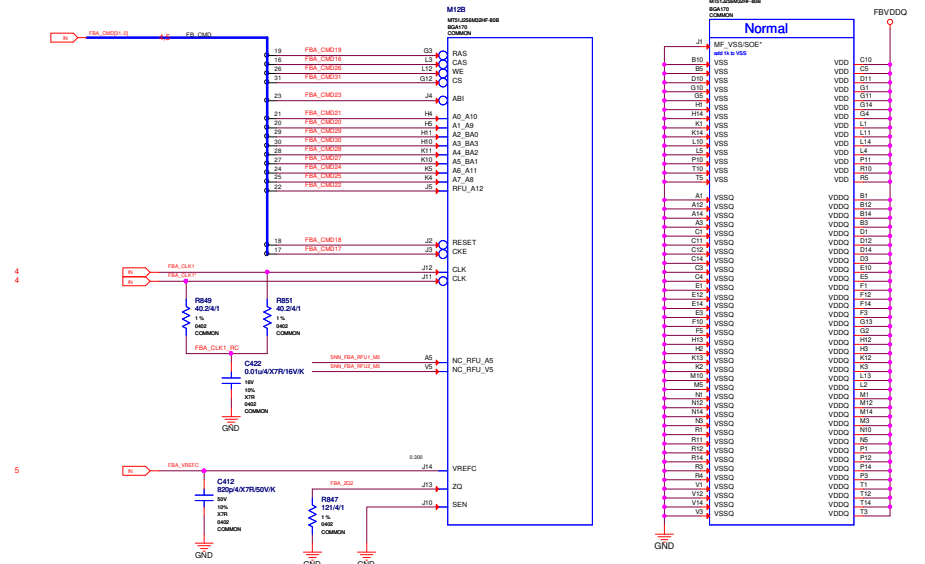
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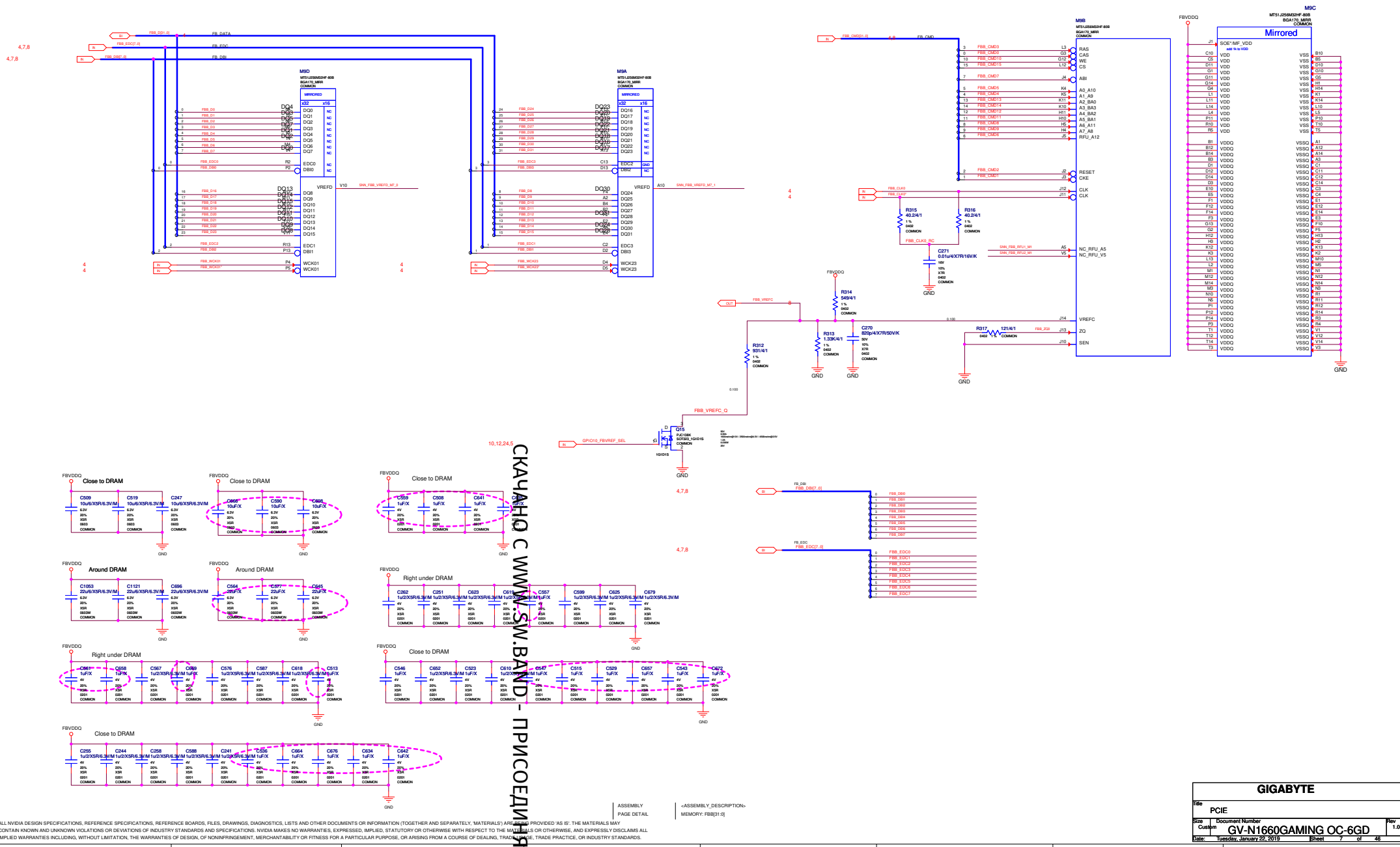












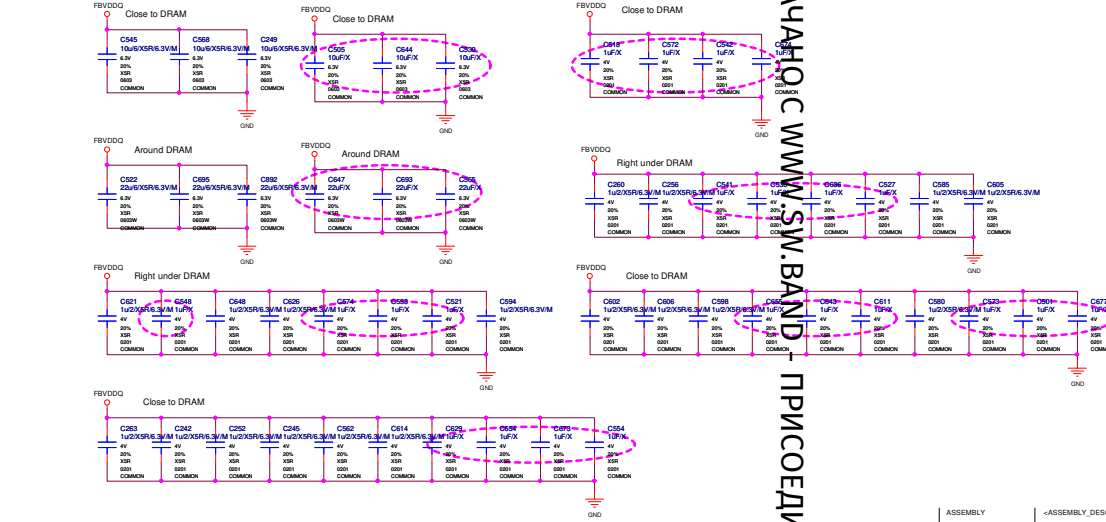
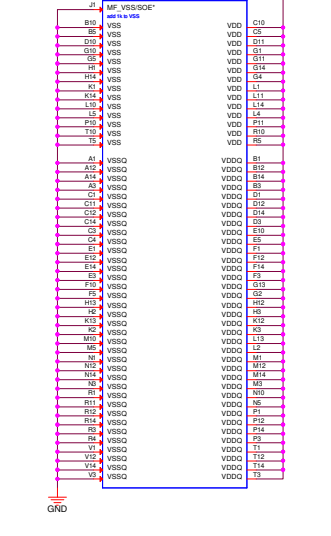
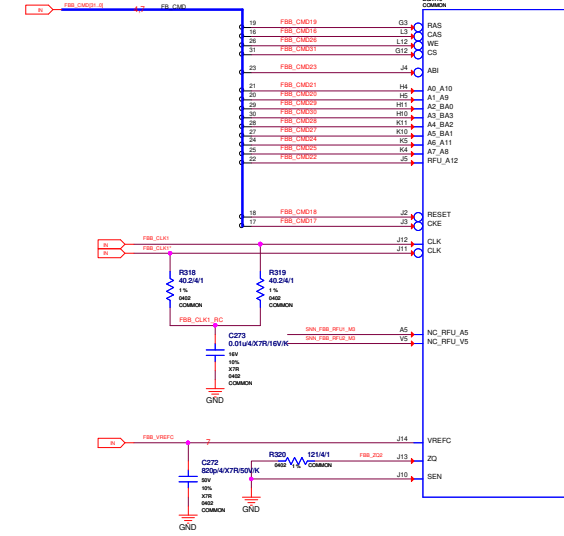
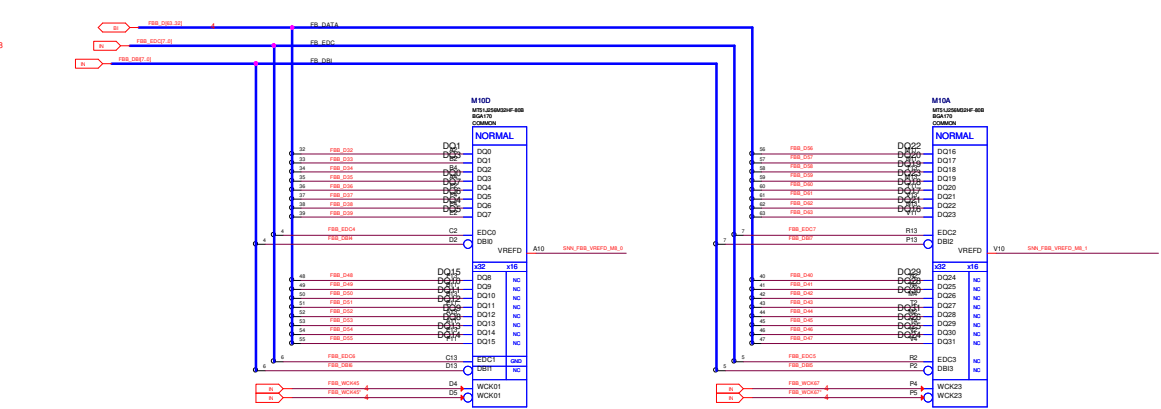
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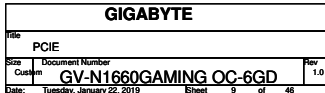
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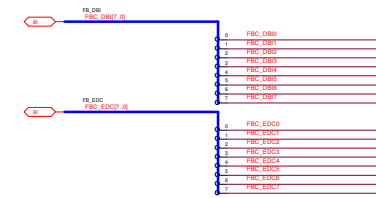
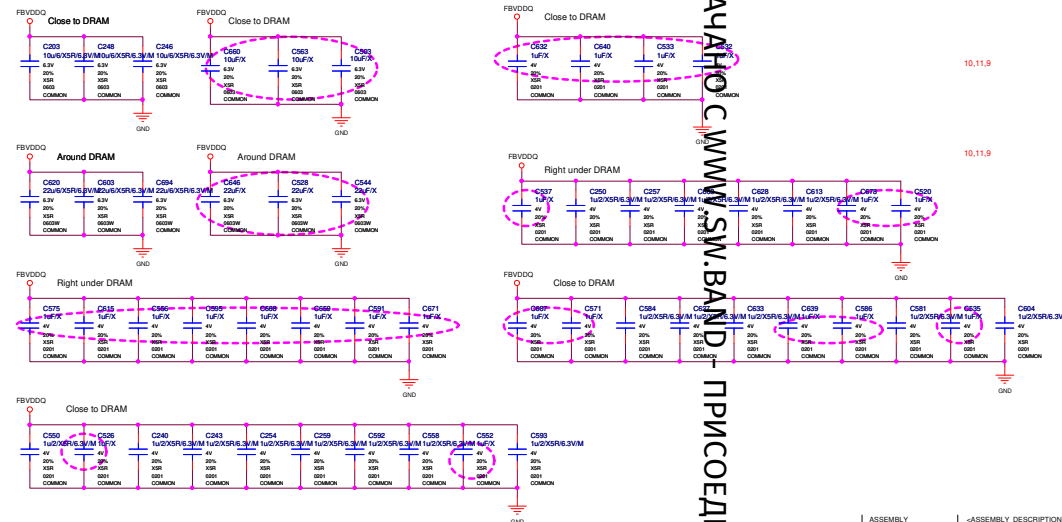
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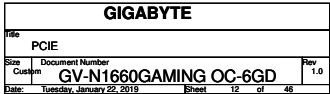
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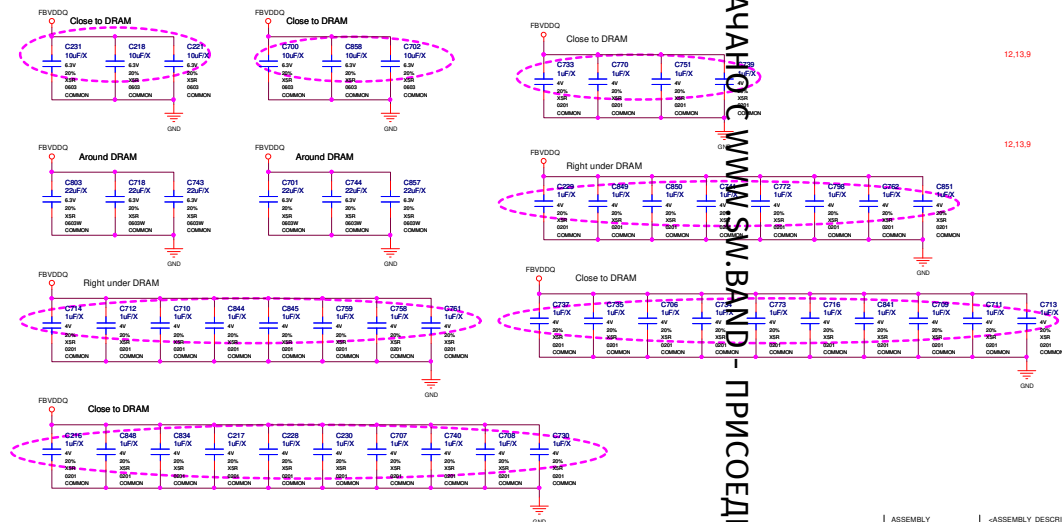
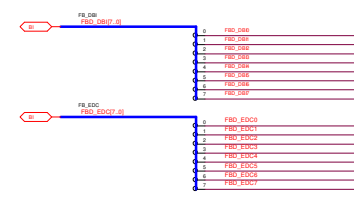
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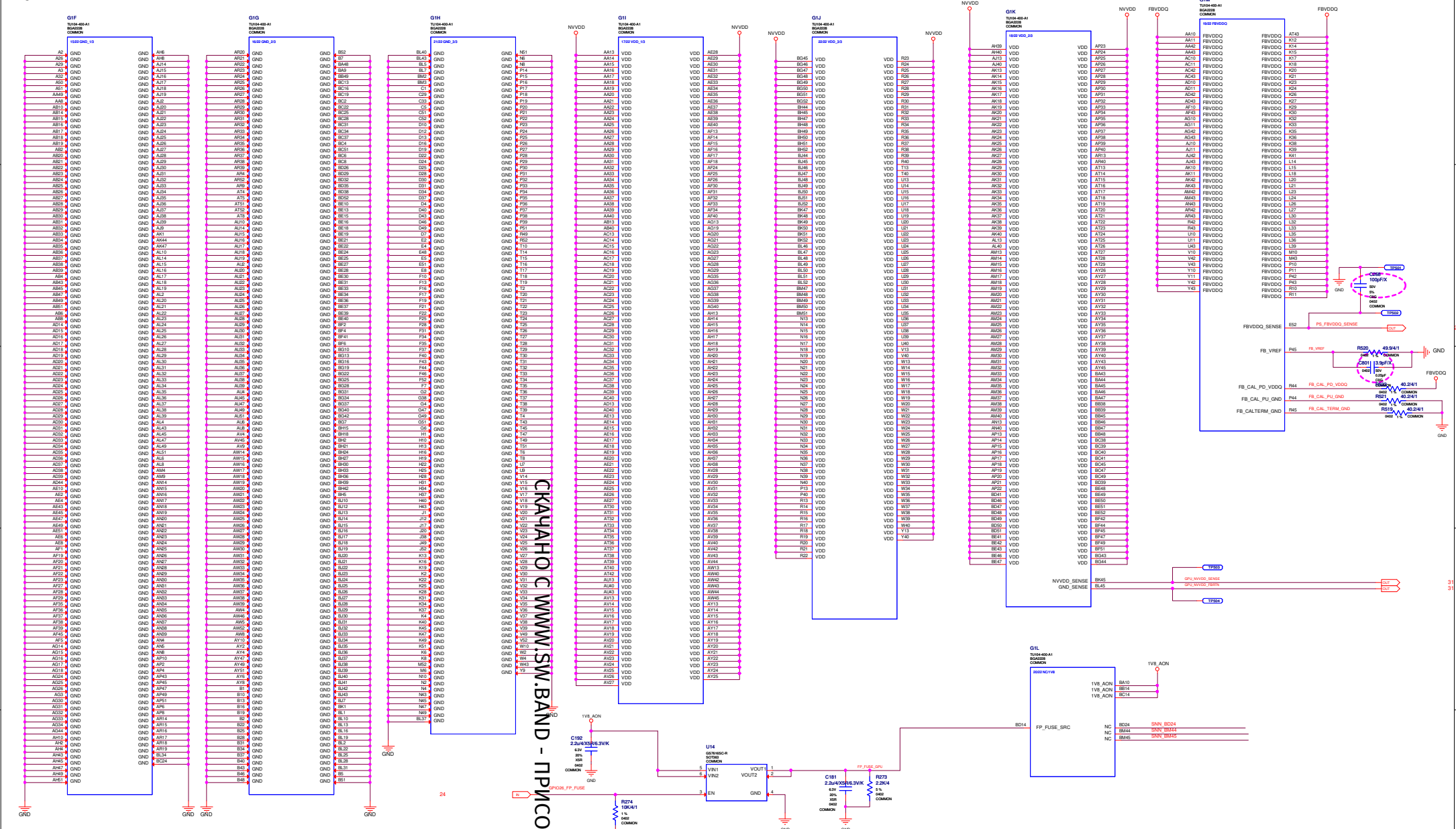
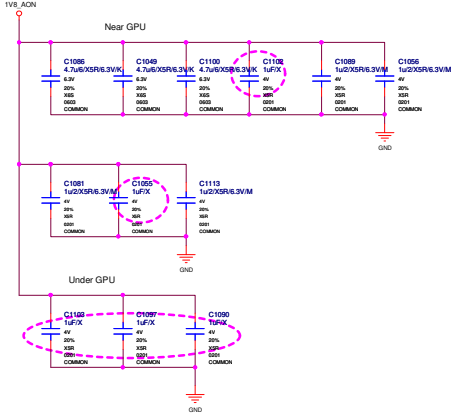


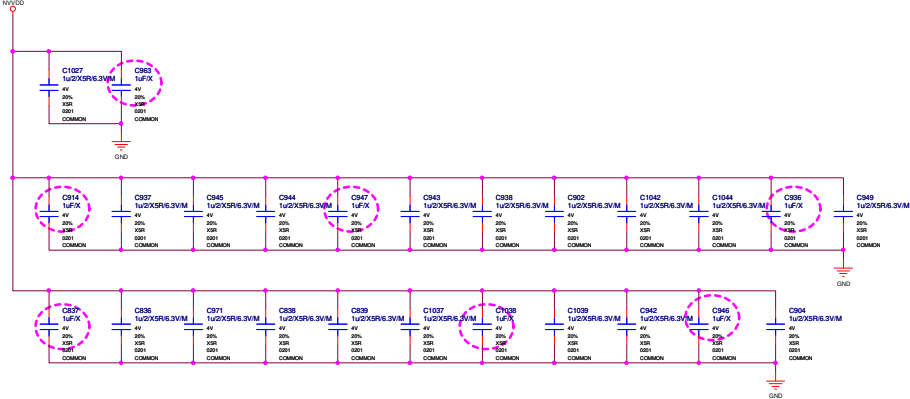
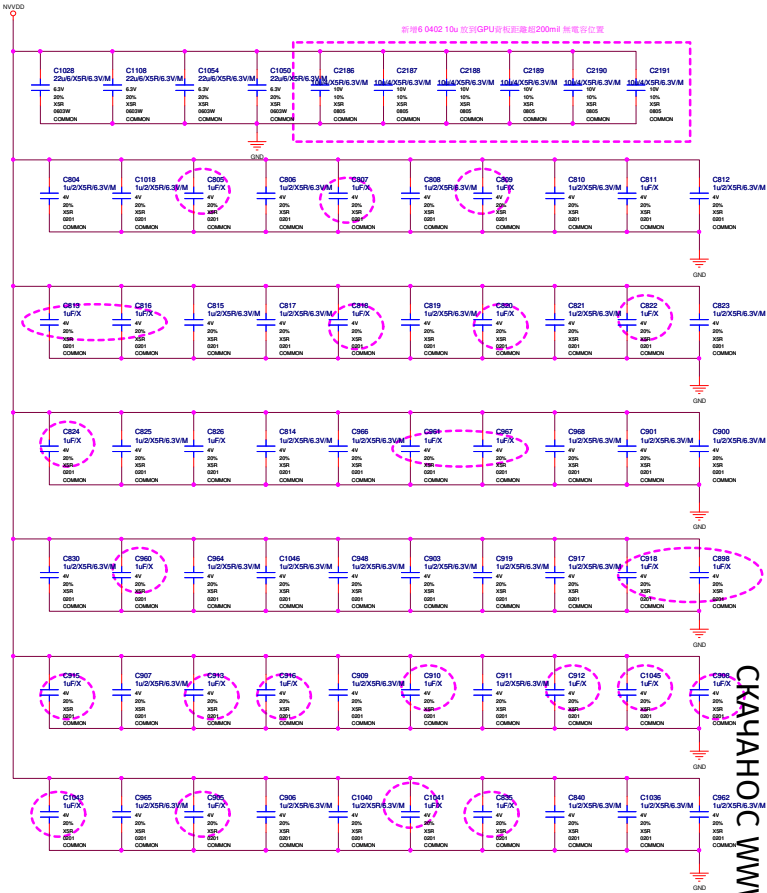
Figure 1 shows the schematic diagram of the four channels of the 12-bit DAC. The diagram is divided into four quadrants, each representing a different DAC channel. Each channel consists of a DAC core (C862, C997, C861, or C998) connected to a 330uA/2V/V/9m current source. The DAC cores are configured with COMMON, VREF, and ALP pins. The ALP pin is connected to a 5.00000V reference voltage. The DAC cores are connected to a 330uA/2V/V/9m current source. The DAC cores are connected to a 330uA/2V/V/9m current source. The DAC cores are connected to a 330uA/2V/V/9m current source.



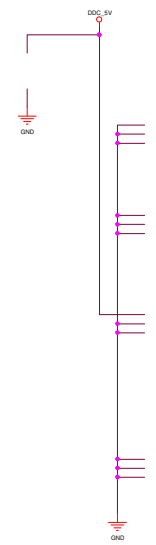
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PAGE DETAIL	GPU DECOUPLING 1

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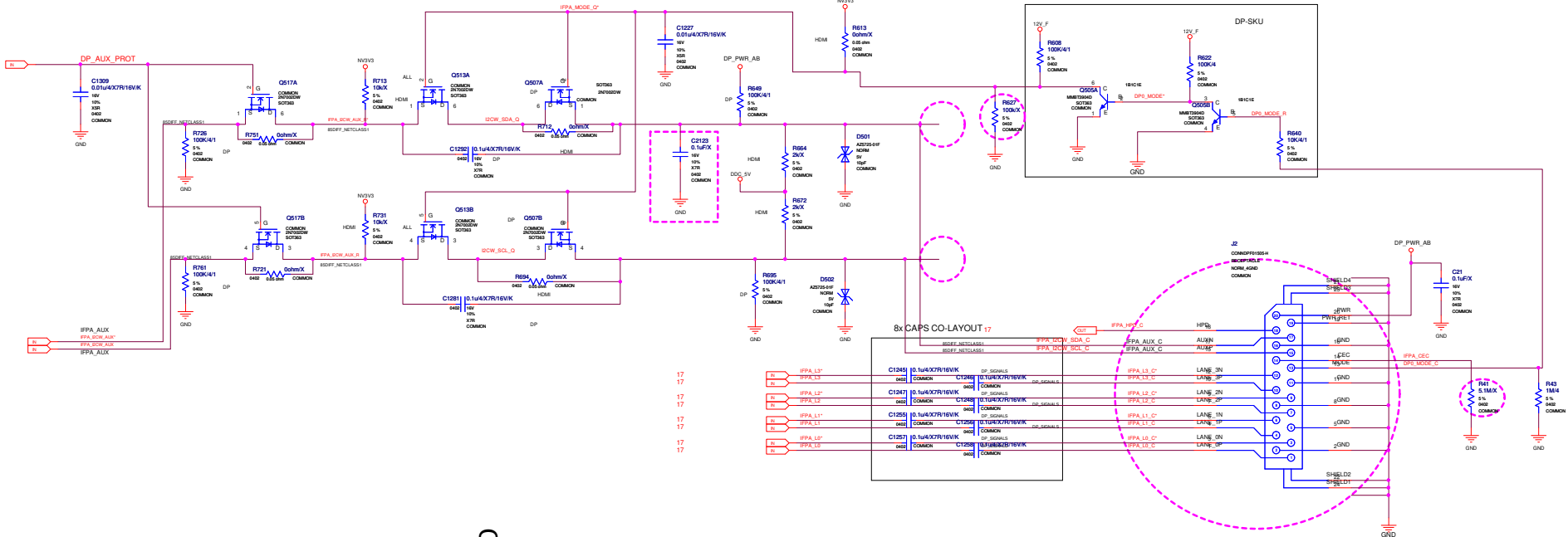
NVDD



КРАЙНОВОЕ WWW.SW.BAND - ПРИБОРАМИ

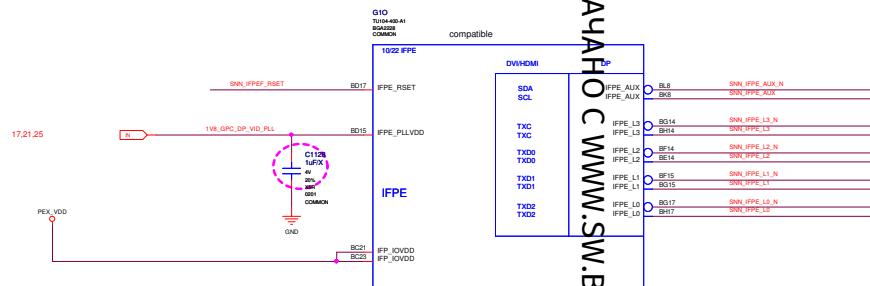


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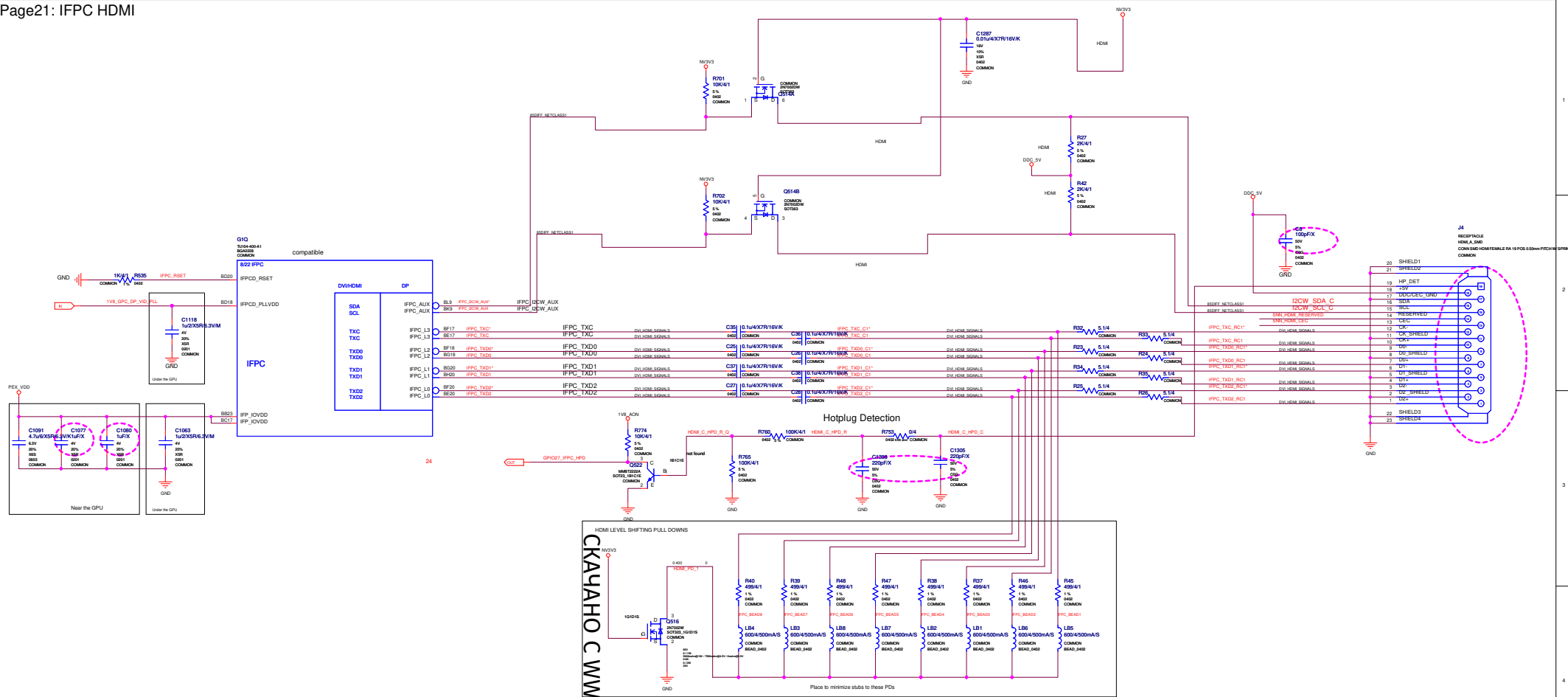


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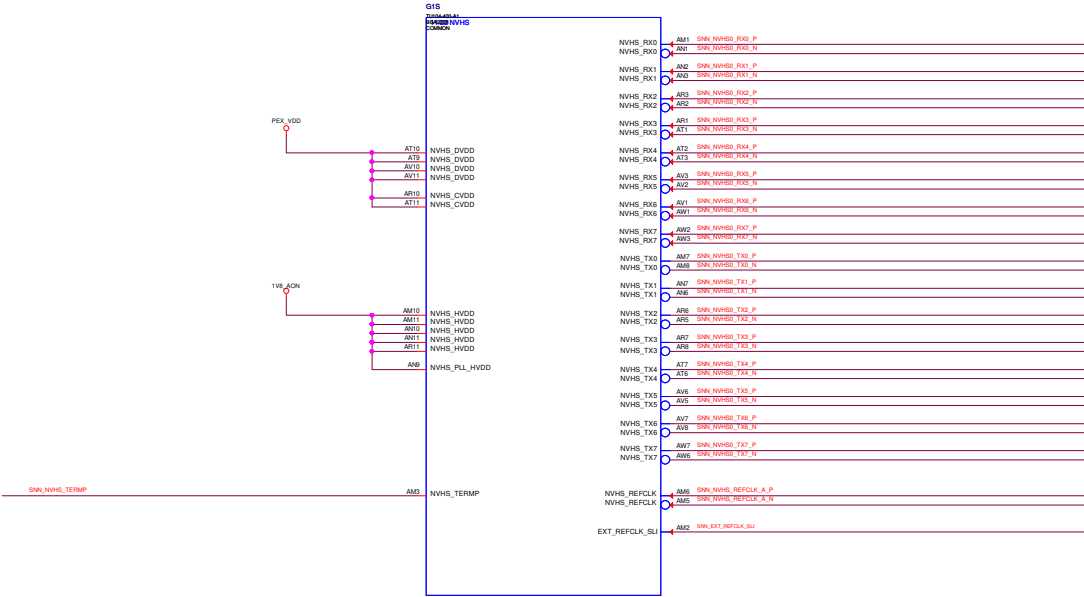


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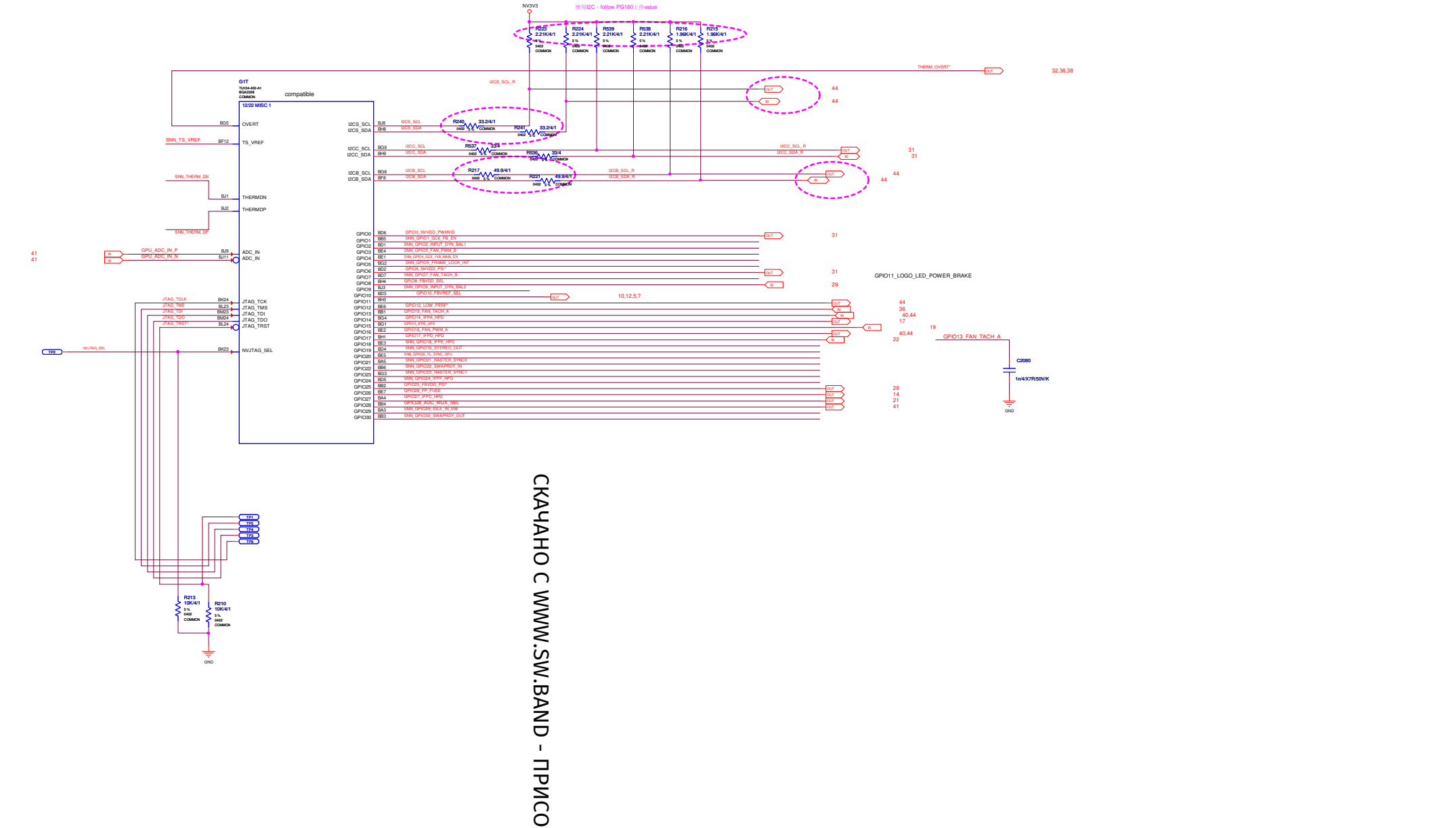




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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung 8Gb 256Mx32 K4G80325FC-HC25
L	L	H	0001	Micron 8Gb 256Mx32 MT51J256M32HF-80:B
L	H	L	0010	Hynix 8Gb 256Mx32 H5GC8H24AJR-R2C
L	H	H	0011	Hynix 8Gb 256Mx32 H5GQ8H24MJR-R4C
H	H	L	0110	
H	H	H	0111	
L	L	M	1000	
L	M	L	1001	

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0].FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	L	M	1	0	0	0
L	L	L	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

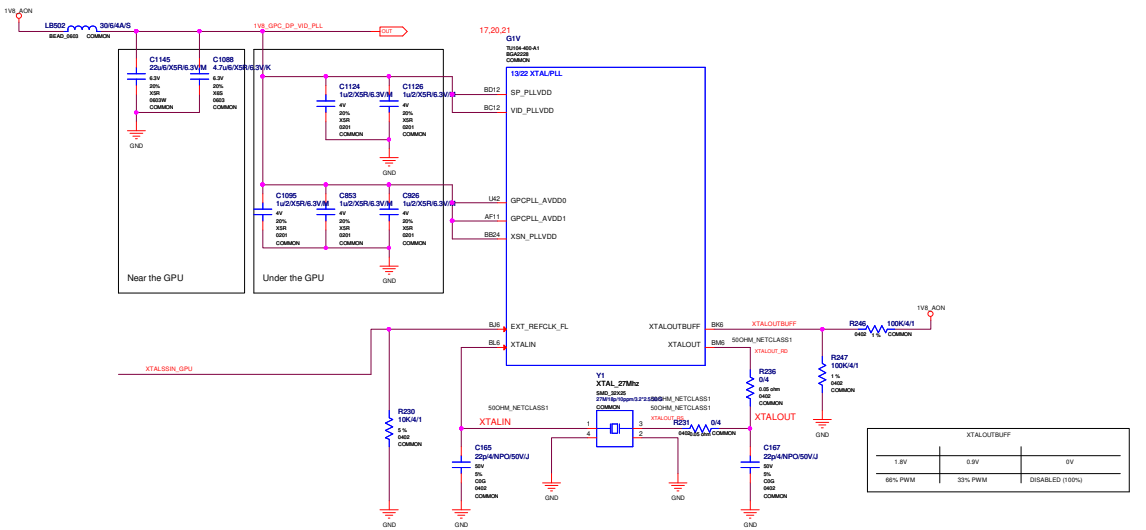
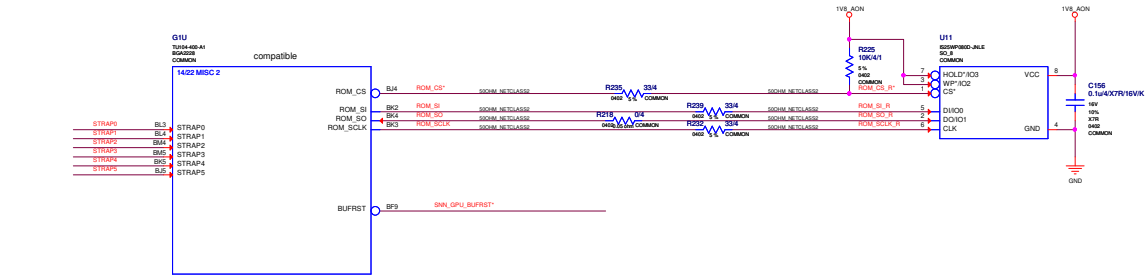
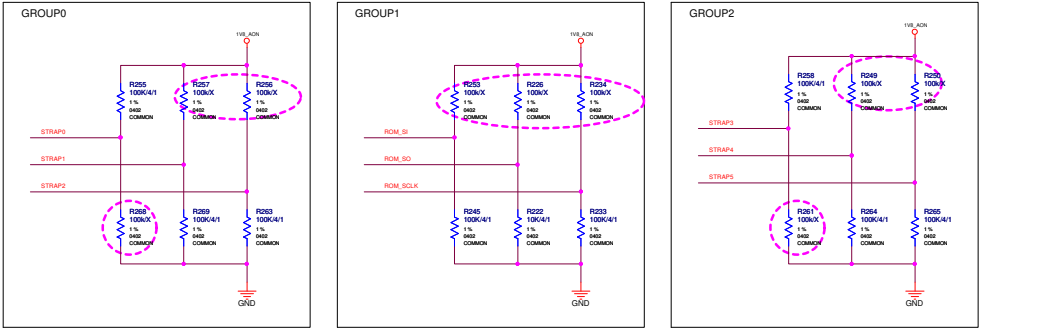
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



XTALOUTBUFF	XTALOUT	XTALOUTBUFF
1.8V	0.9V	0V
80% PWM	33% PWM	DISABLED (100%)

GIGABYTE

PCIE

Size: 16GB

Document Number: GV-N1660GAMING OC-6GD

Date: Tuesday, January 22, 2019

Rev: 1.0

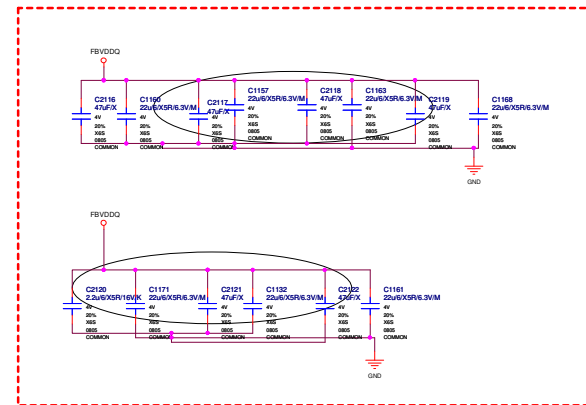
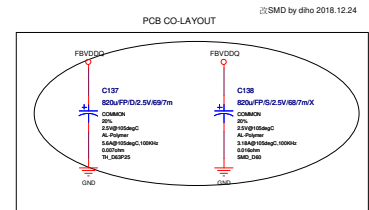


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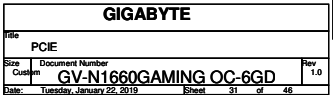
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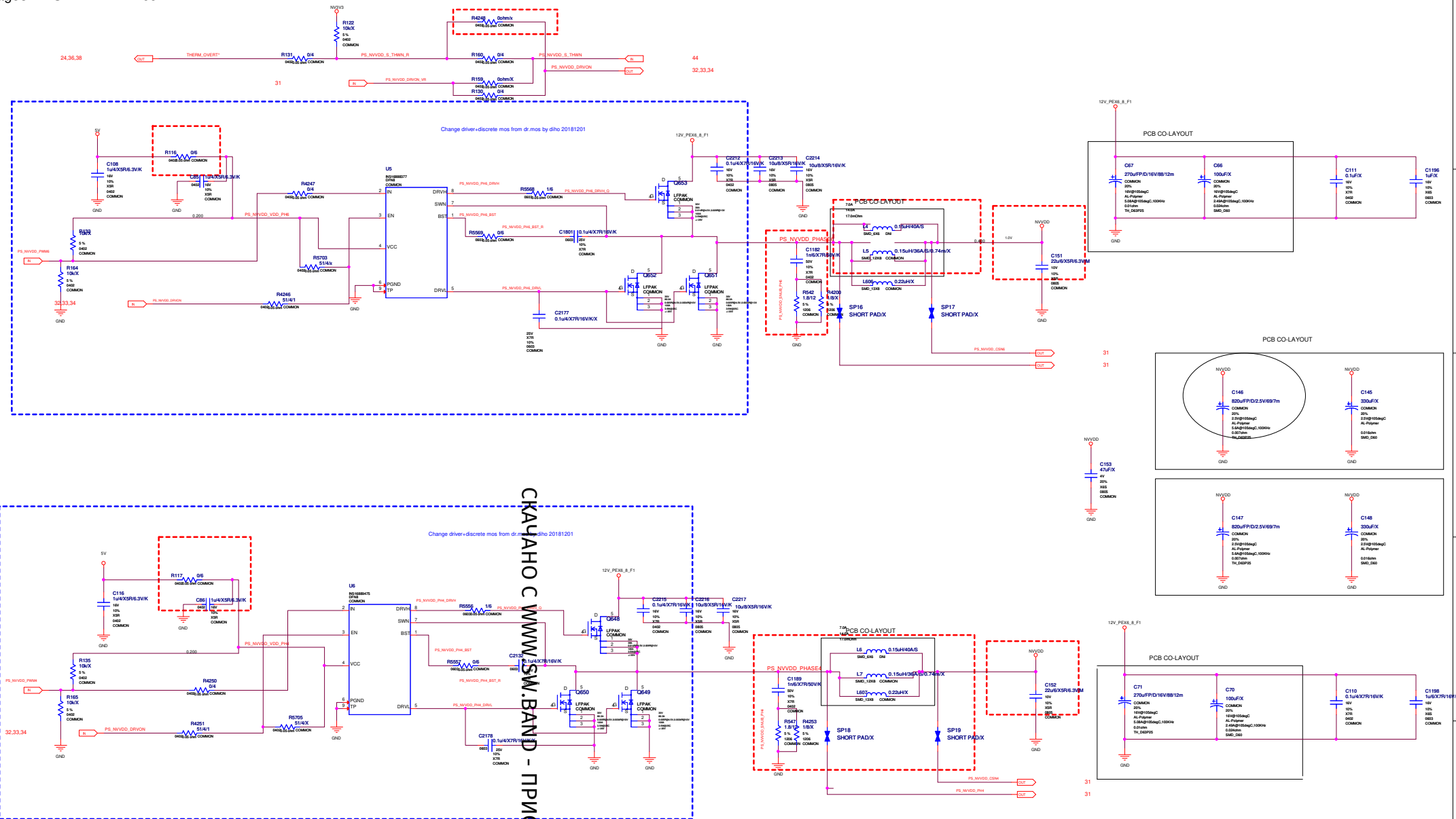
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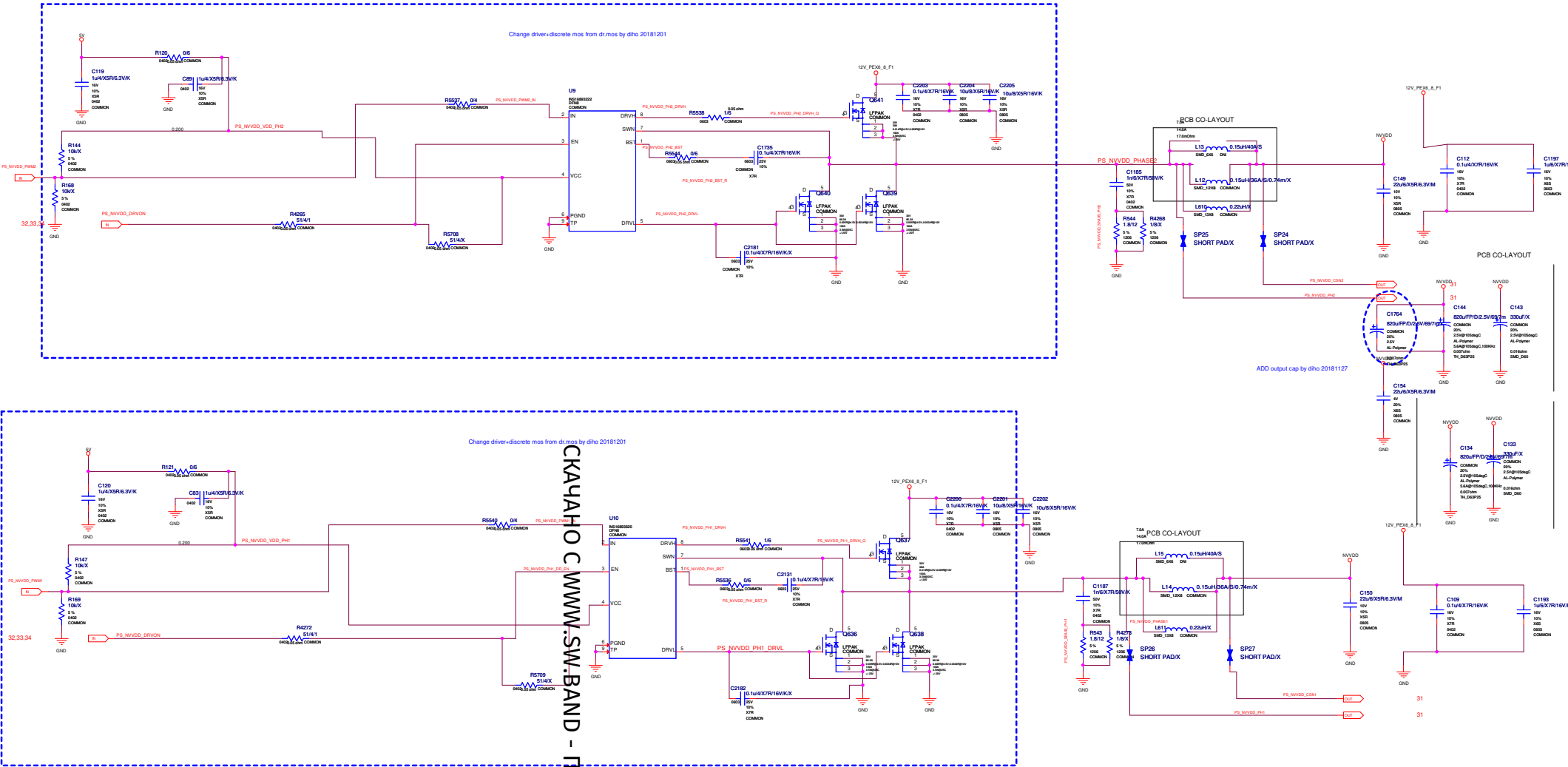


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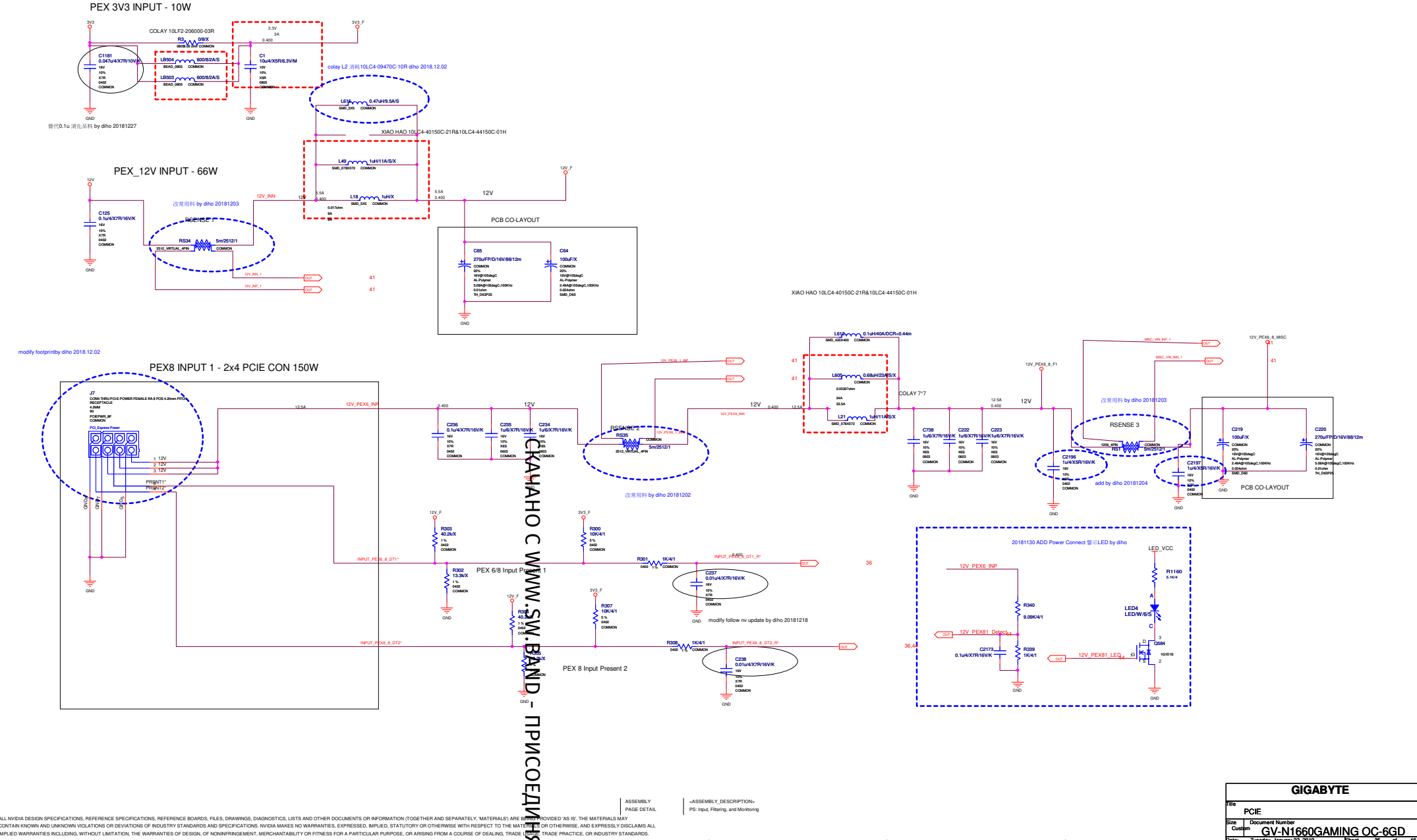


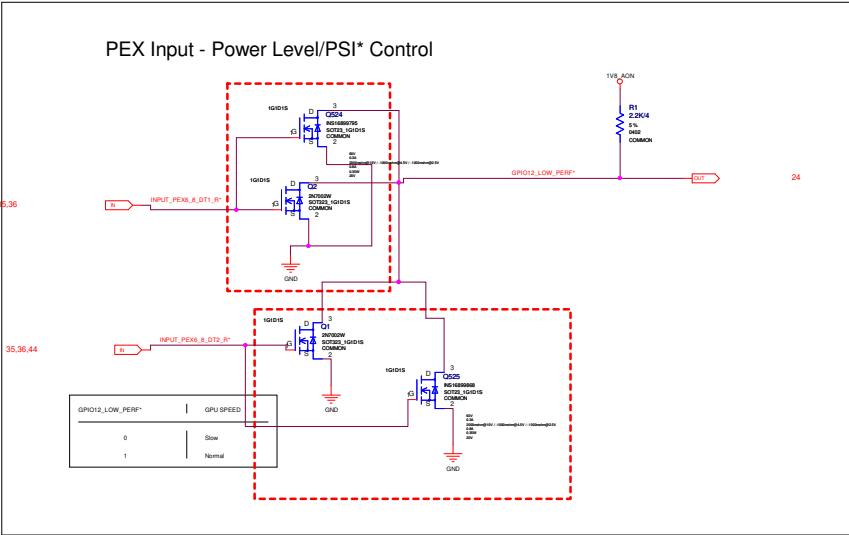
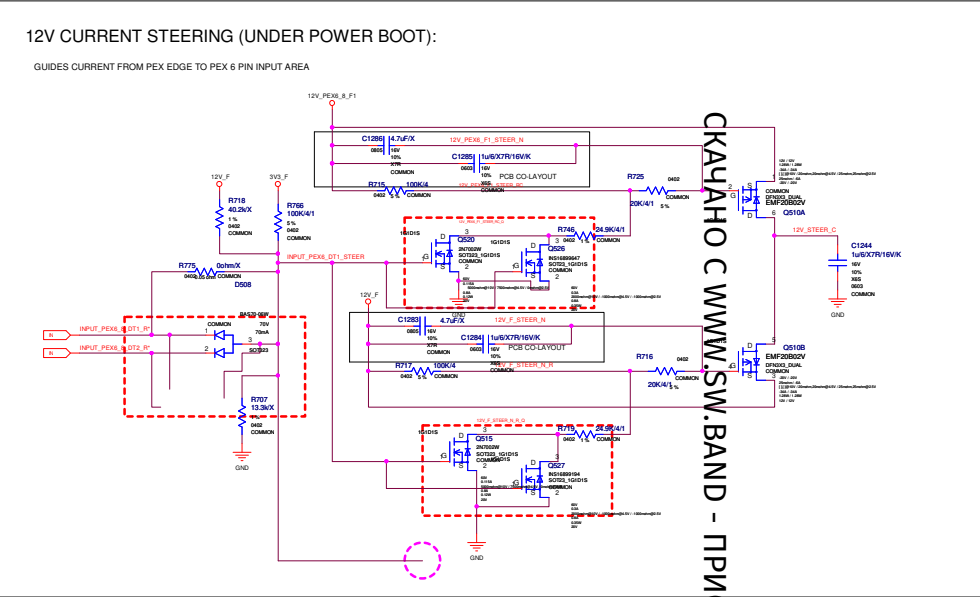
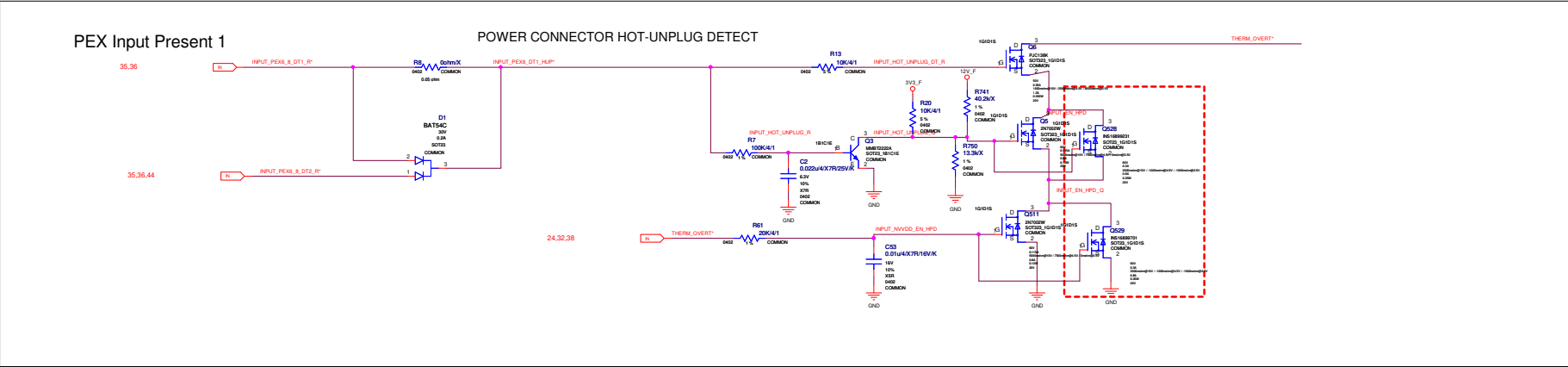






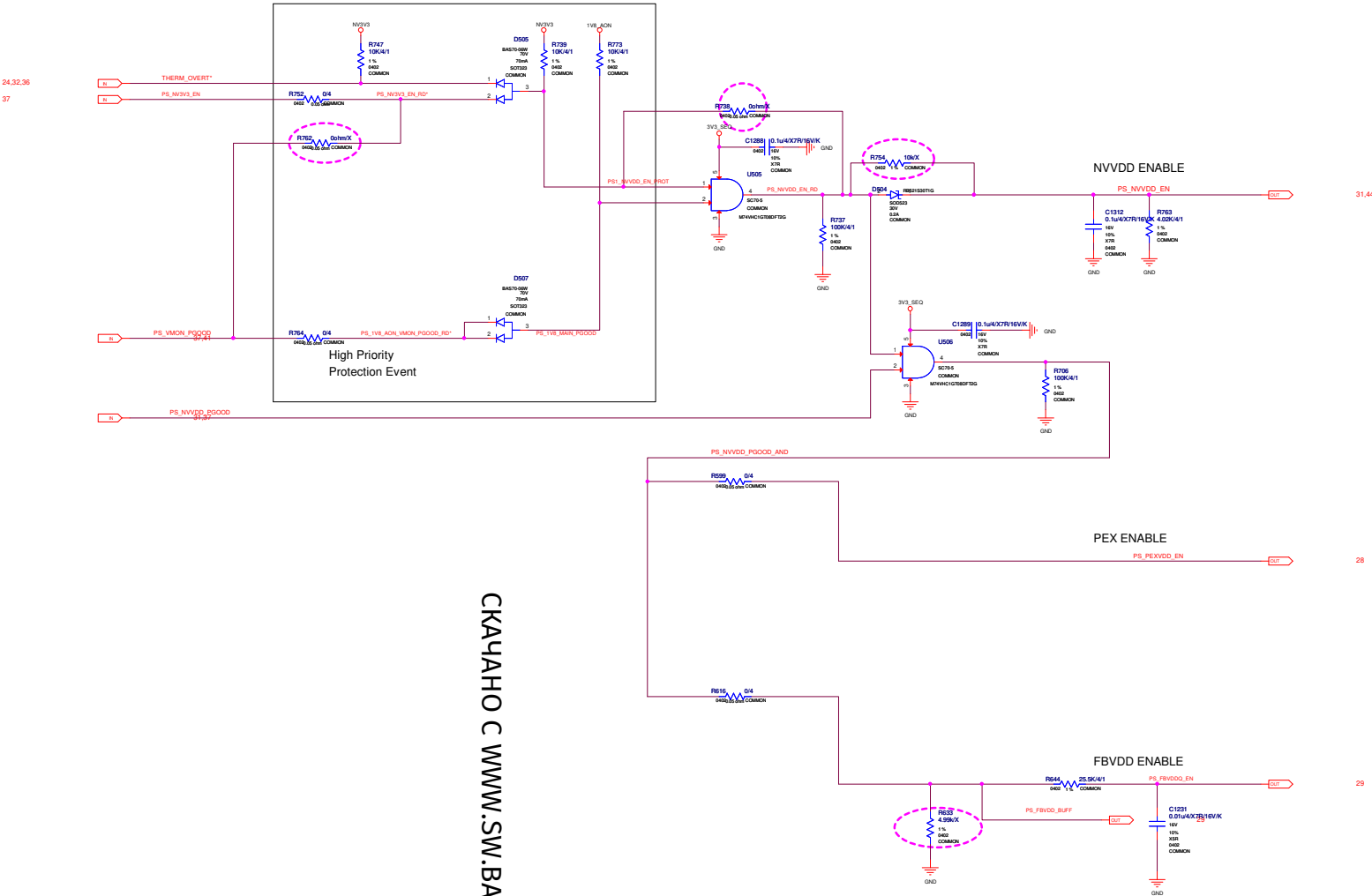
Page38: PS: Inputs, Filtering, and Monitoring



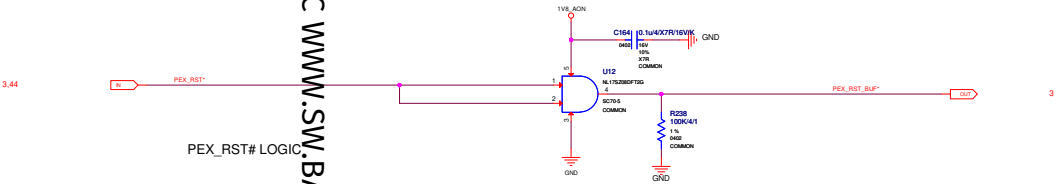
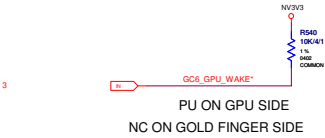
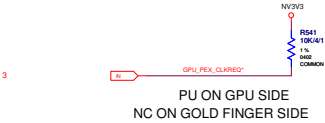




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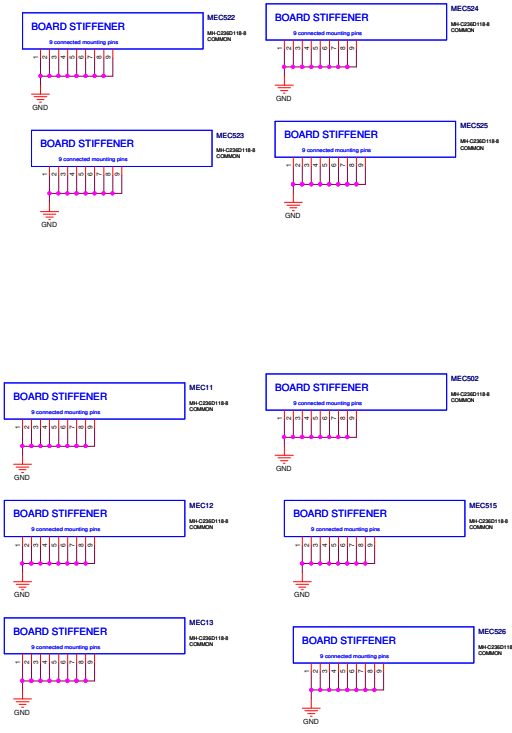
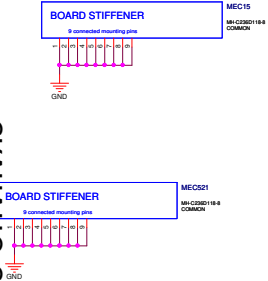
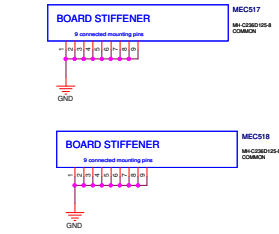
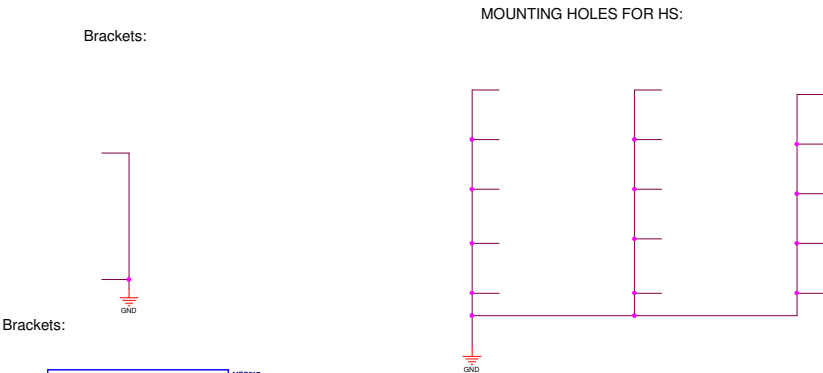


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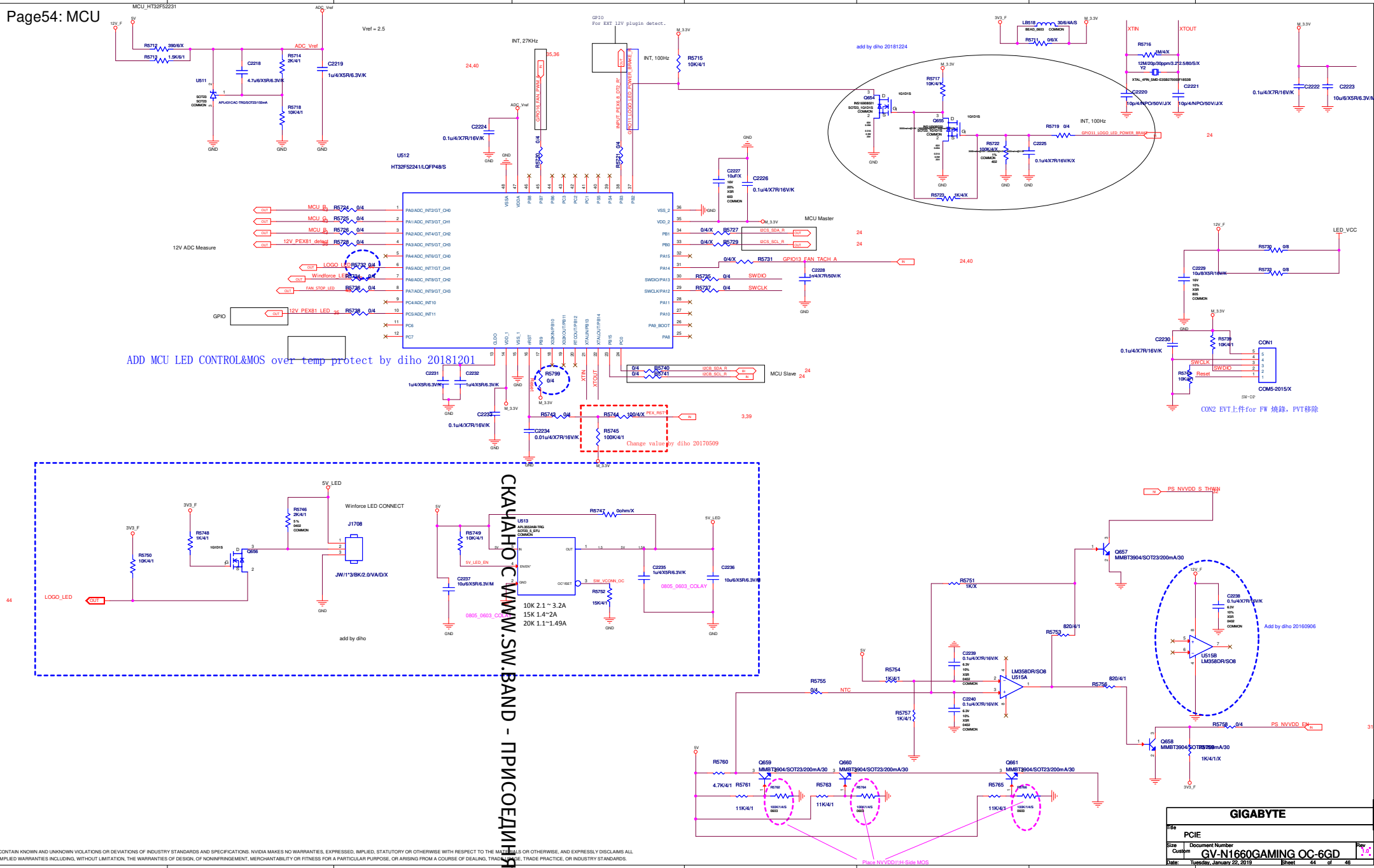


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СКАЧАТЬ С WWW.SW.BAND - ПРИСОЕДИНИТЬСЯ



A	B	C	D	E	F	G	H
1							
2							
3							
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5							

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History

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2019.01.04	First version

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