

GP104 - 8GB GDDR5, 256b, 256Mx32
 Tall DVI-D + DP + DP + DP/HDMI + DP

Page	Description
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1	Table of Contents
2	Block Diagram
3	PCI Express
4	MEMORY: GPU Partition A/B
5	MEMORY: FBA[31:0]
6	MEMORY: FBA[63:32]
7	MEMORY: FBB[31:0]
8	MEMORY: FBB[63:32]
9	MEMORY: GPU Partition C/D
10	MEMORY: FBC[31:0]
11	MEMORY: FBC[63:32]
12	MEMORY: FBD[31:0]
13	MEMORY: FBD[63:32]
14	GPU PWR and GND
15	GPU Decoupling
16	IFPAB DVI-D-DL
17	IFPE DP
18	IFPEF DP
19	IFPC HDMI 2.0/DP
20	IFPD DP
21	MIOA/B Interface and Frame Lock
22	MISC1; Fan, Thermal, JTAG, GPIO, Stereo
23	MISC2: ROM, XTAL, Straps
24	PS: 1V8, 1V8_AON
25	PS: 5V, PEX_VDD

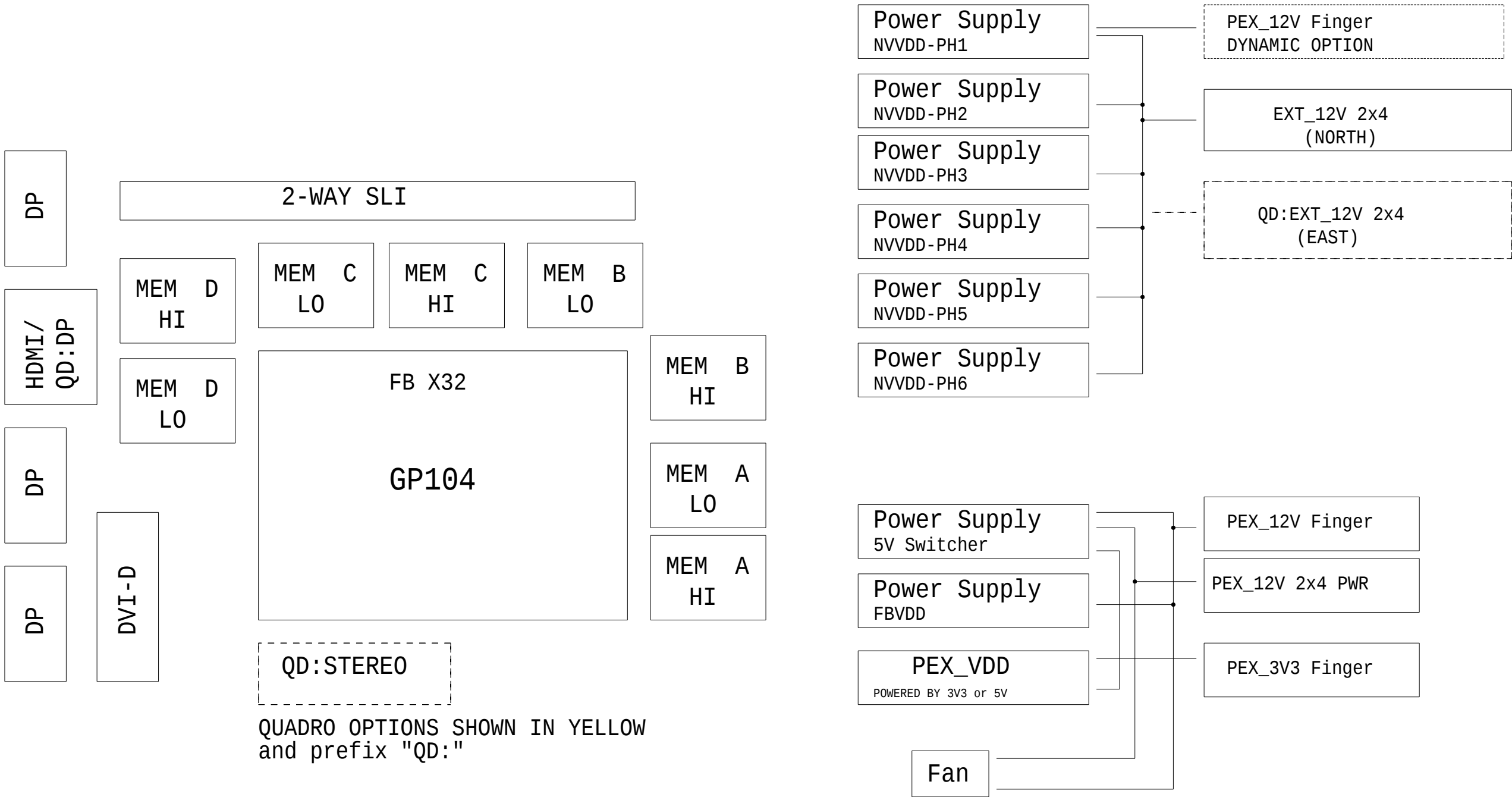
Page	Description
26	PS: FBVDD
27	PS: NVVDD_OVR8
28	PS: Blank Page
29	PS: NVVDD Phase 1-4
30	PS: NVVDD Phase 5 & 6
31	PS: Blank Page
32	PS: Dynamic Power Balance Phases
33	PS: Dynamic Power Balance Logic
34	PS: NV3V3, NV12V
35	PS: Inputs, Filtering, and Monitoring
36	PS: Shutdown and Sequencing
37	PS: 12V Current Steering PSI Control and LED
38	MECH: Bracket/Thermal

ASSEMBLY	SKU0020 SCHEMATIC COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Table of Contents

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NV_PN	600-1G411-0020-110		
PCB REV	16411-A01	PAGE	1 OF 38
BOM REV	B	DATE	30-JUN-2016

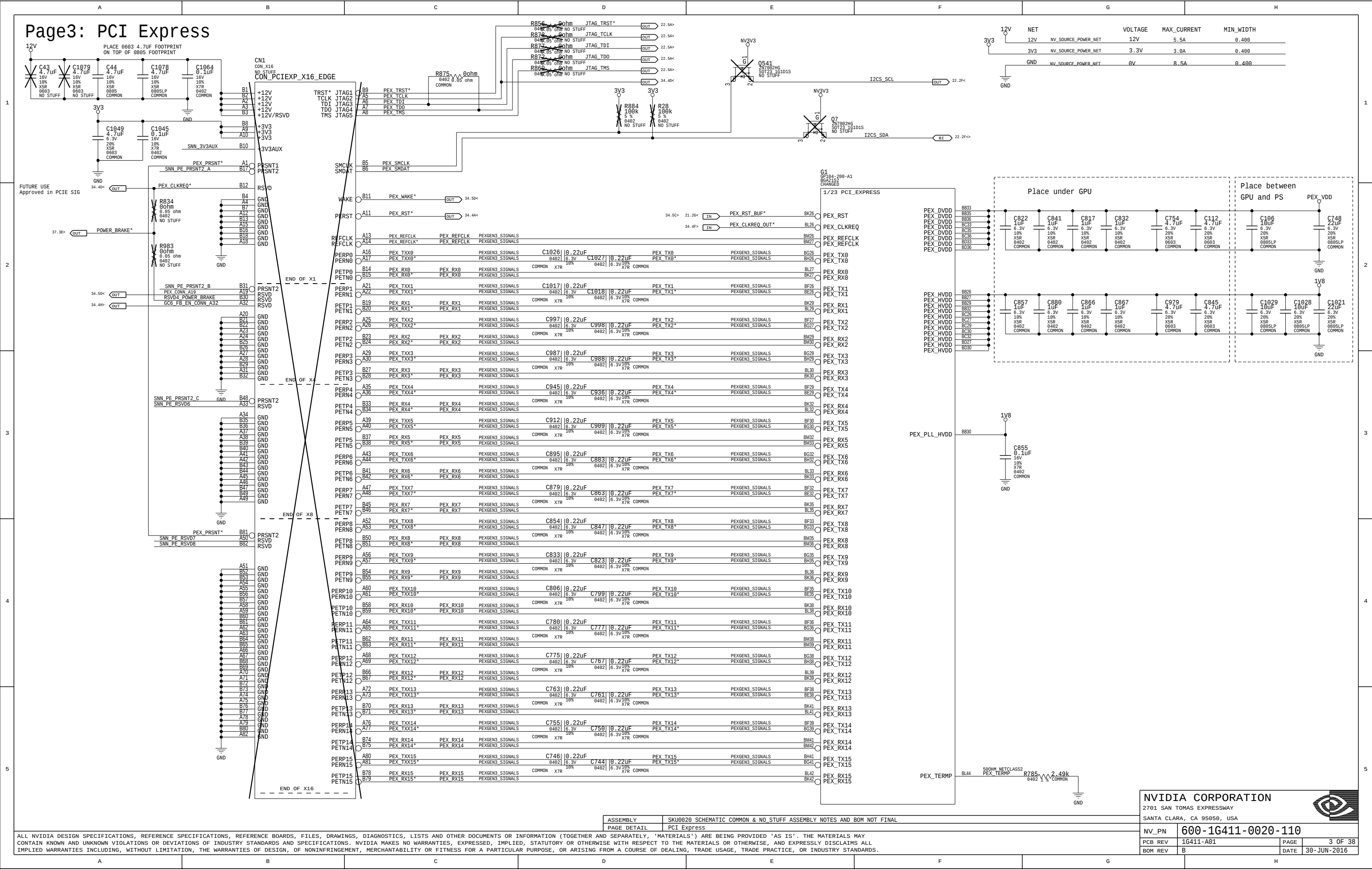
Page2: Block Diagram

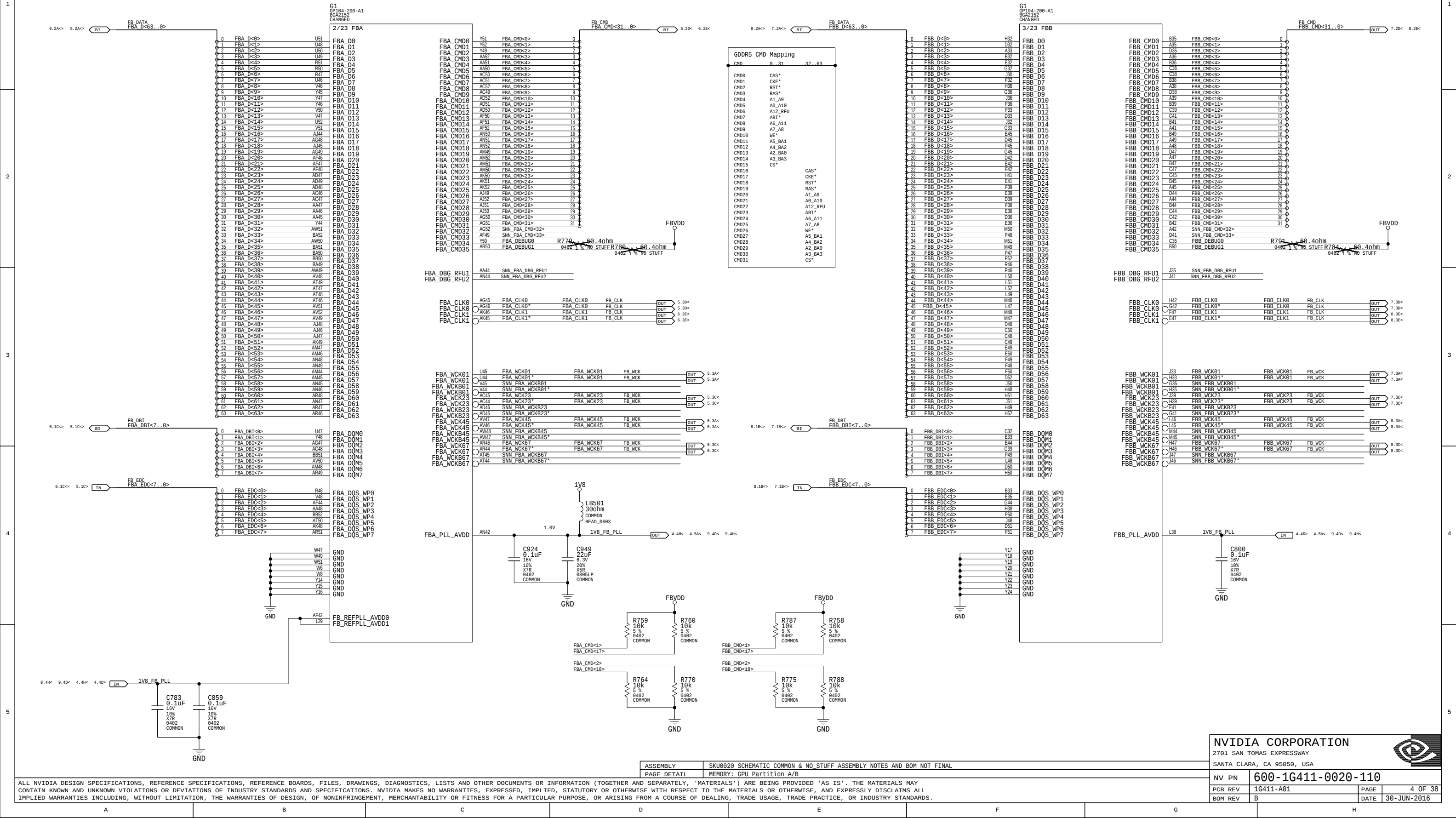


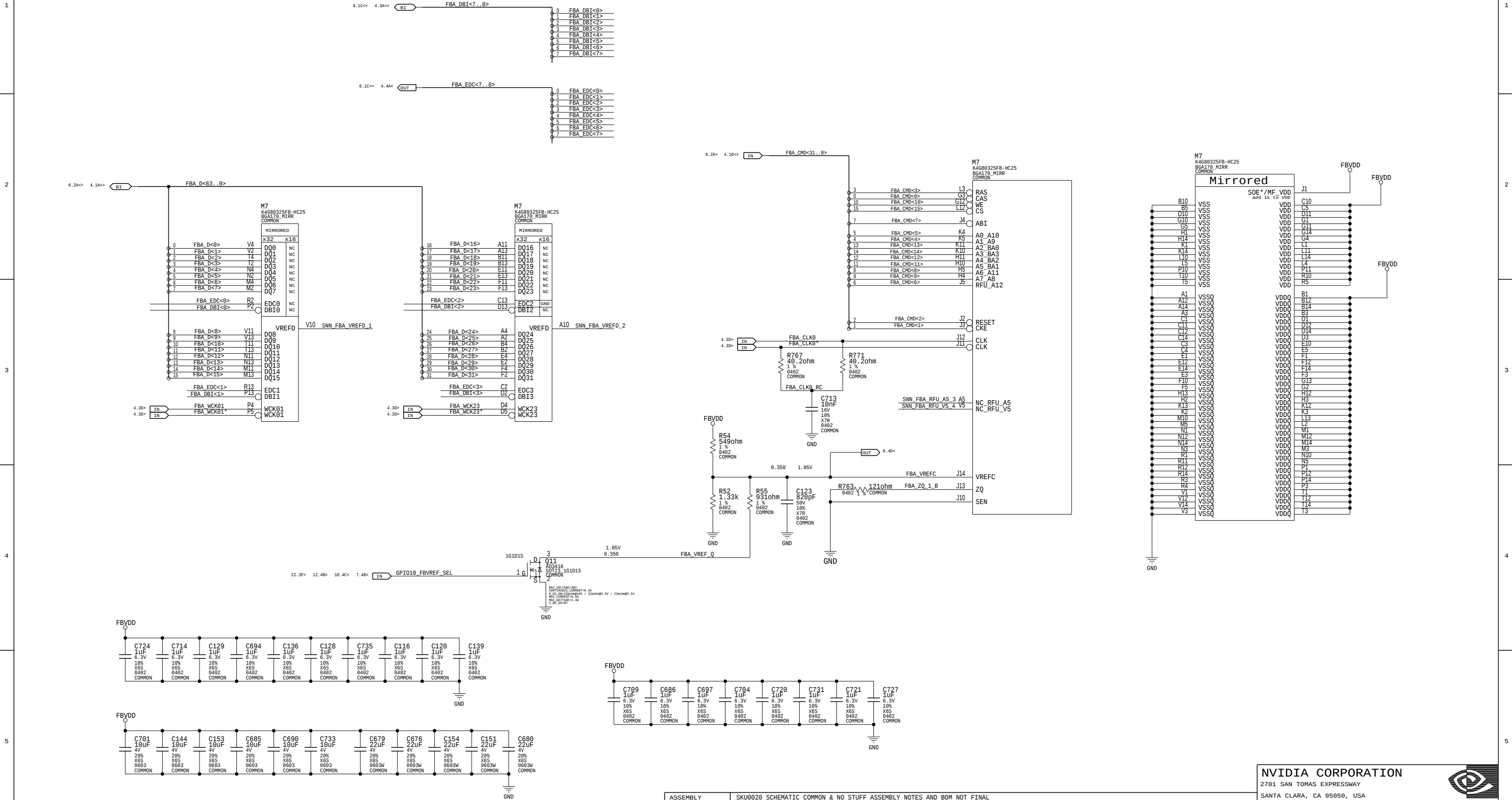
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NV_PN	600-1G411-0020-110		
PCB REV	1G411-A01	PAGE	2 OF 38
BOM REV	B	DATE	30-JUN-2016

Page3: PCI Express







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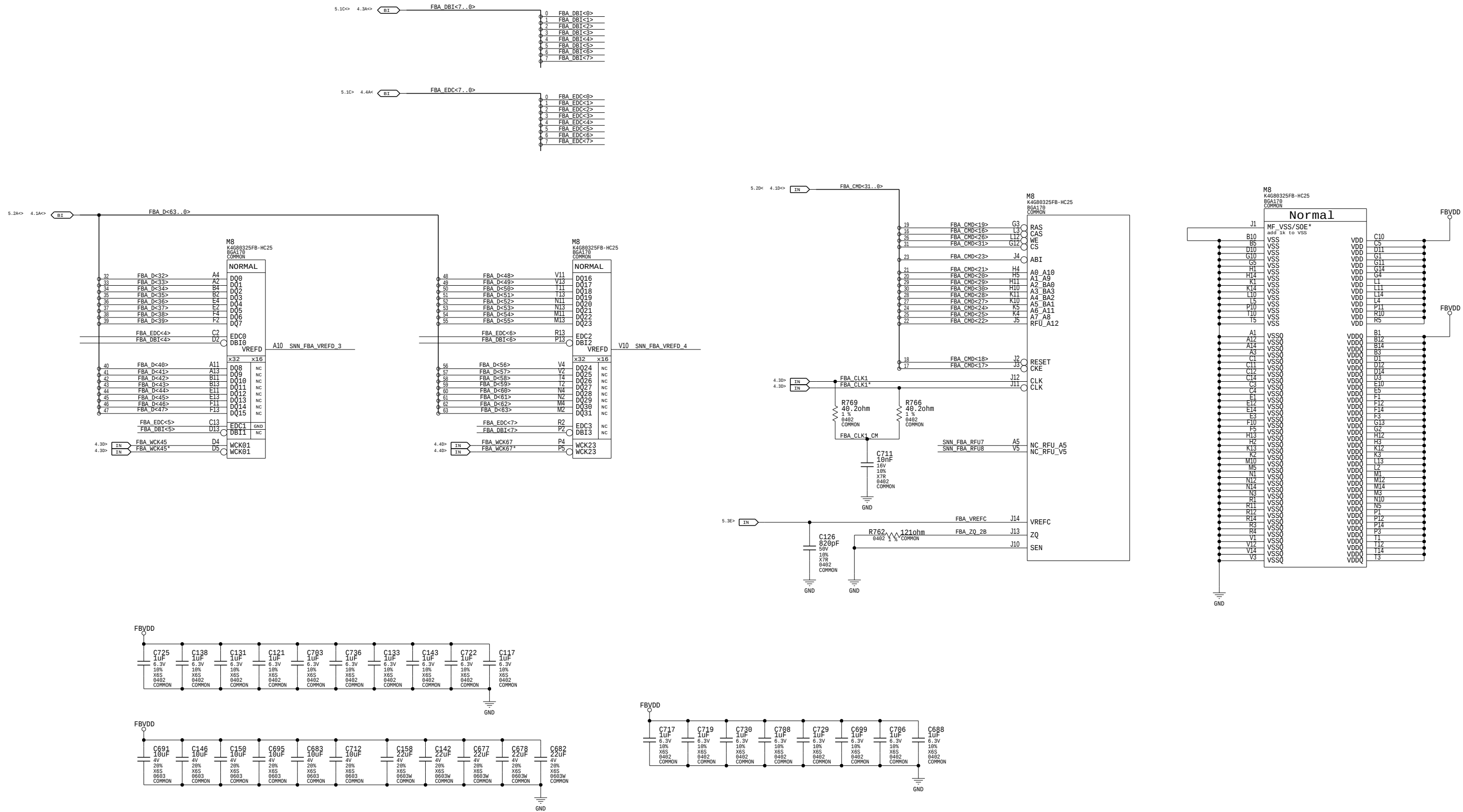
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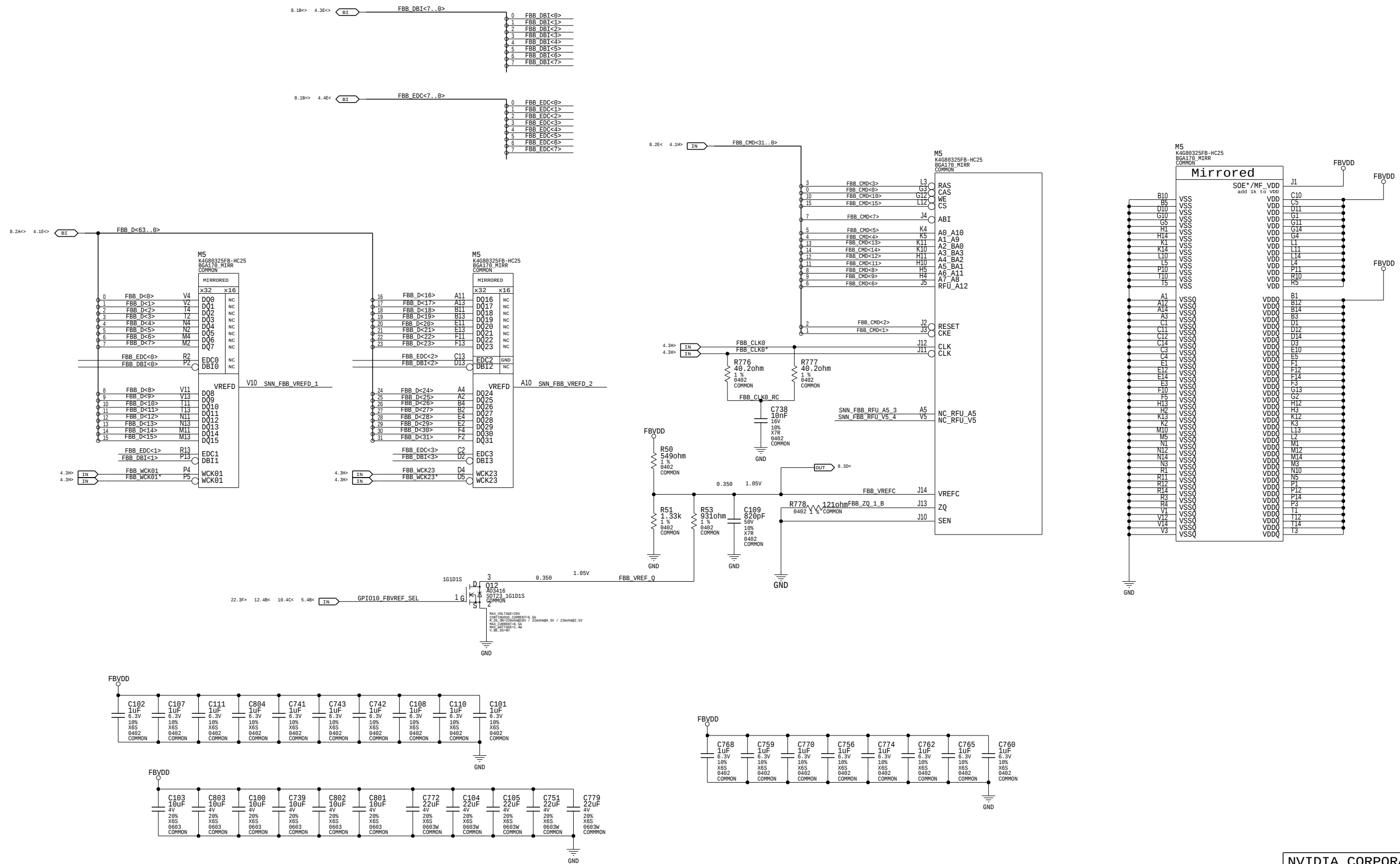
5 OF 38

DATE

30-JUN-2016



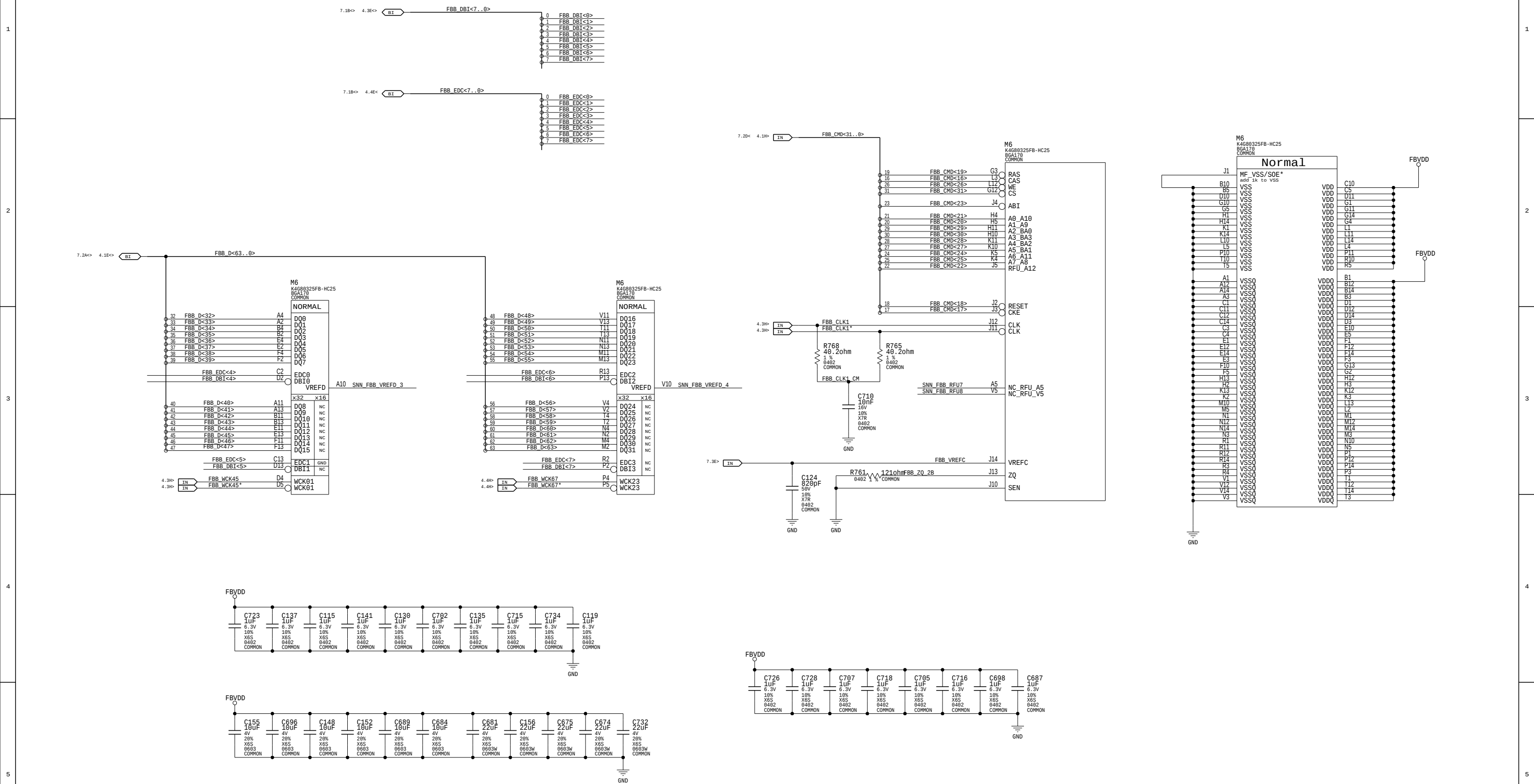
Page7: MEMORY: FBB Partition 31..0

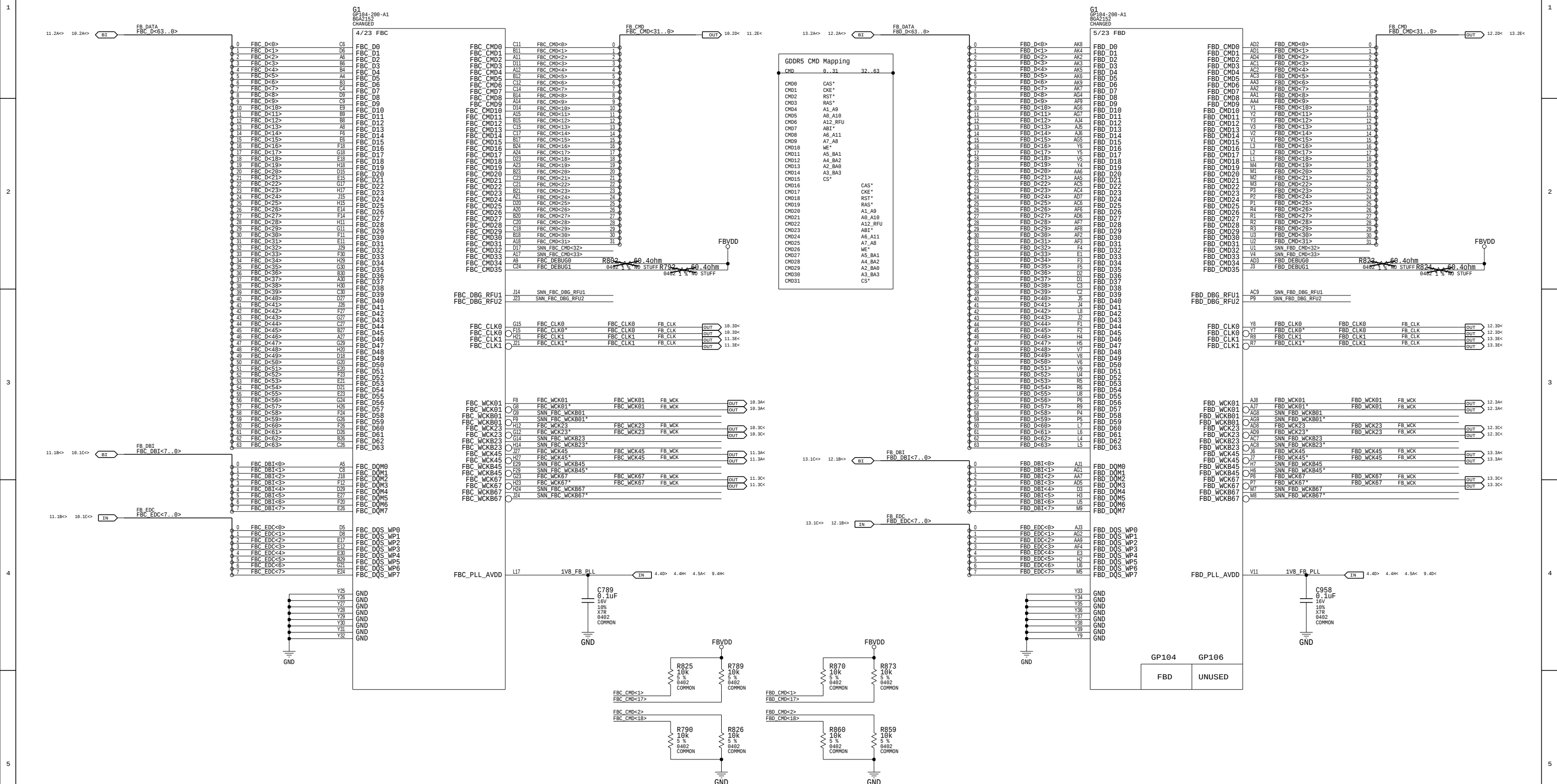


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PAGE DETAIL	MEMORY: FBB[31:0]

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PCB REV	16411-A01	PAGE	7 OF 38
BOM REV	B	DATE	30-JUN-2016





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16411-A01

PAGE

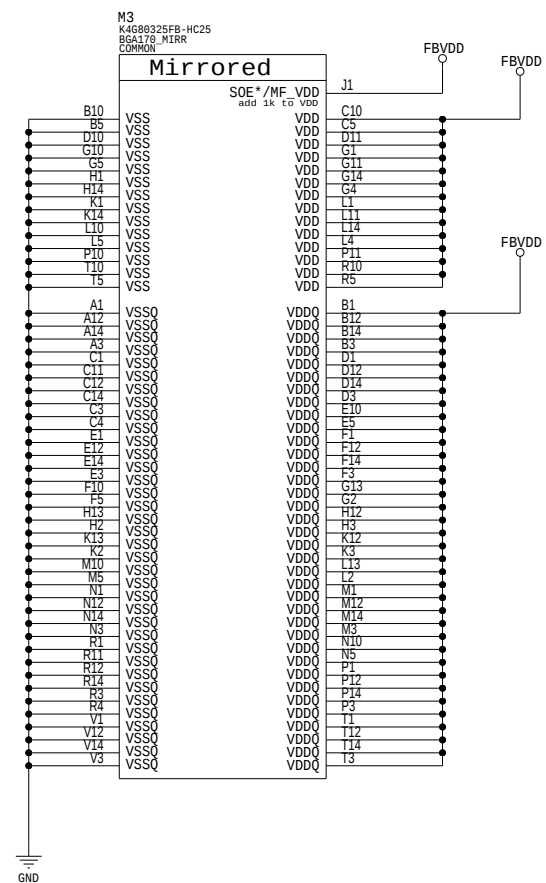
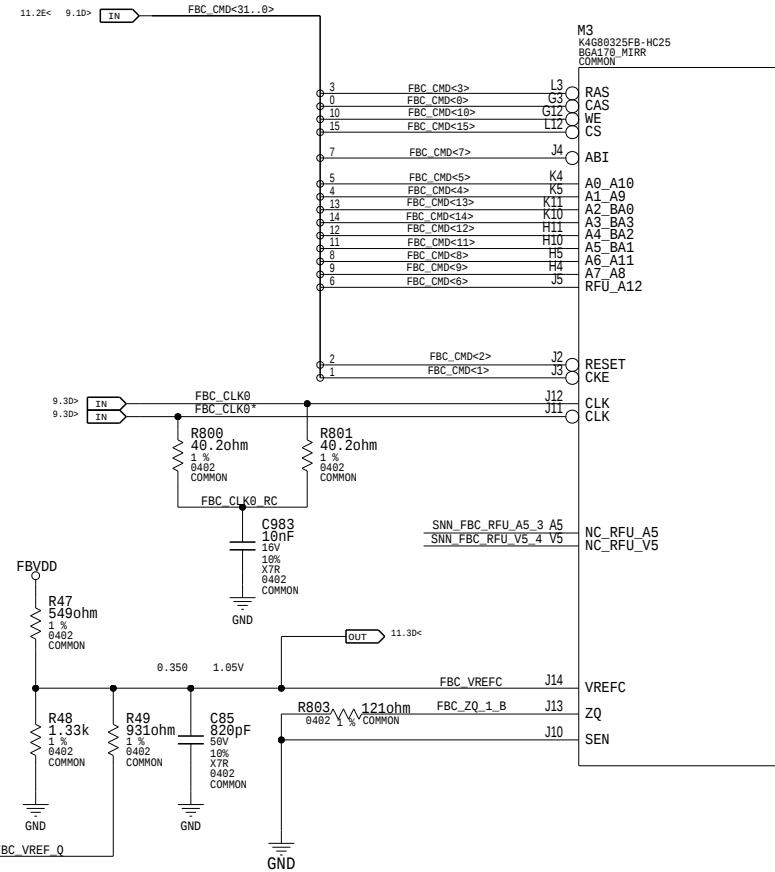
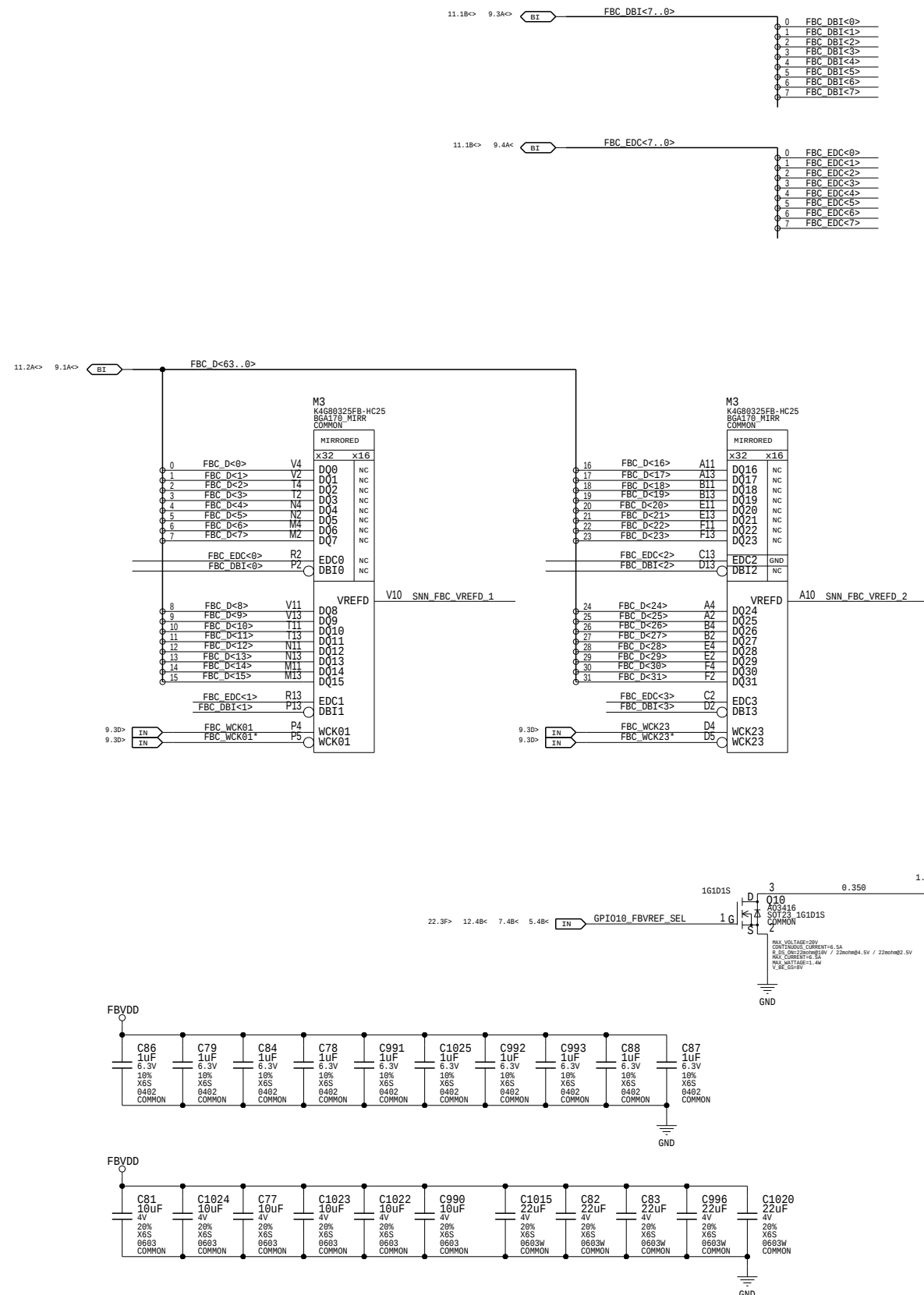
9 OF 38

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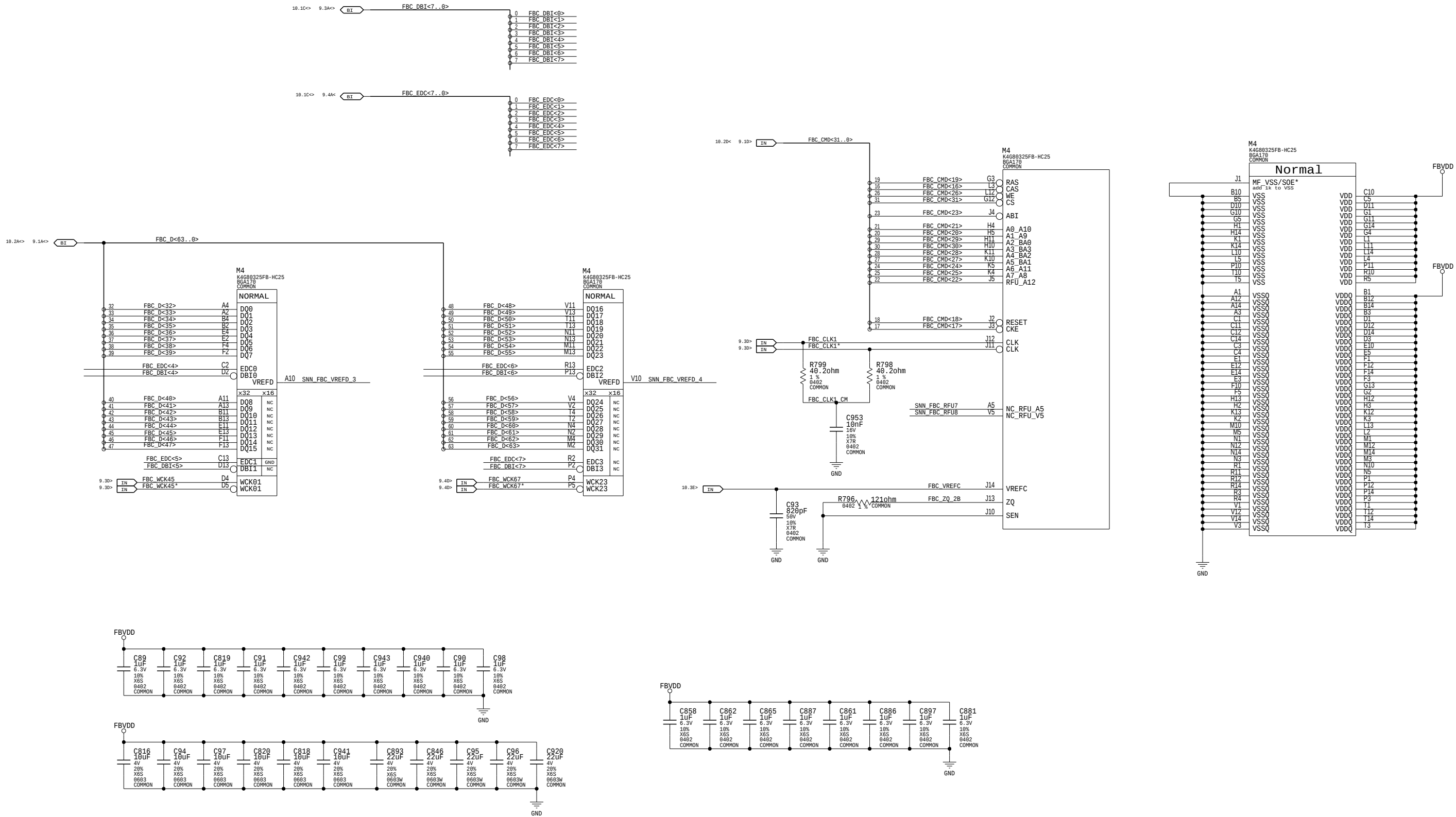
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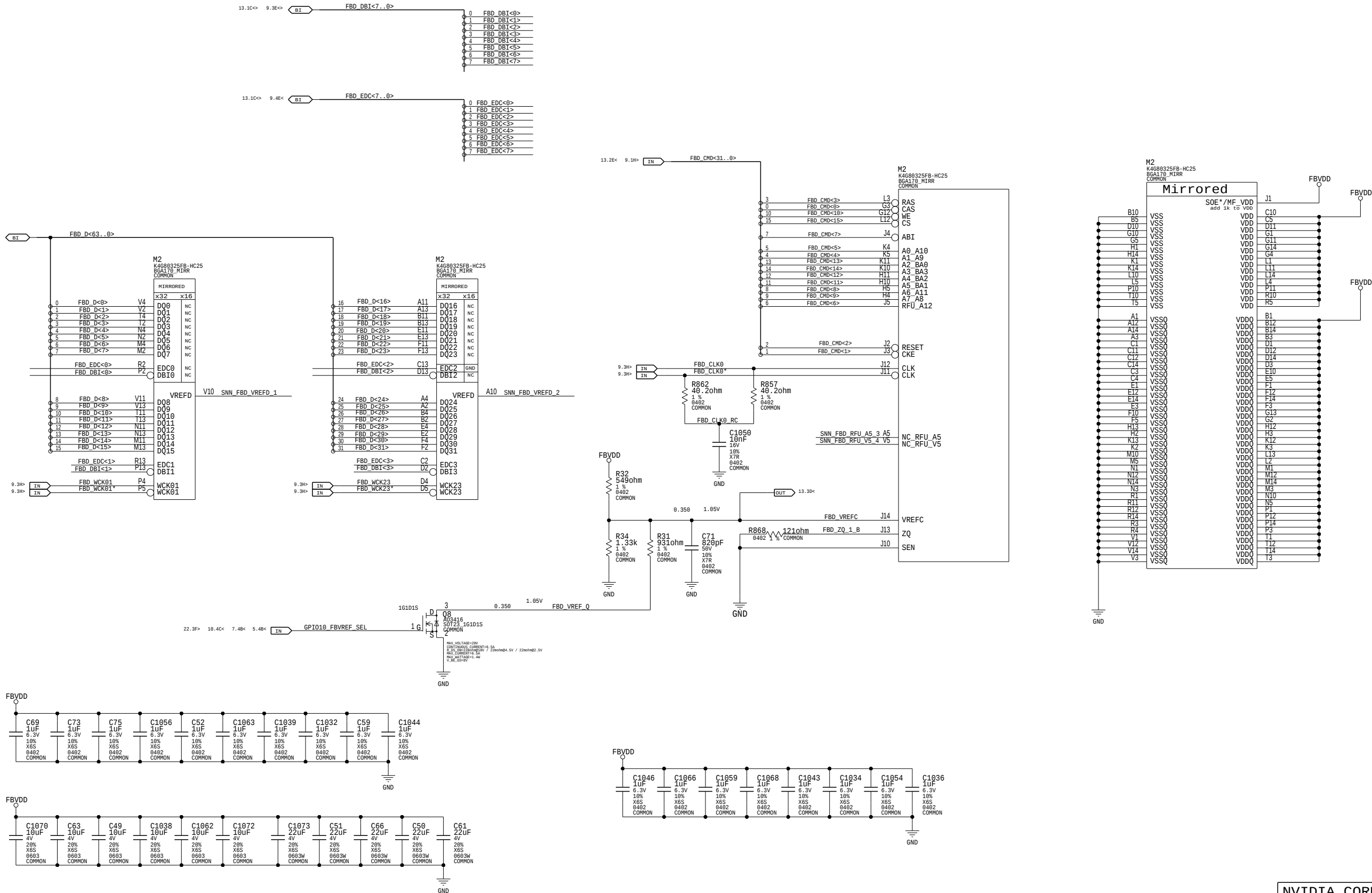
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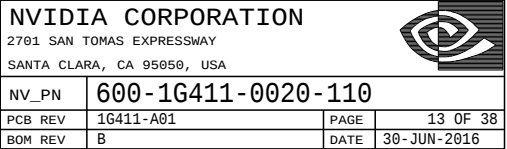
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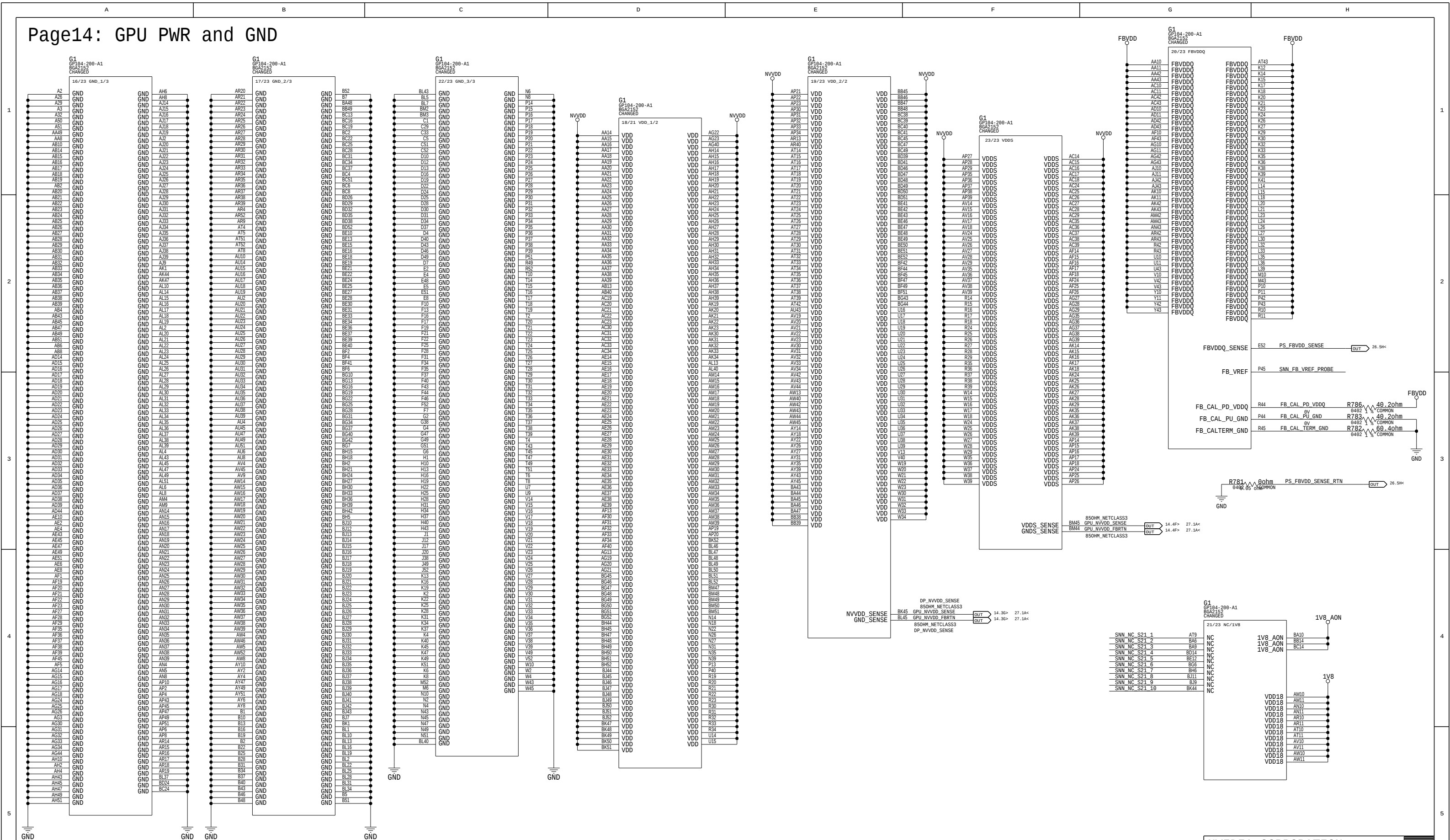
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NV_PN	600-1G411-0020-110		
PCB REV	1G411-A01	PAGE	10 OF 38
BOM REV	B	DATE	30-JUN-2016



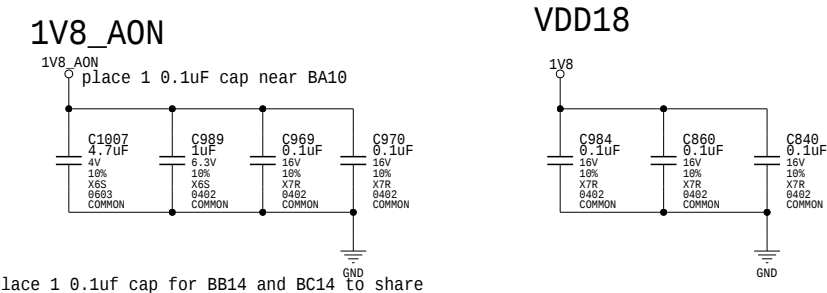
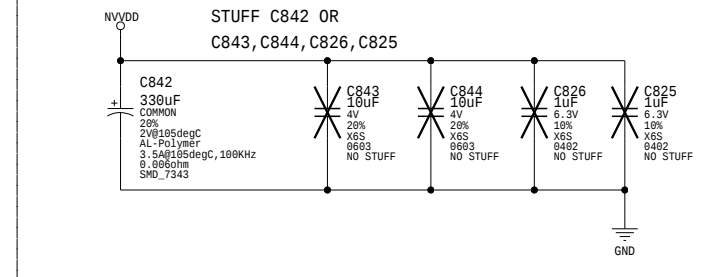
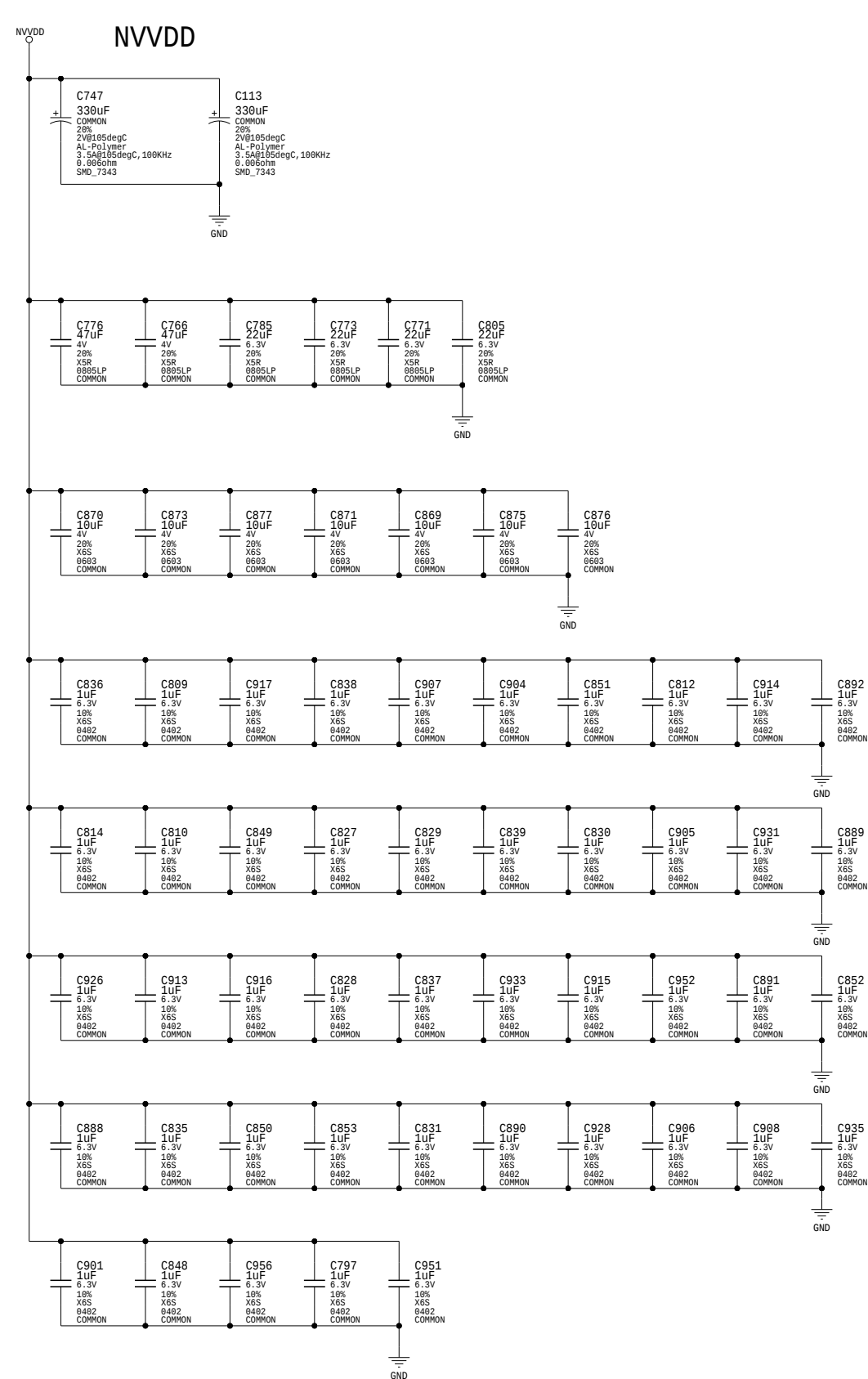




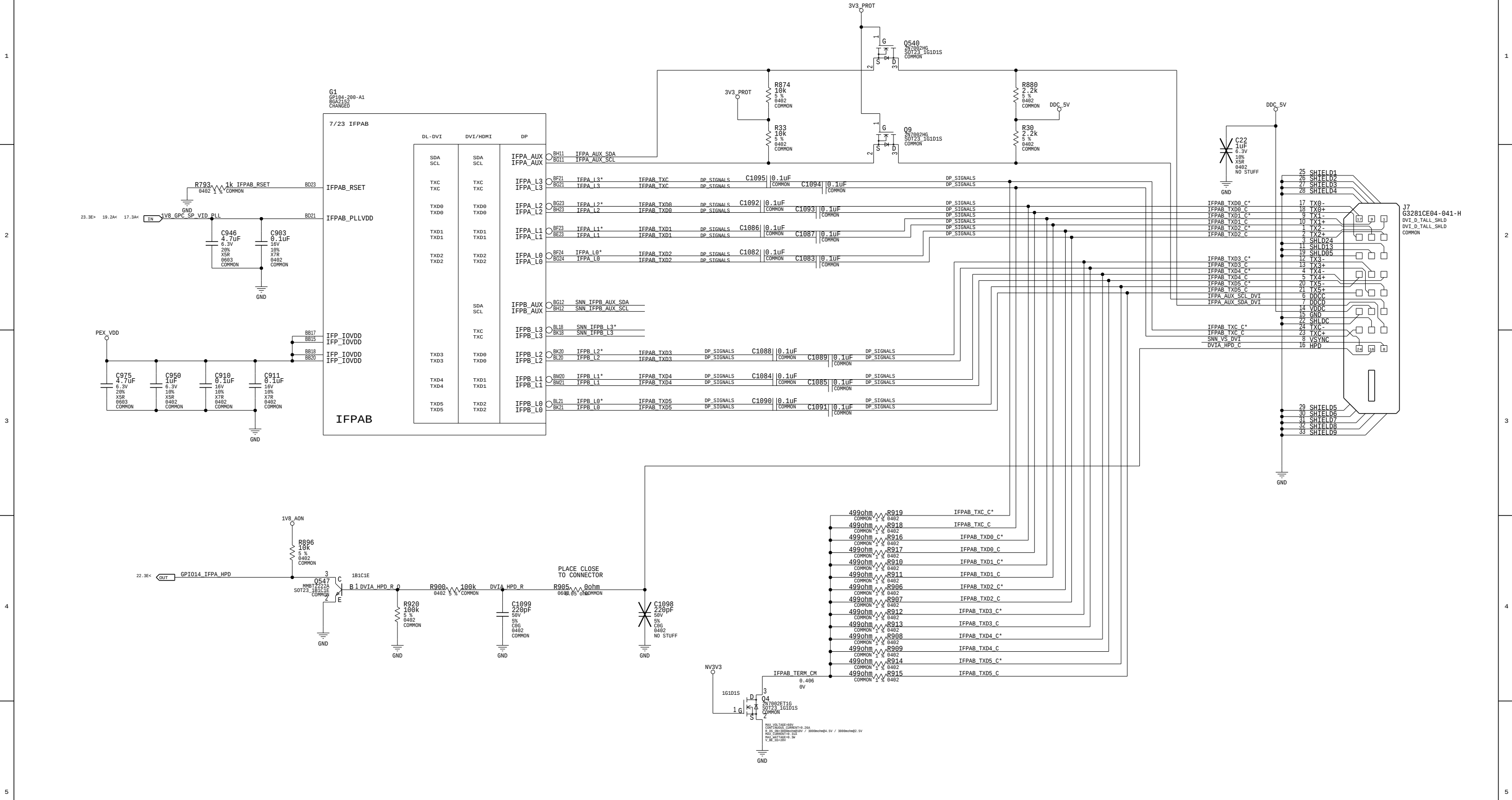
Page14: GPU PWR and GND



FBVDD



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NV_PN	600-1G411-0020-110		
PCB REV	1G411-A01	PAGE	15 OF 38
BOM REV	B	DATE	30-JUN-2016



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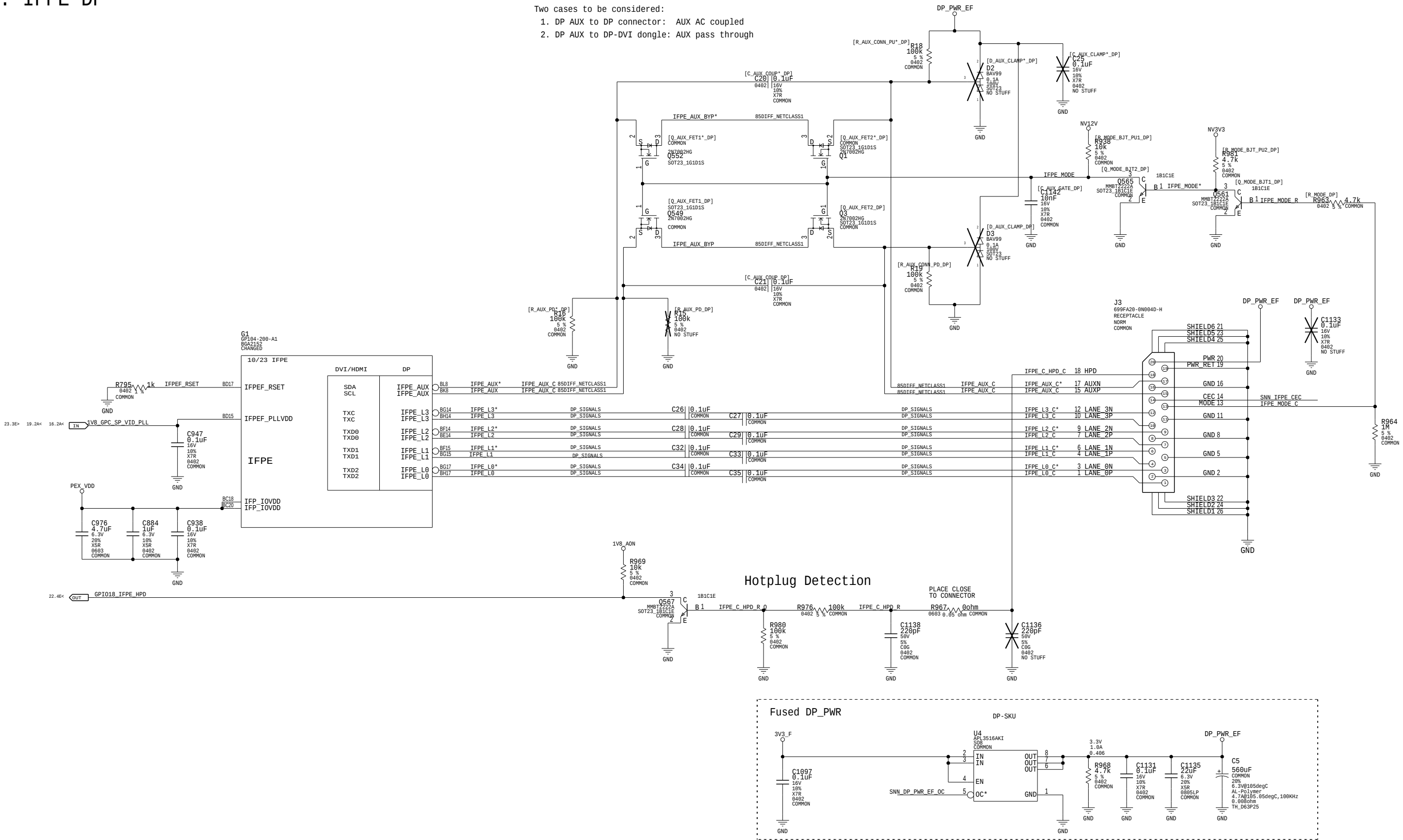
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16 OF 38

DATE

30-JUN-2016

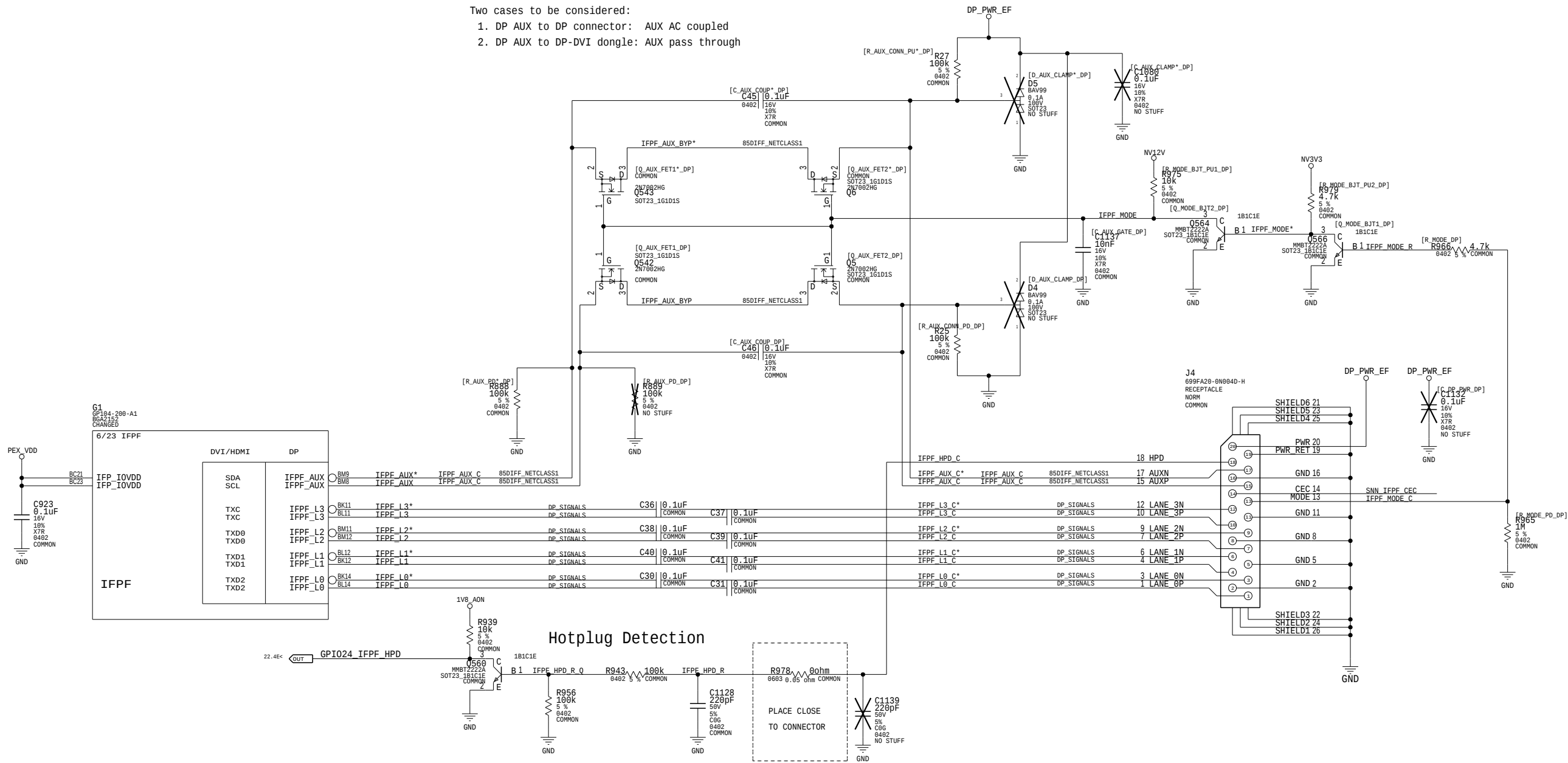
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1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through

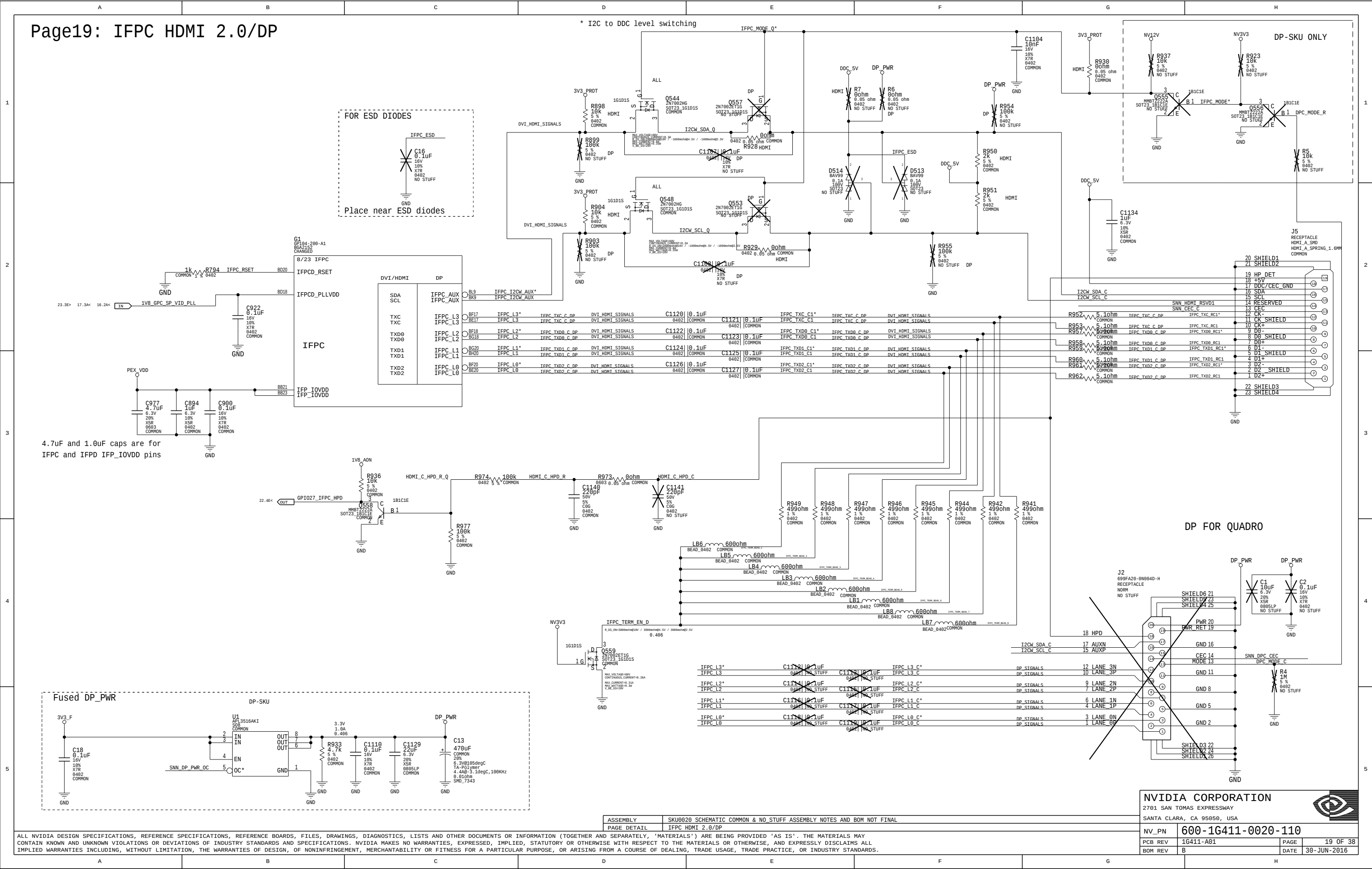


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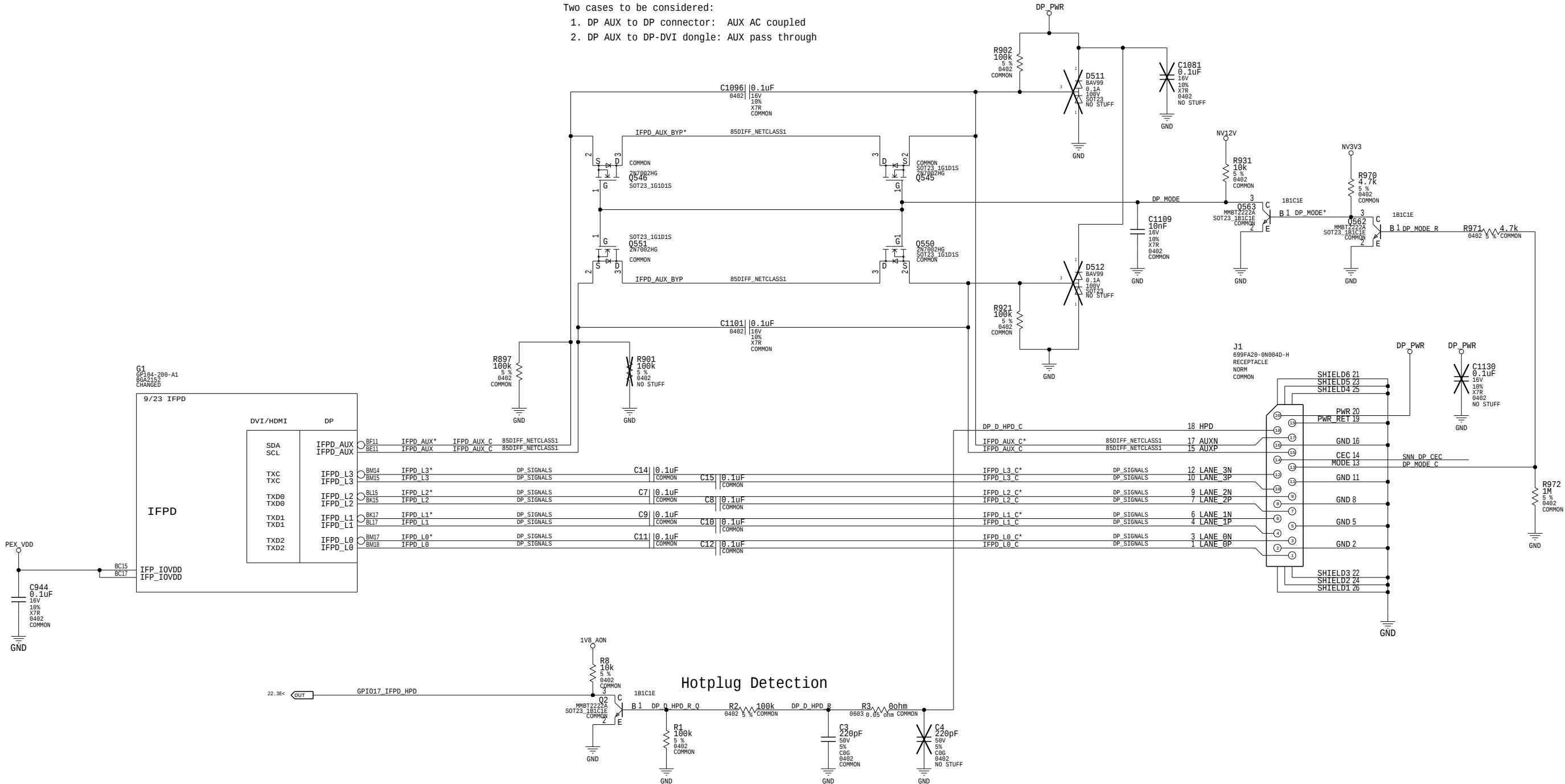
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NV_PN	600-1G411-0020-110		
PCB REV	1G411-A01	PAGE	17 OF 38
BOM REV	B	DATE	30-JUN-2016

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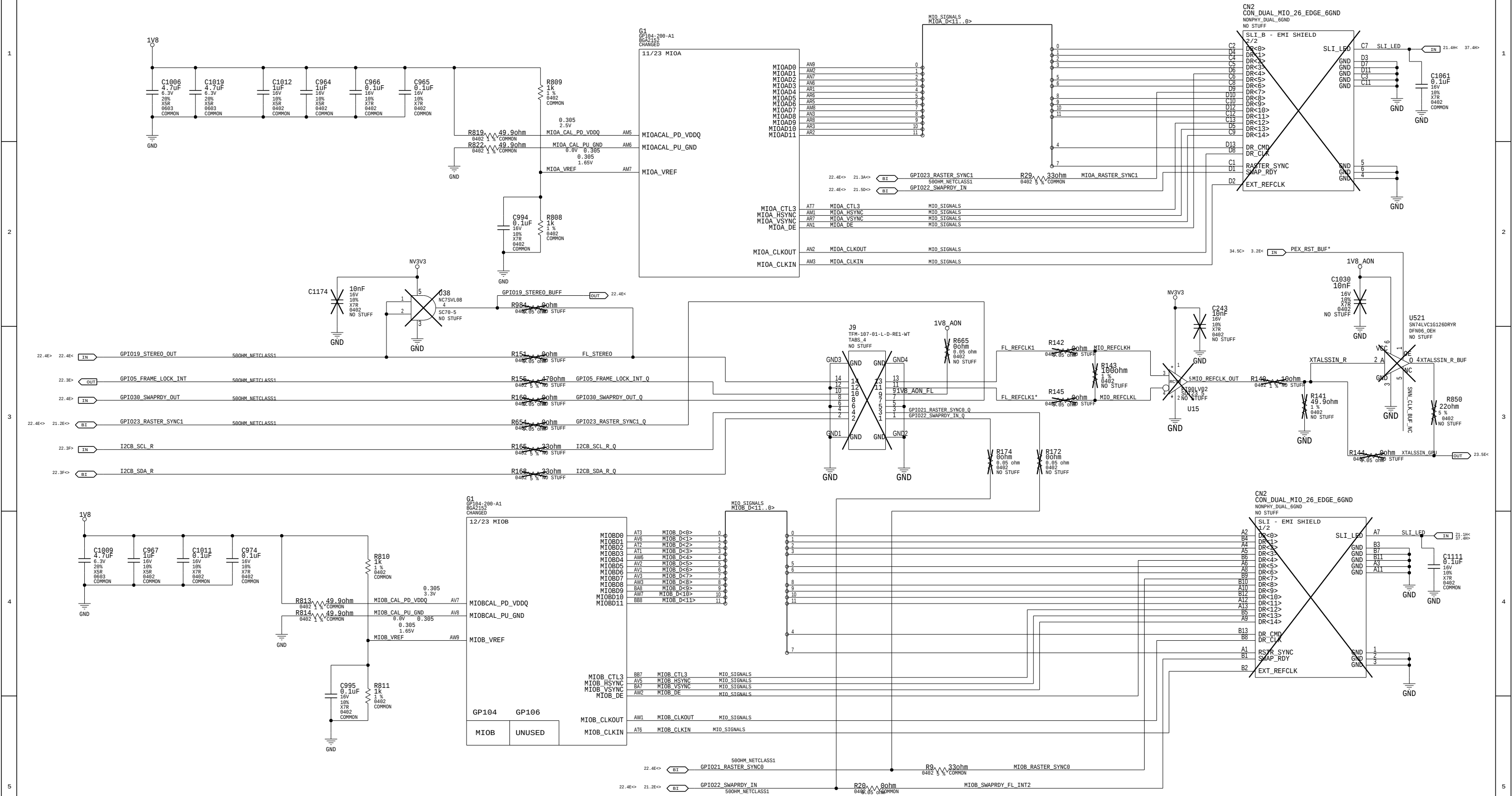


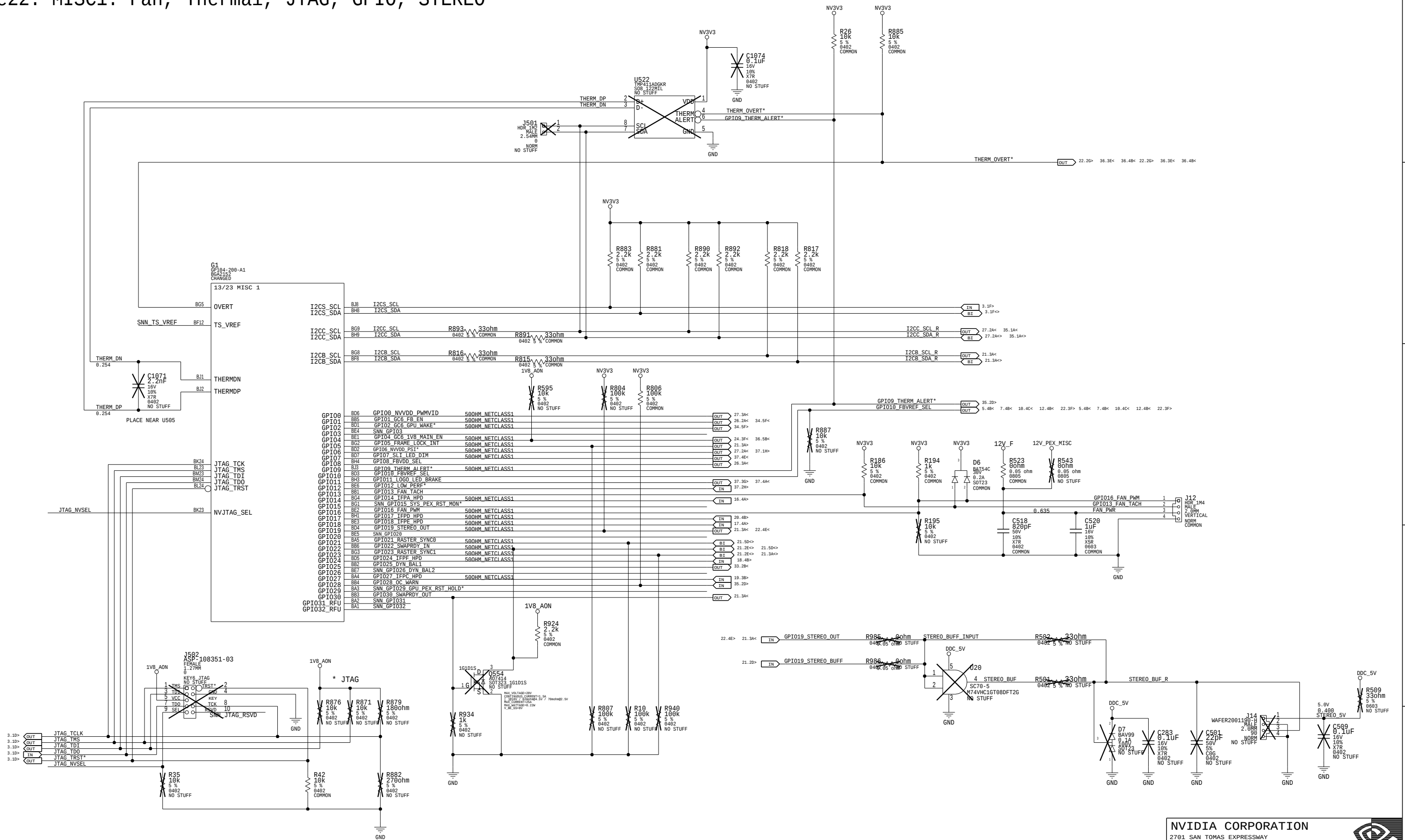


- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through



Page21: MIOA/B Interface and FRAME LOCK





Page23: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	CFG[2:0]
L	L	L	000
L	H	L	001
L	H	L	010
L	H	H	011
H	H	L	110
H	H	H	111
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0] 1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT SOR0/1/2/3 ENABLE
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

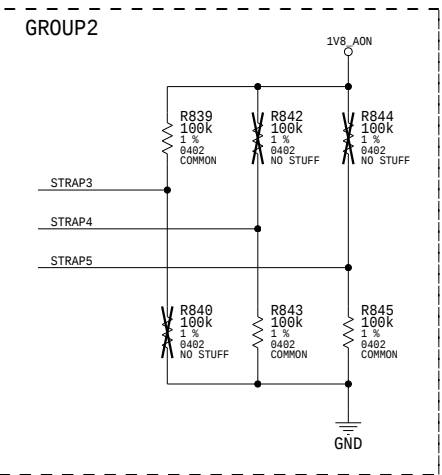
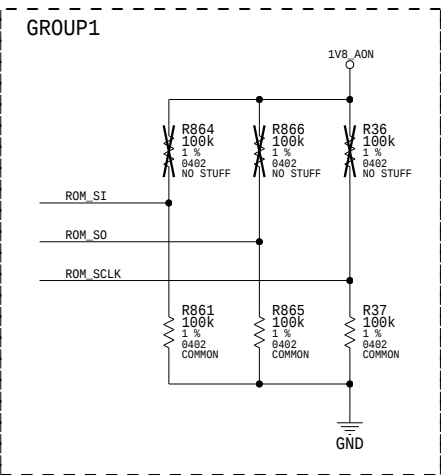
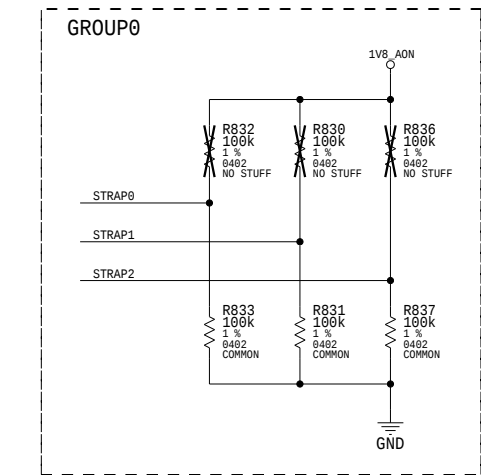
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

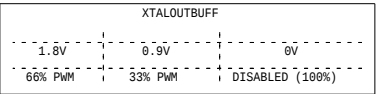
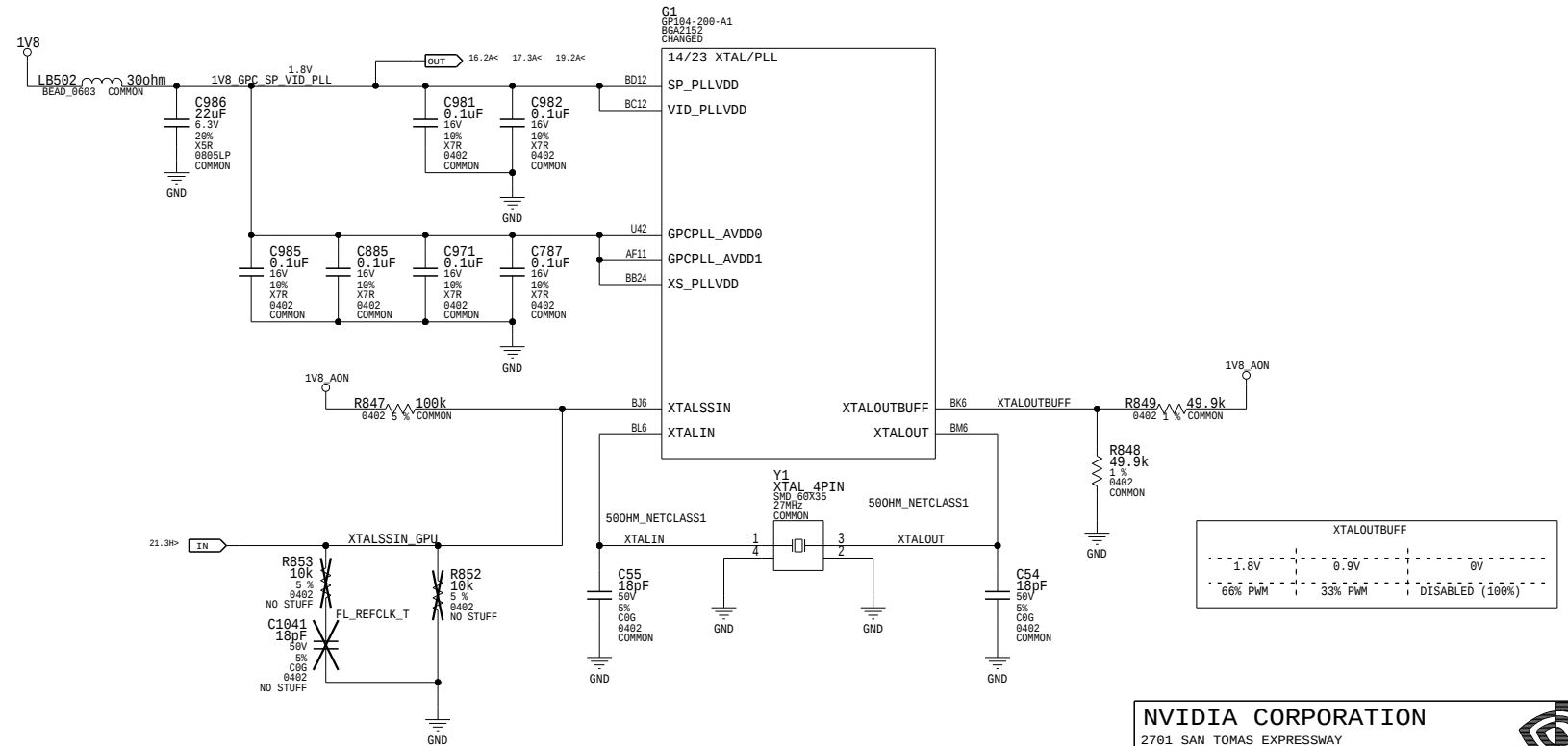
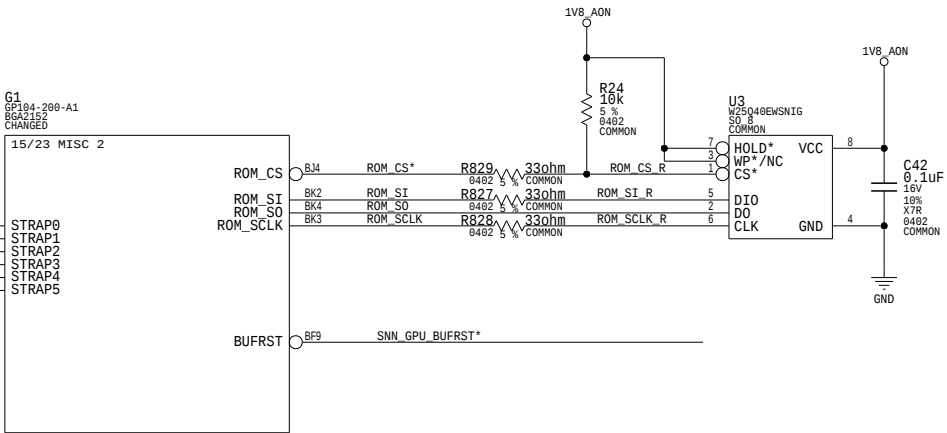
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



CFG[2:0]	Config	Width	Vendor
000	256Mx32	256-bit	Samsung
001	256Mx32	256-bit	Micron
010	256Mx32	256-bit	Hynix
011	Reserved		
100	Reserved		
101	Reserved		
110	Reserved		
111	Reserved		

STRAP0	BL3
STRAP1	BL4
STRAP2	BM4
STRAP3	BM5
STRAP4	BK5
STRAP5	BJS

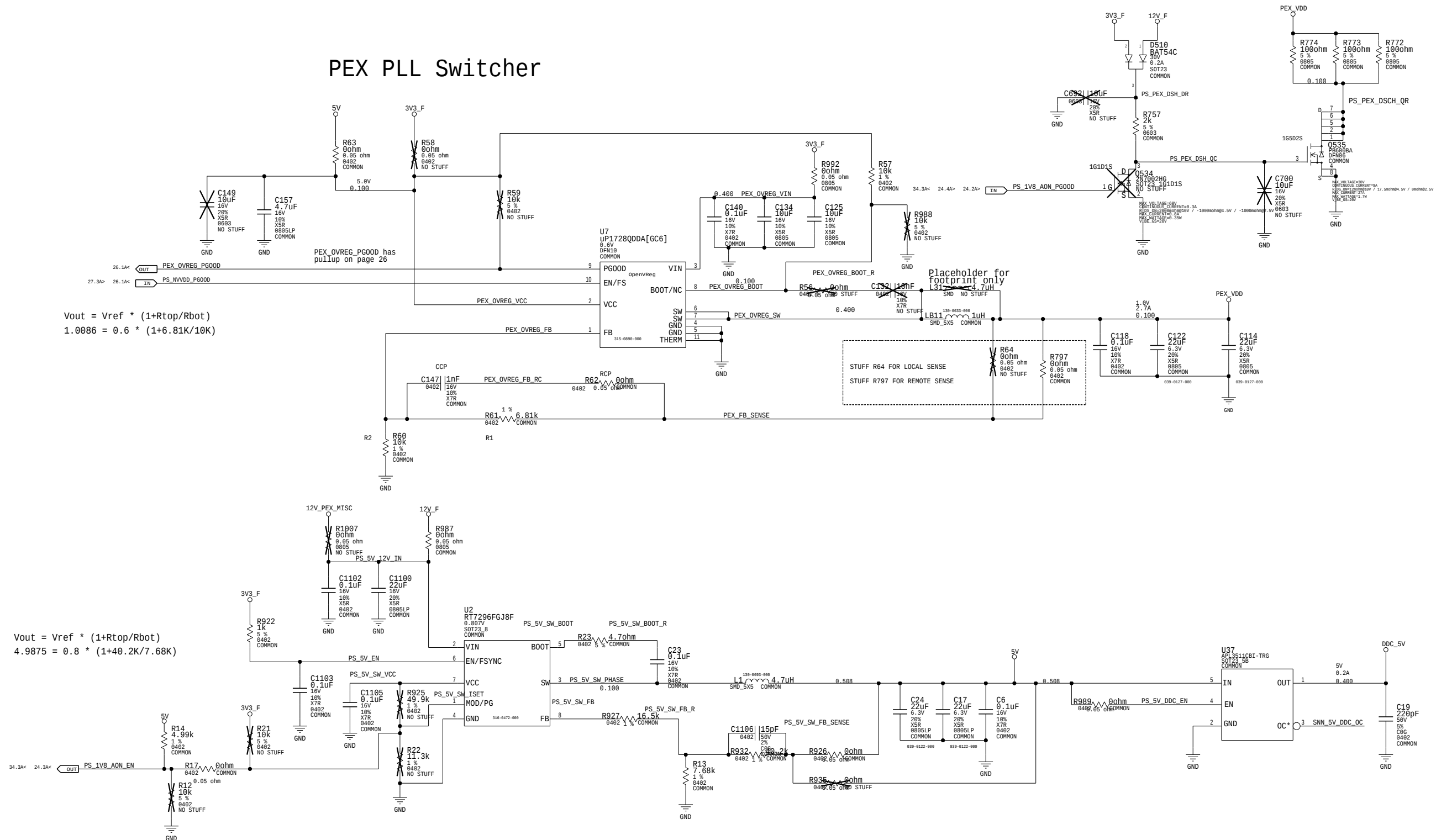




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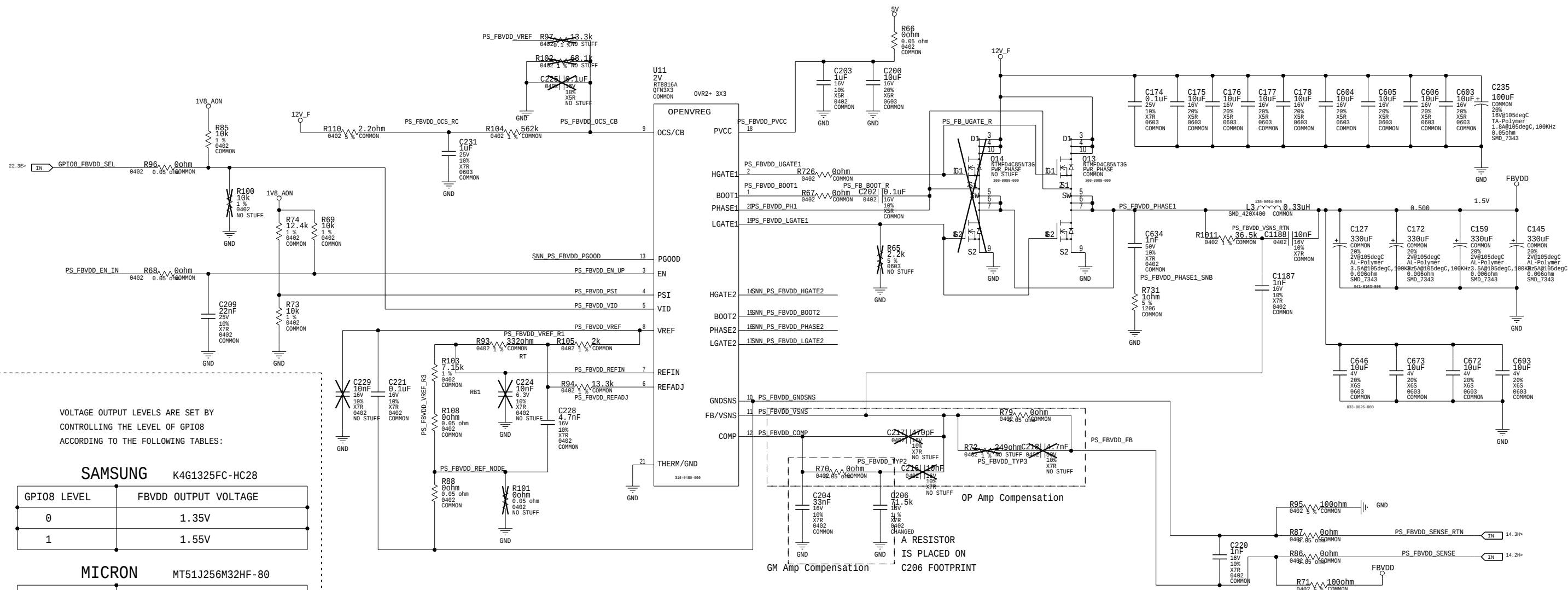
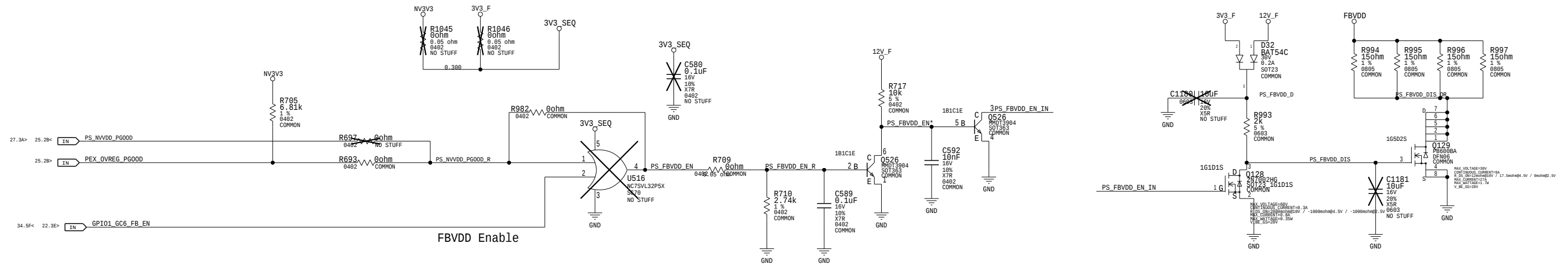
PEX PLL Switcher



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PAGE DETAIL	PS: 5V, PEX VDD

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NV_PN 600-1G411-0020-110				
PCB REV 16411-A01	PAGE 25 OF 38			
BOM REV B	DATE 30-JUN-2016			

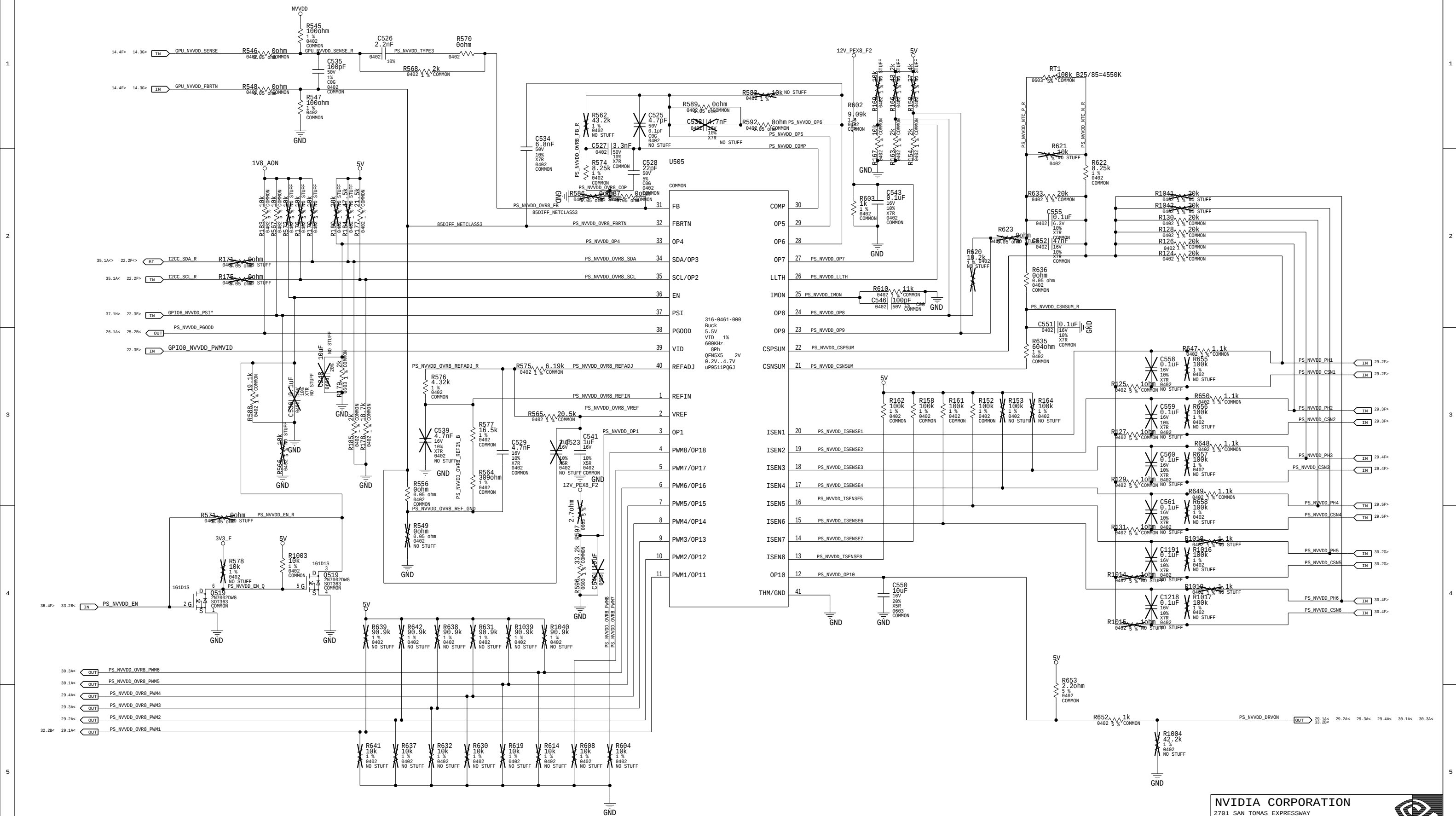


SAMSUNG		K4G1325FC-HC28
GPI08	LEVEL	FBVDD OUTPUT VOLTAGE
0		1.35V
1		1.55V

MICRON		MT51J256M32HF-80	
GPI08	LEVEL	FBVDD	OUTPUT VOLTAGE
0			1.35V
1			1.5V

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Page27: PS: NVVDD_OVR8



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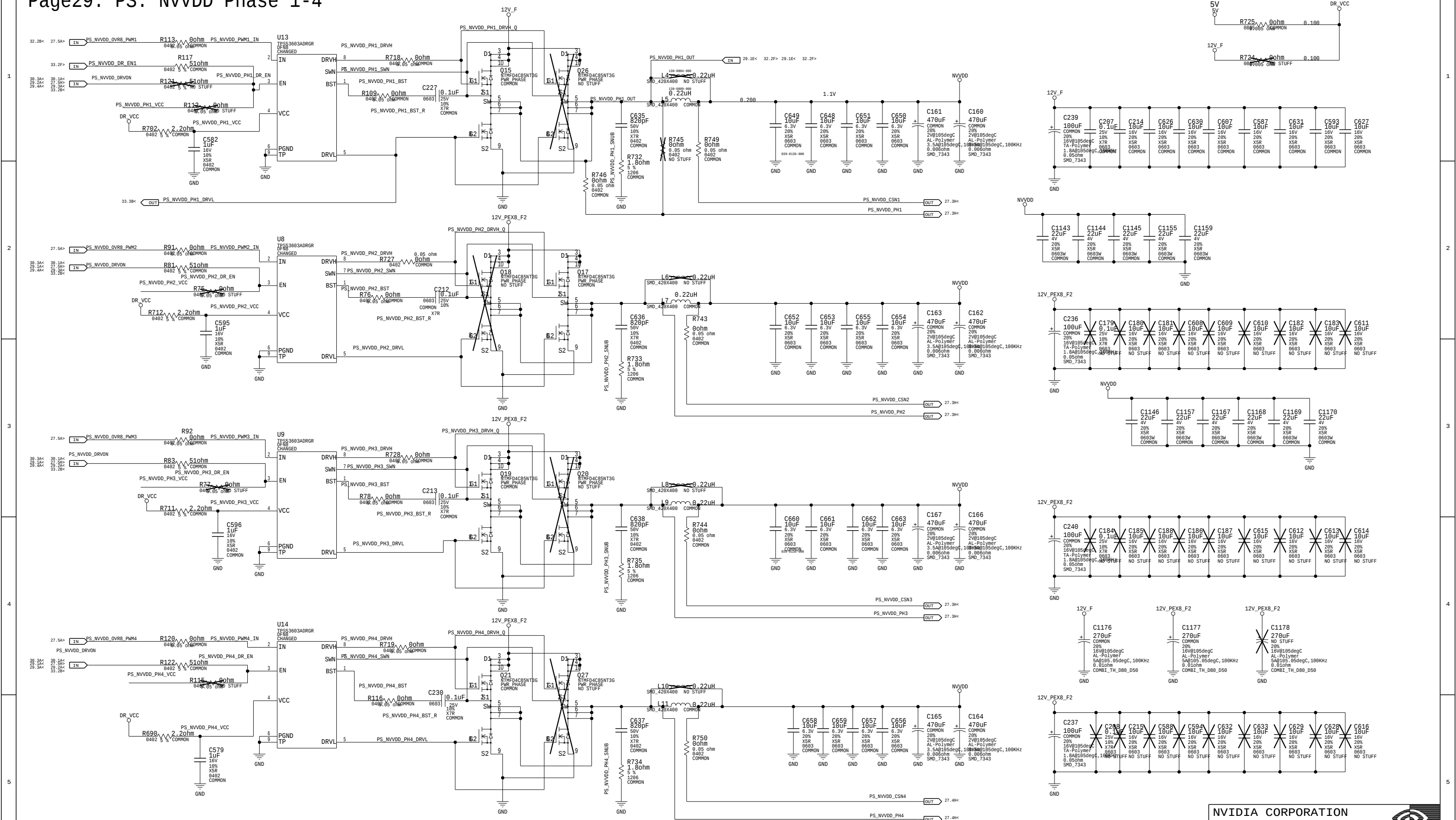
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PCB REV	1G411-A01	PAGE	27 OF 38
BOM REV	B	DATE	30-JUN-2016

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Page29: PS: NVVDD Phase 1-4

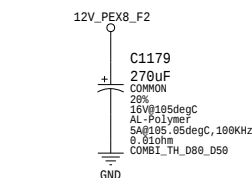
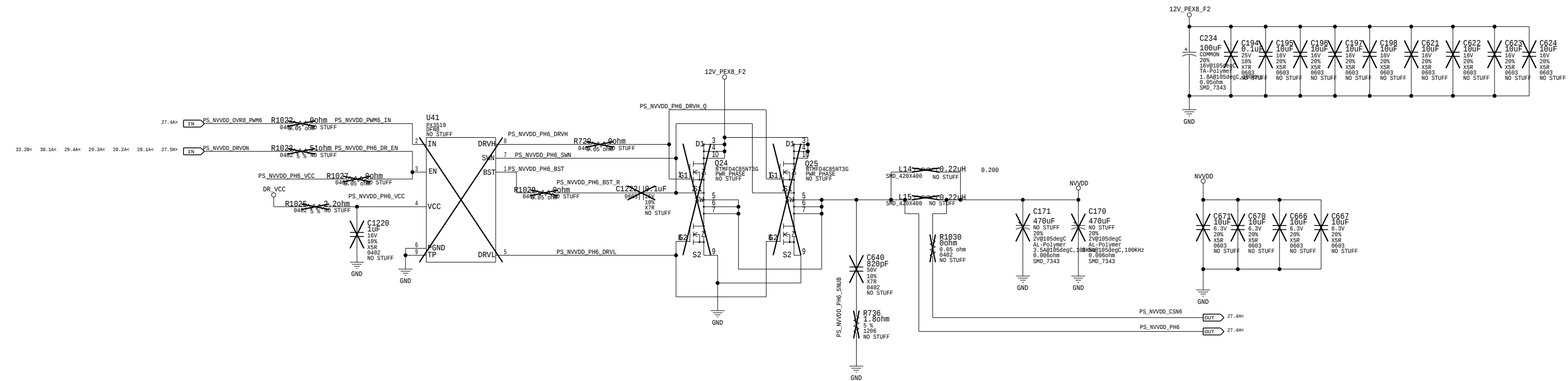
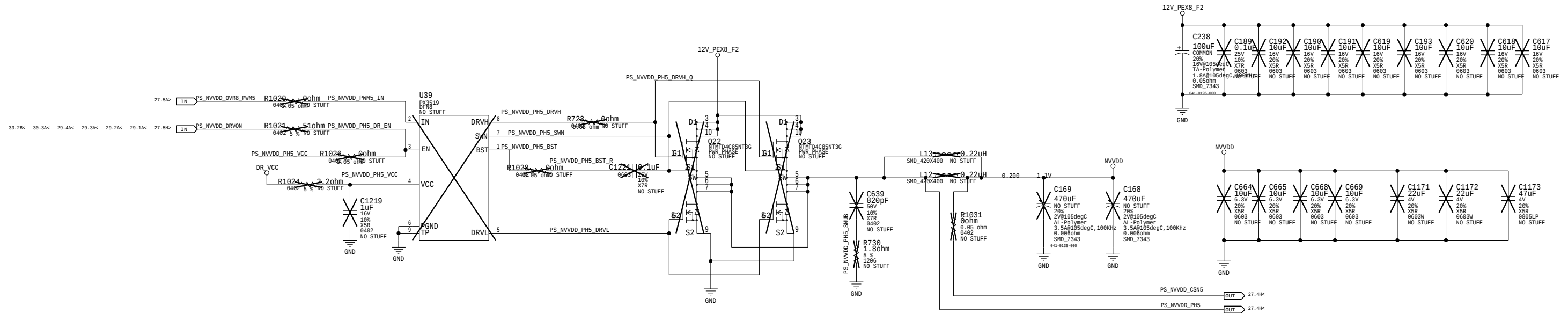


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PAGE DETAIL	PS: NWDD Phase 1-4

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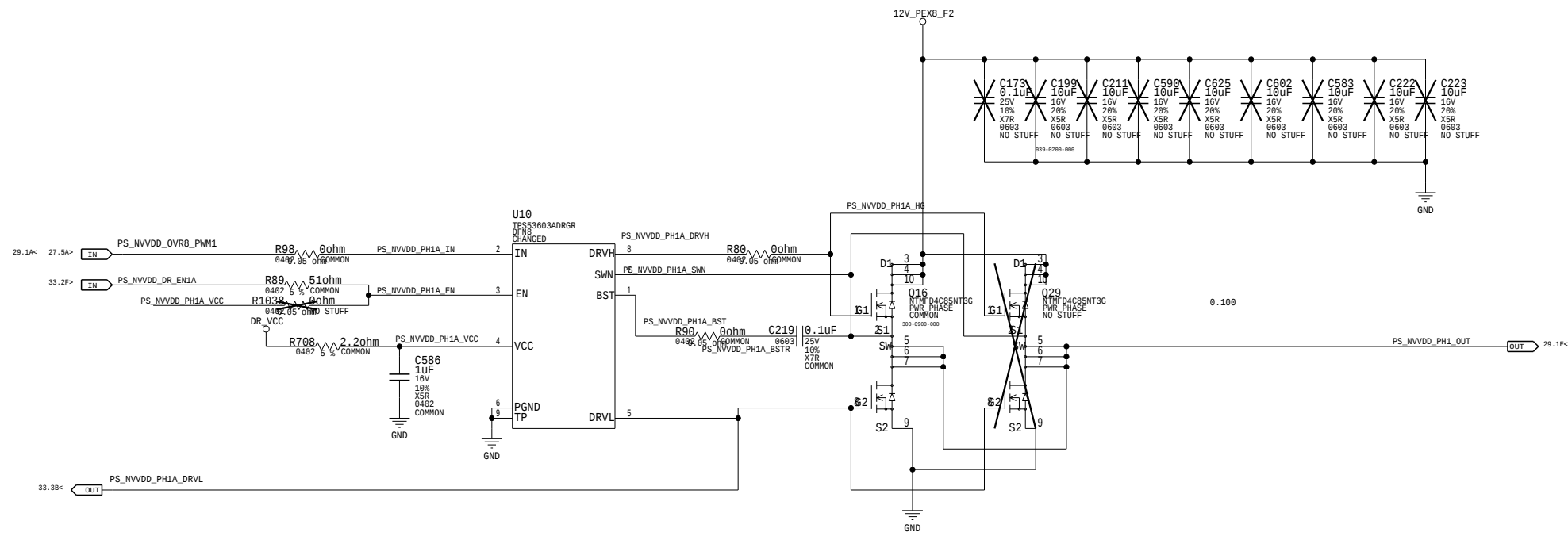
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NV_PN	600-1G411-0020-110		
PCB REV	1G411-A01	PAGE	29 OF 38
BOM REV	B	DATE	30-JUN-2016

Page30: PS: NVVDD Phase 5 & 6



NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN 600-1G411-0020-110			
PCB REV	1G411-A01	PAGE	30 OF 38
BOM REV	B	DATE	30-JUN-2016

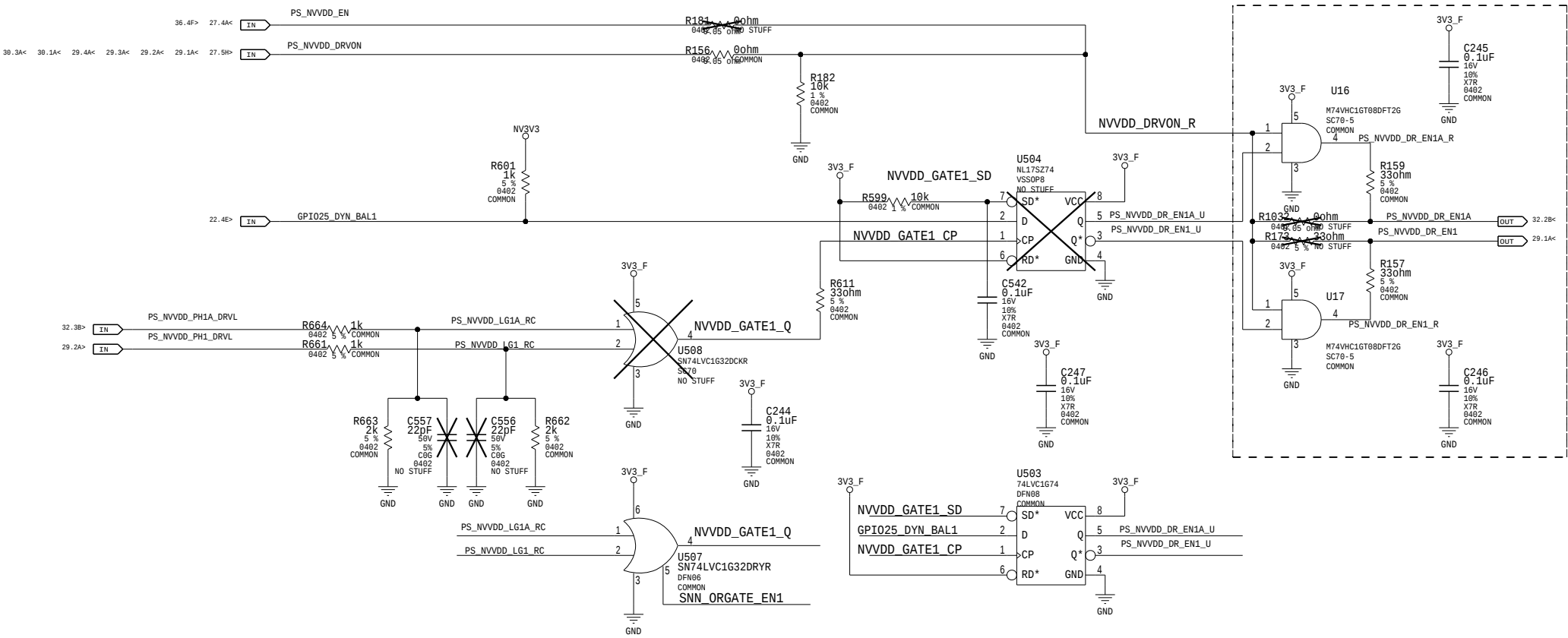
Page32: PS: Dynamic Power Balance Phases

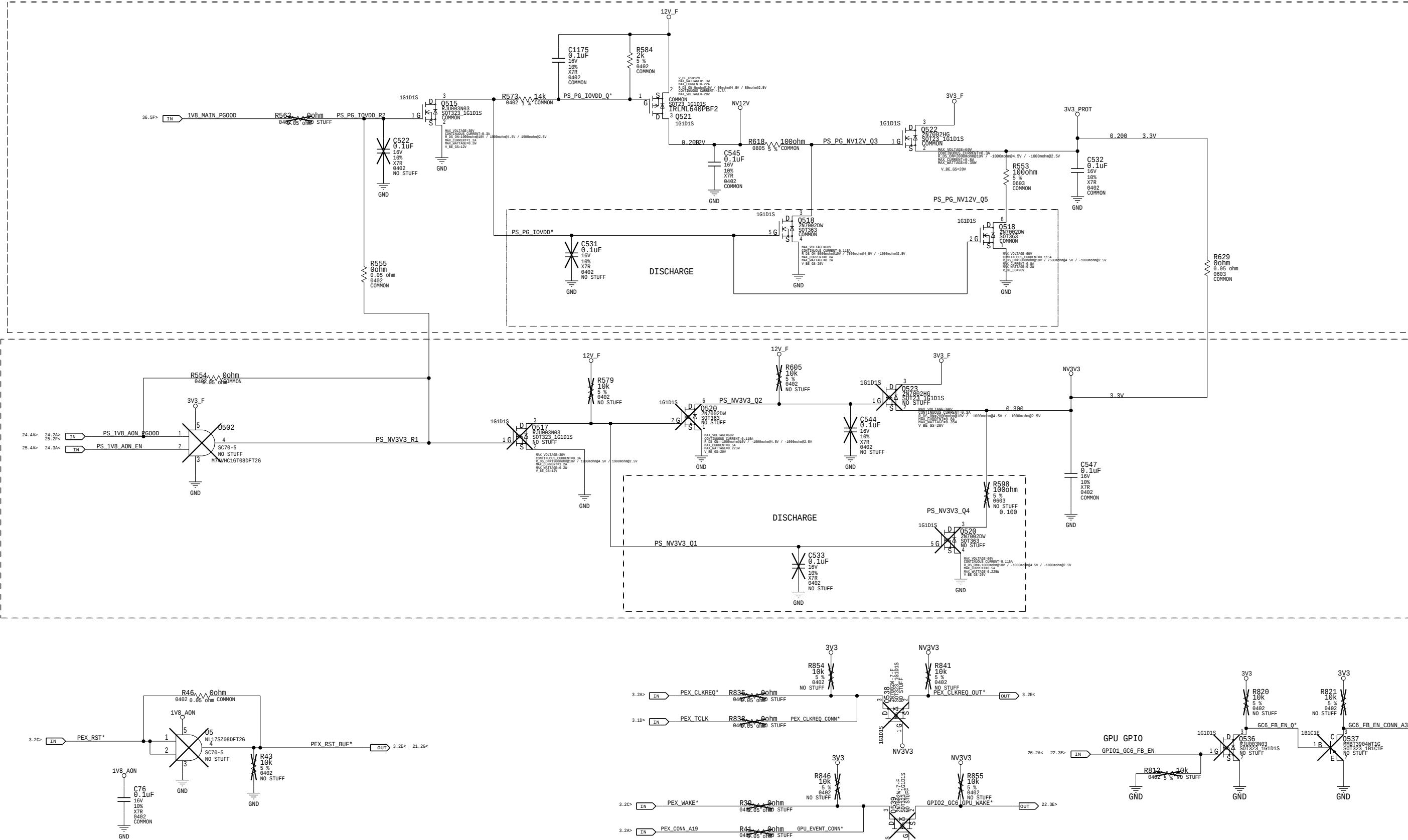


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NV_PN	600-1G411-0020-110		
PCB REV	1G411-A01	PAGE	32 OF 38
BOM REV	B	DATE	30-JUN-2016

Page33: PS: Dynamic Power Balance Logic

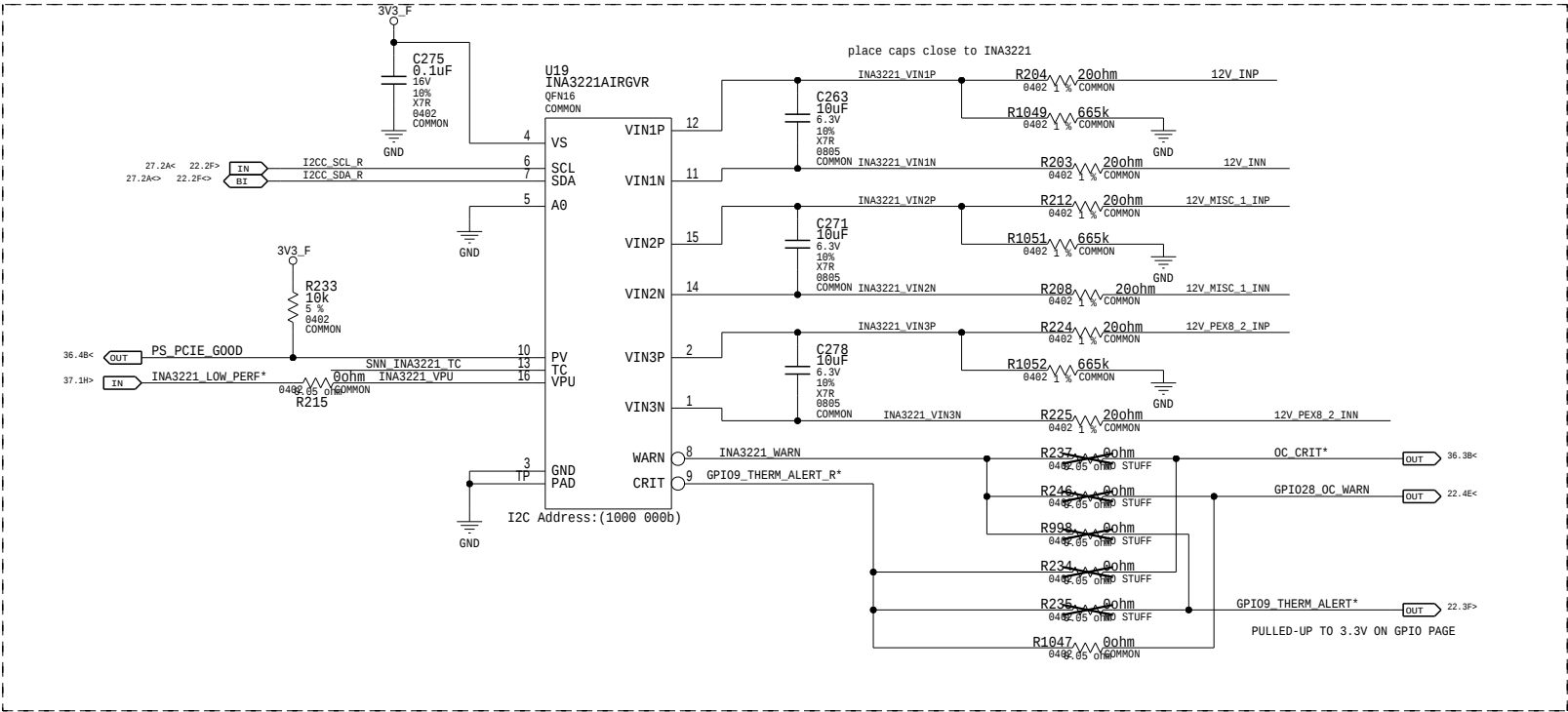




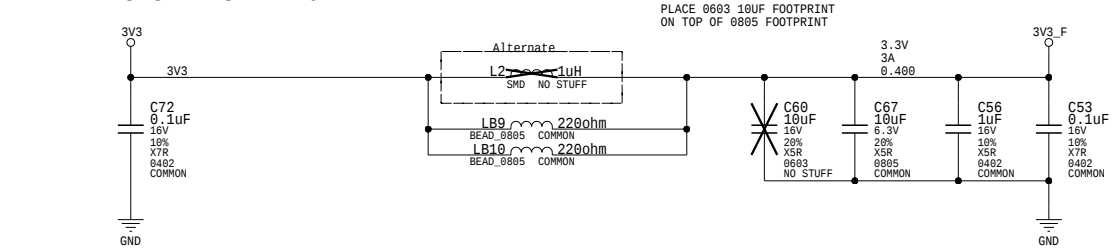
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NV_PN	600-10411-0020-110		
PCB REV	10411-A01	PAGE	34 OF 38
BOM REV	B	DATE	30-JUN-2016

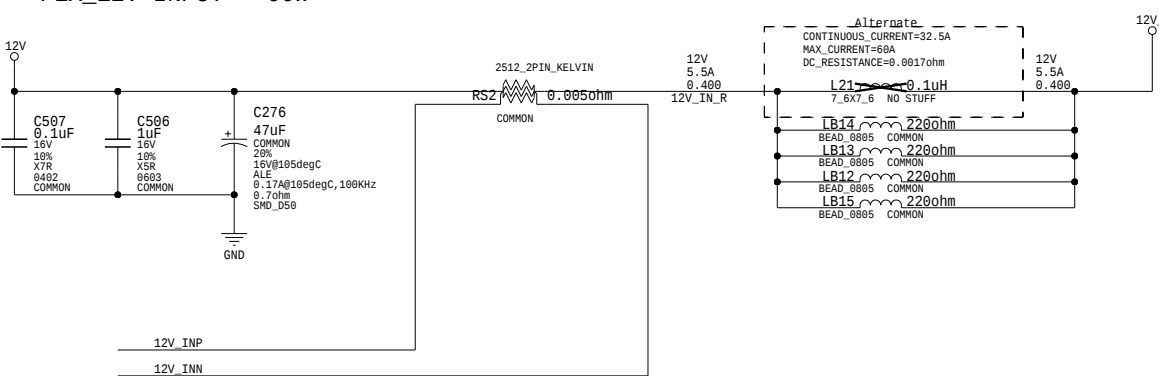
Page35: PS: Inputs, Filtering, and Monitoring



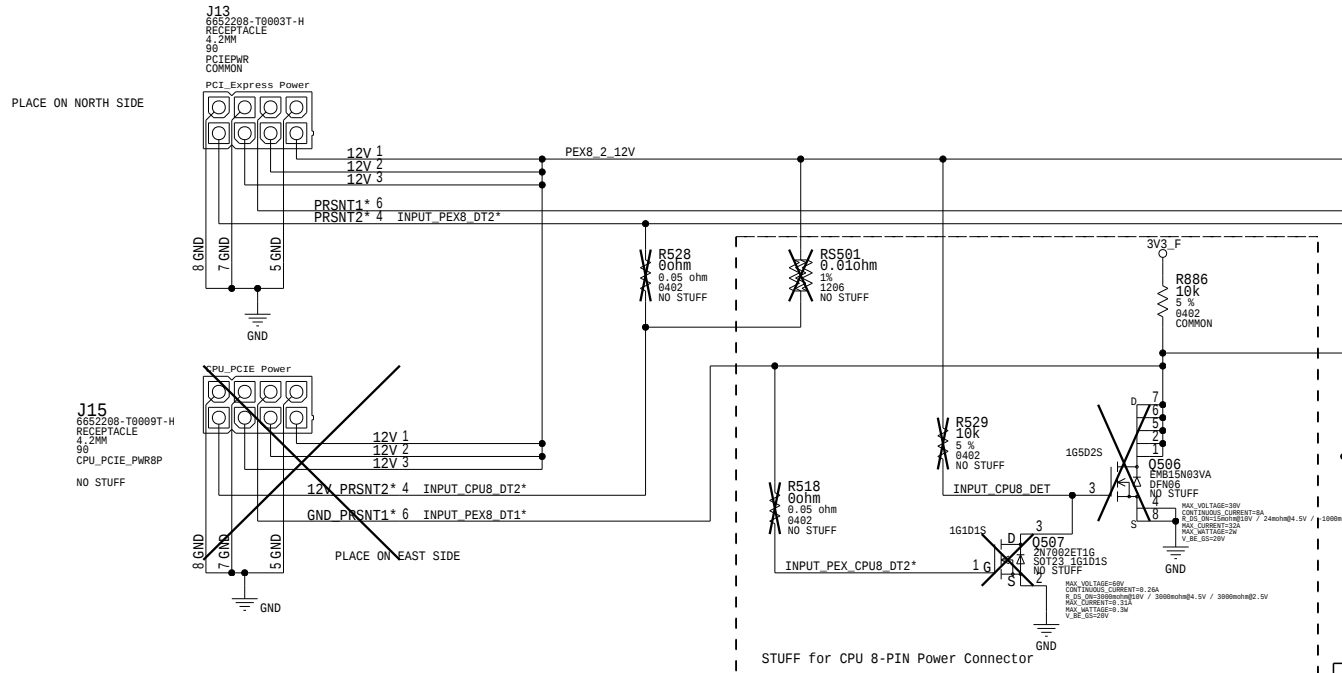
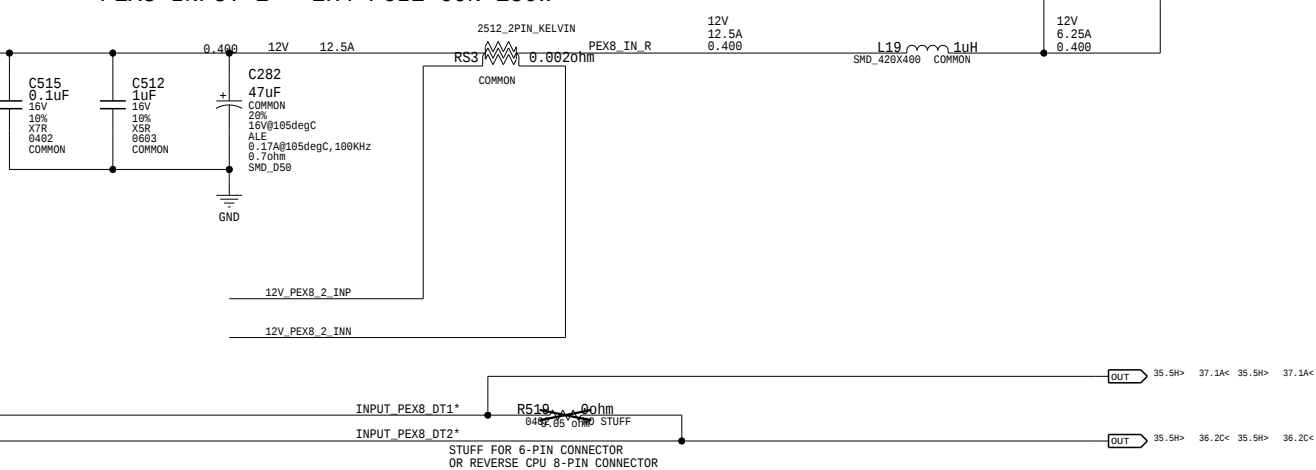
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



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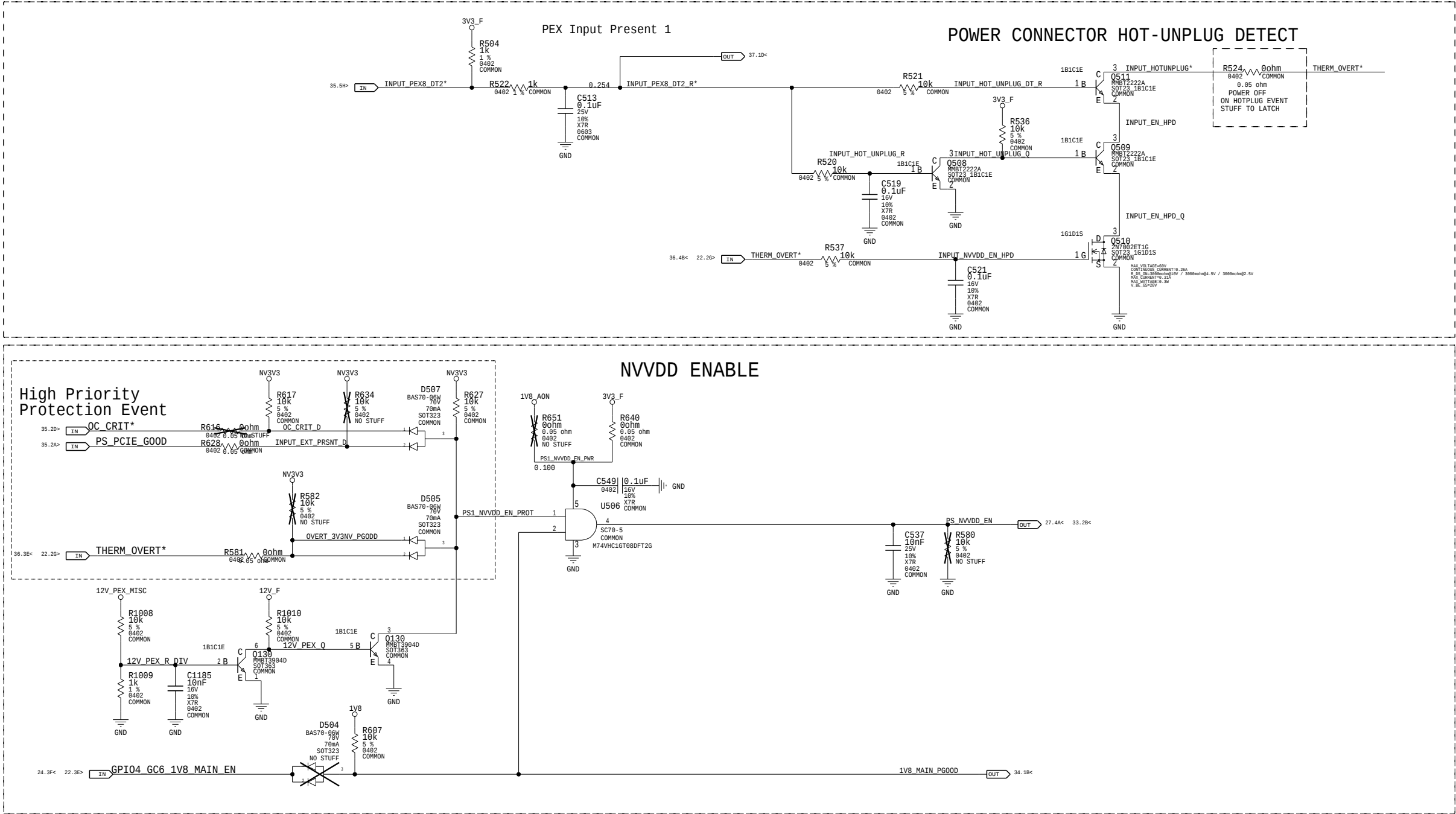
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PCB REV 16411-A01

BOM REV B

PAGE 35 OF 38

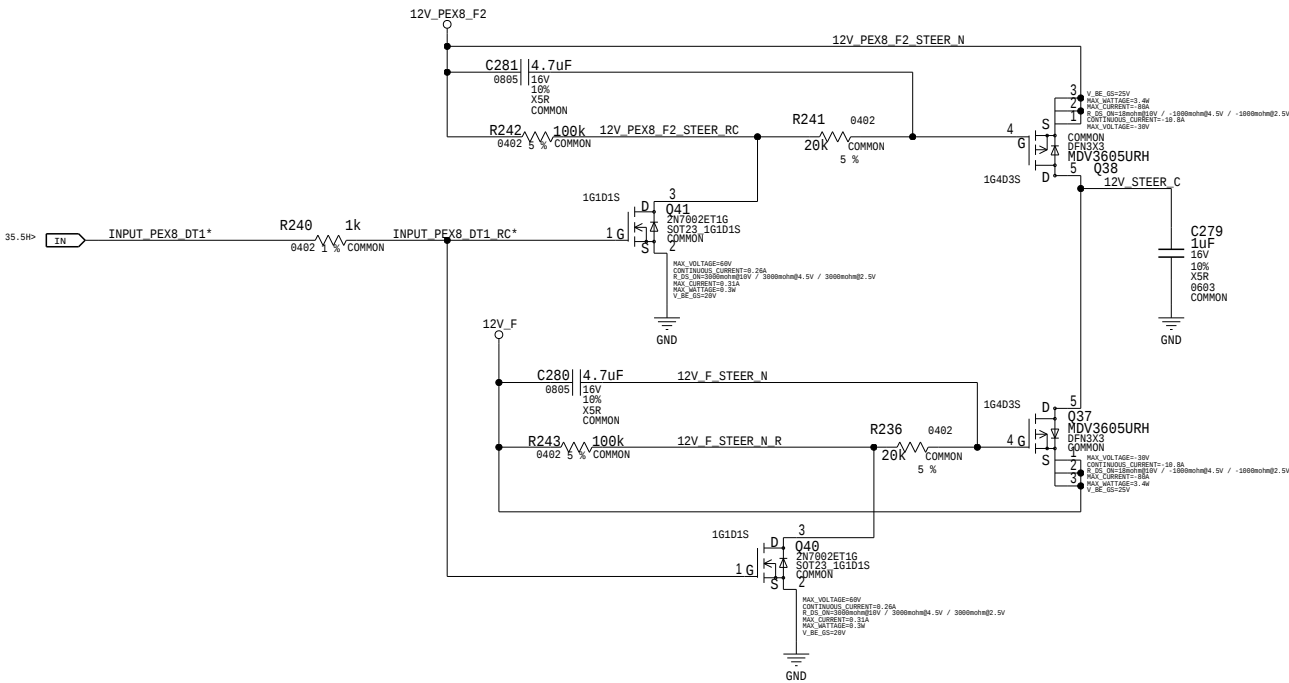
DATE 30-JUN-2016



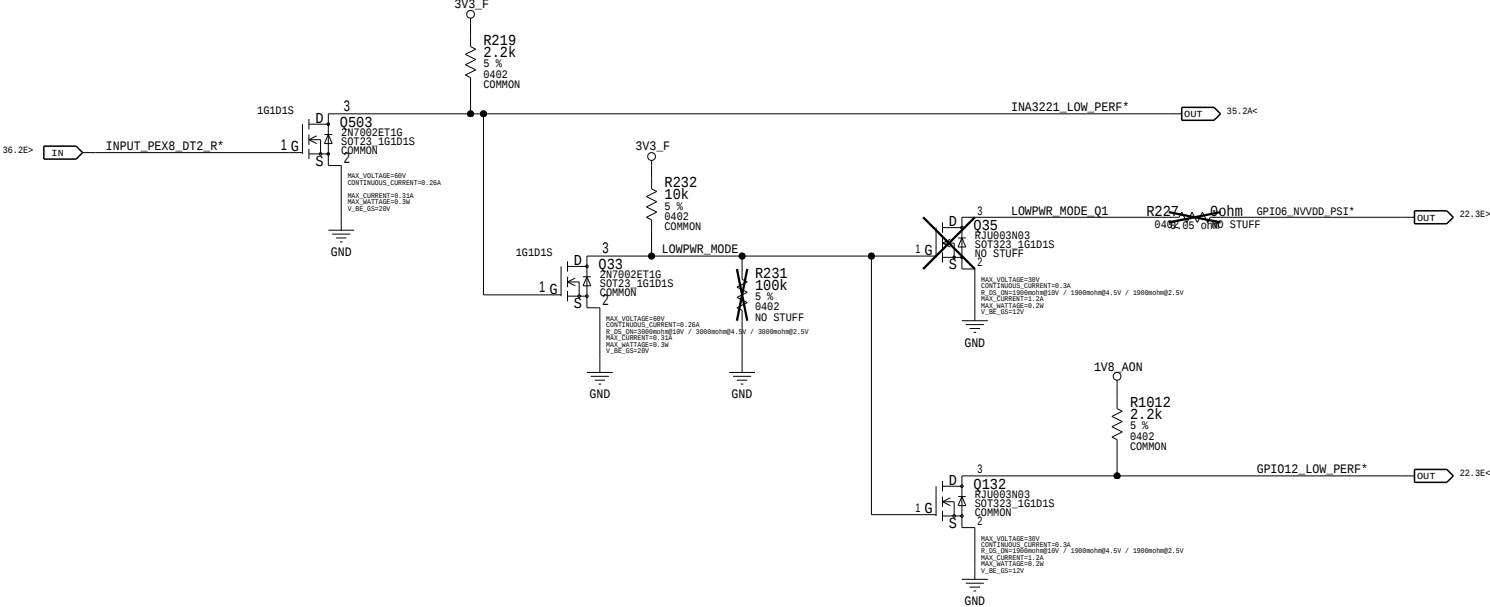
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NV_PN	600-16411-0020-110		
PCB REV	16411-A01	PAGE	36 OF 38
BOM REV	B	DATE	30-JUN-2016

PEX Input - 12V Current Steering FETs

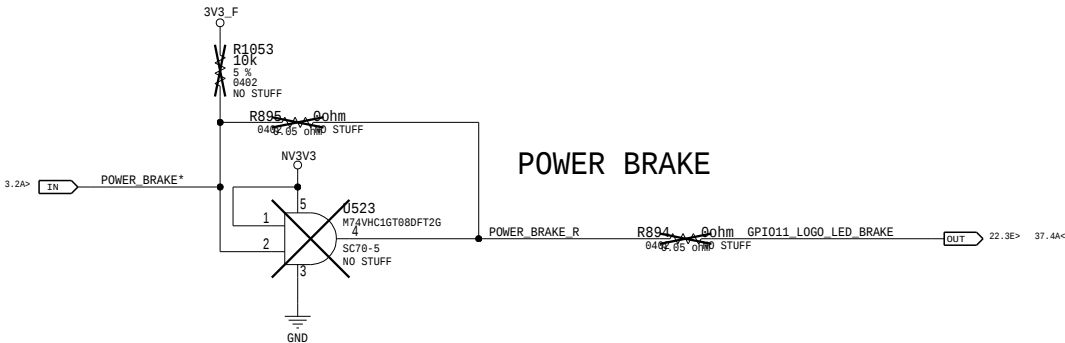


PEX Input - Power Level/PSI* Control



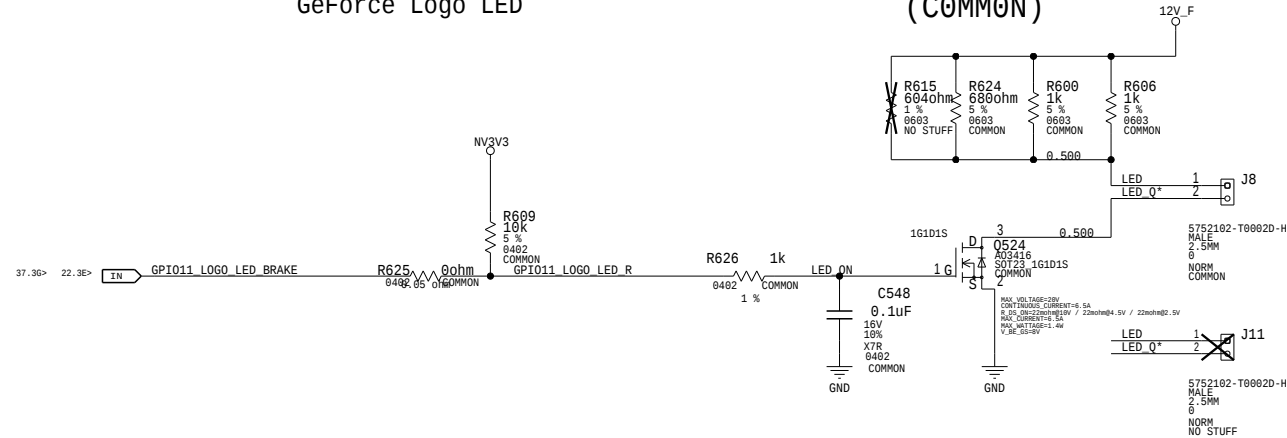
GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

POWER BRAKE

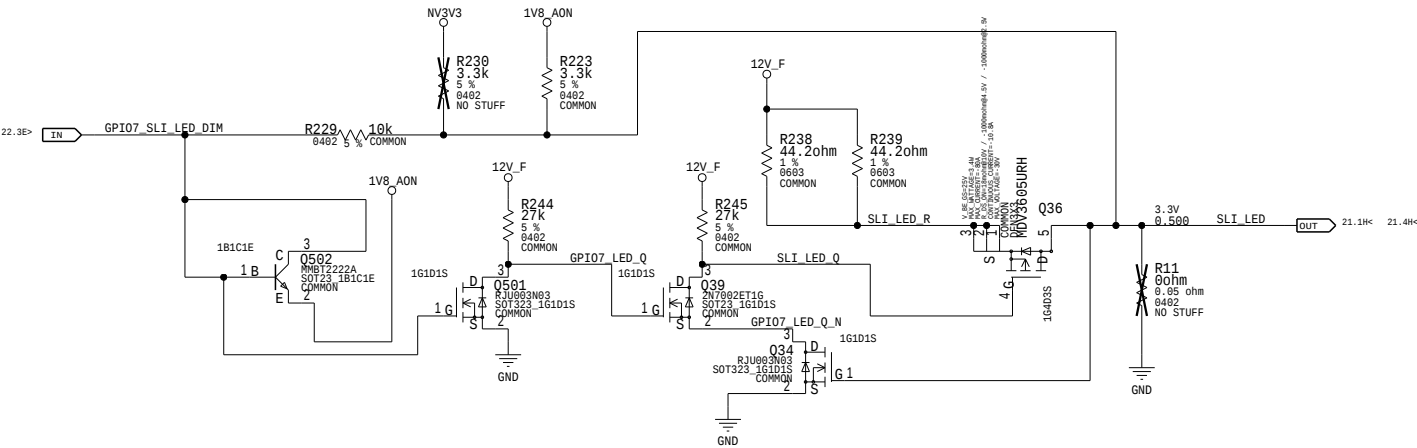


GeForce Logo LED

LED HEADER (COMMON)



SLI LED (GEFORCE ONLY)



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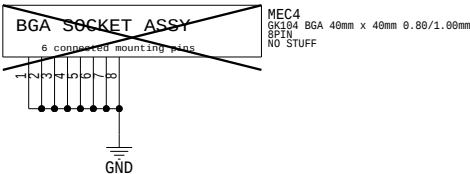
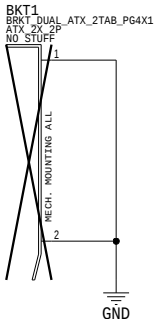
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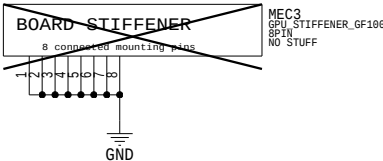
PCB REV 16411-A01 PAGE 37 OF 38

BOM REV B DATE 30-JUN-2016

Brackets:



GPU Stiffner



Mechanical Holes Symbol

