

P75D V10

GP107 128b GDDR5, 75W

DVI-D + HDMI + DP

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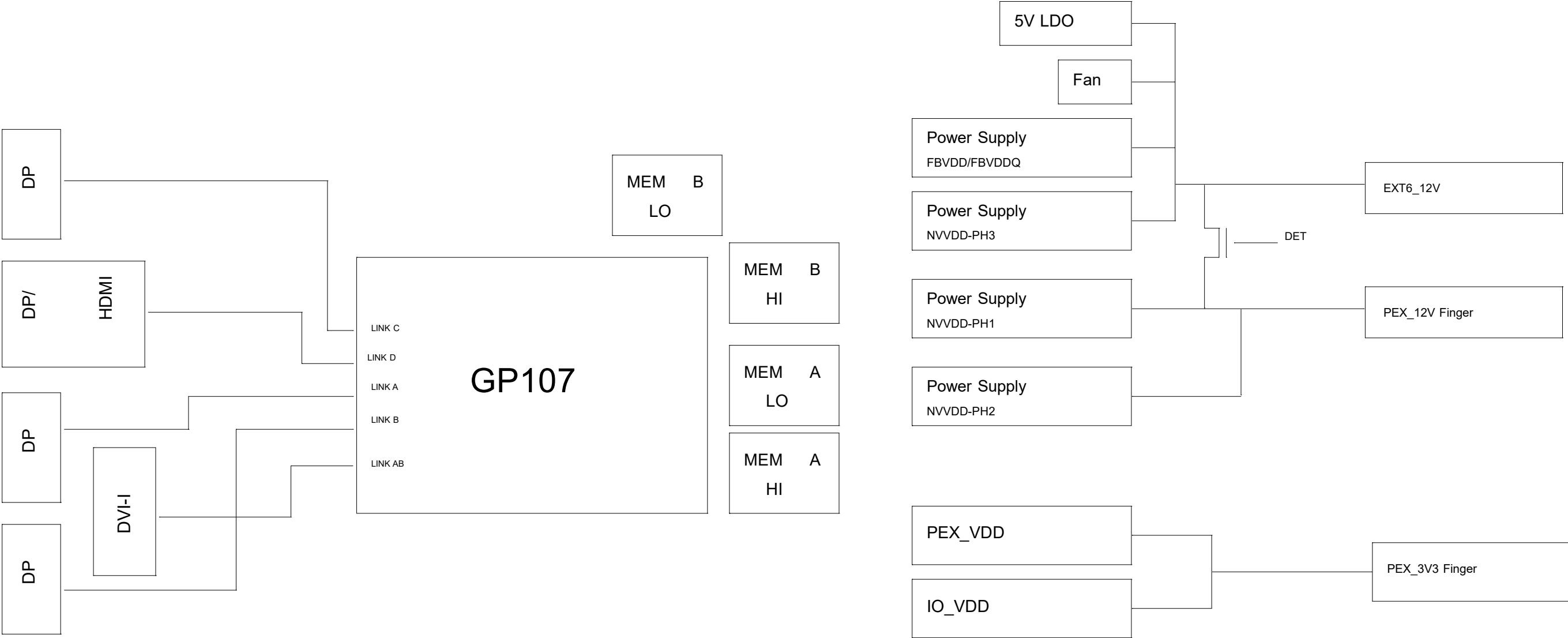
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Block Diagram



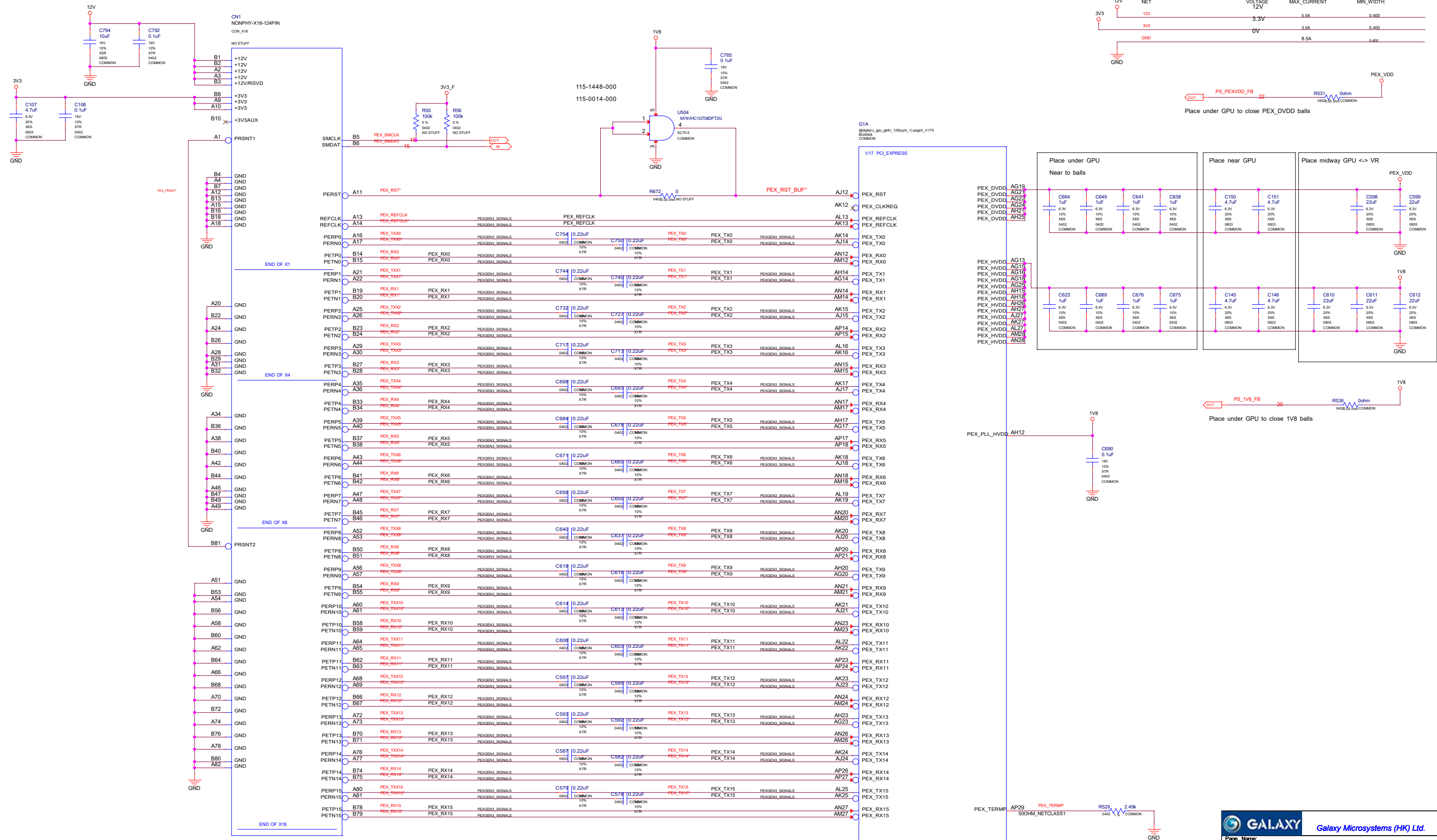
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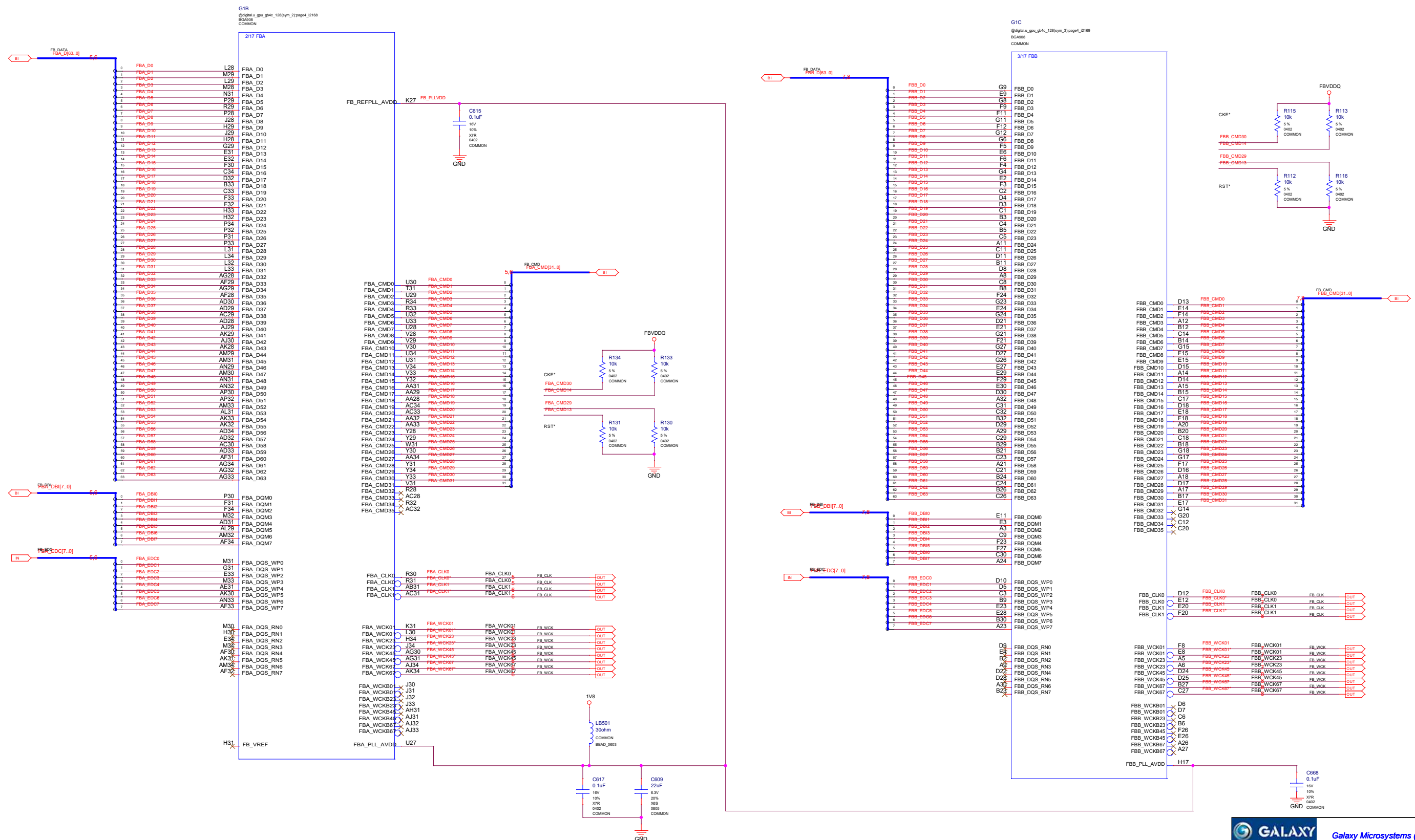
PCI Express



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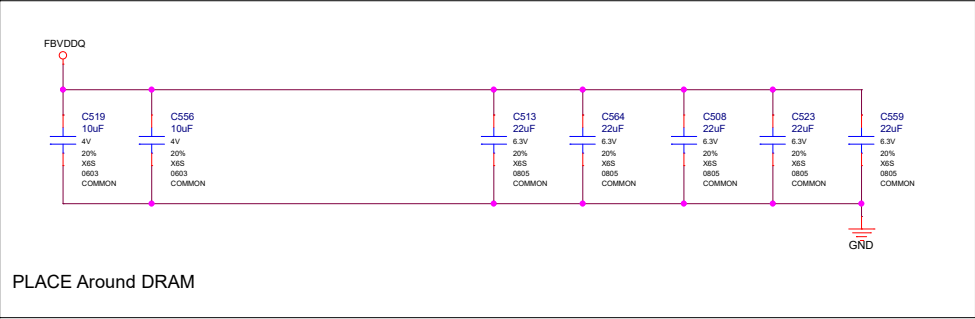
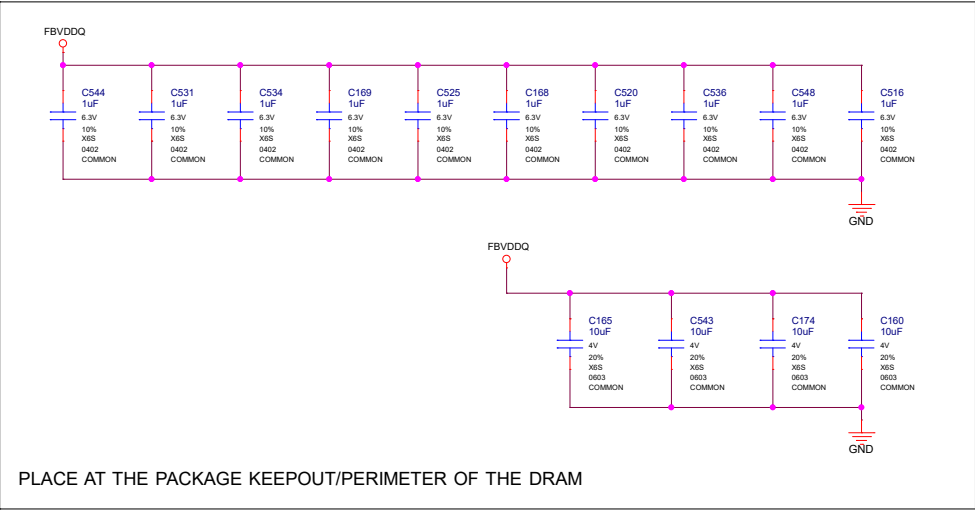
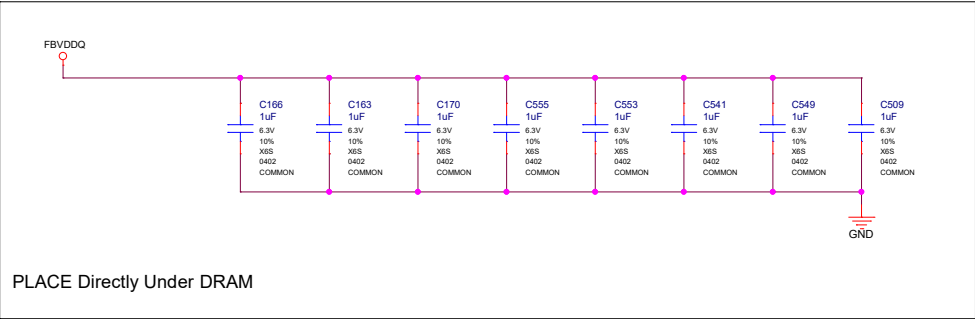
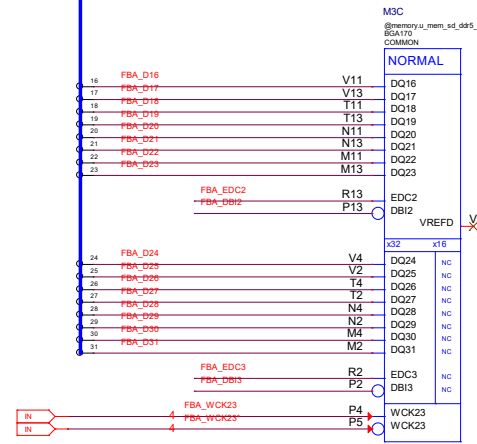
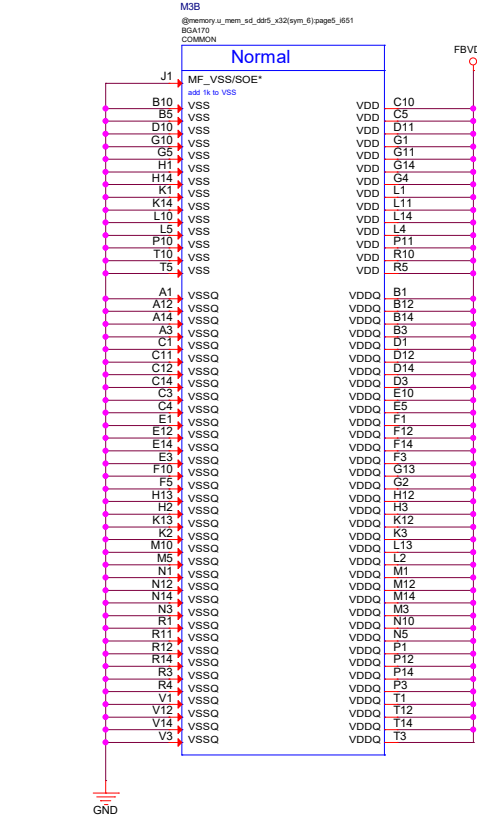
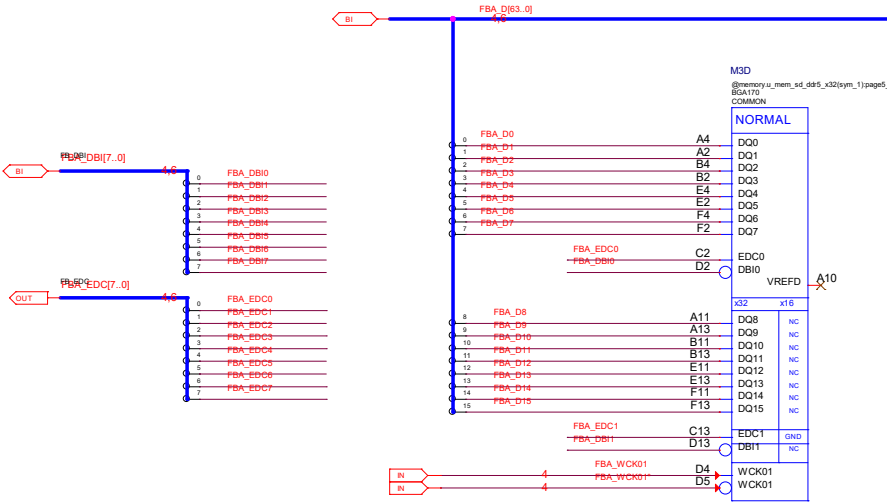
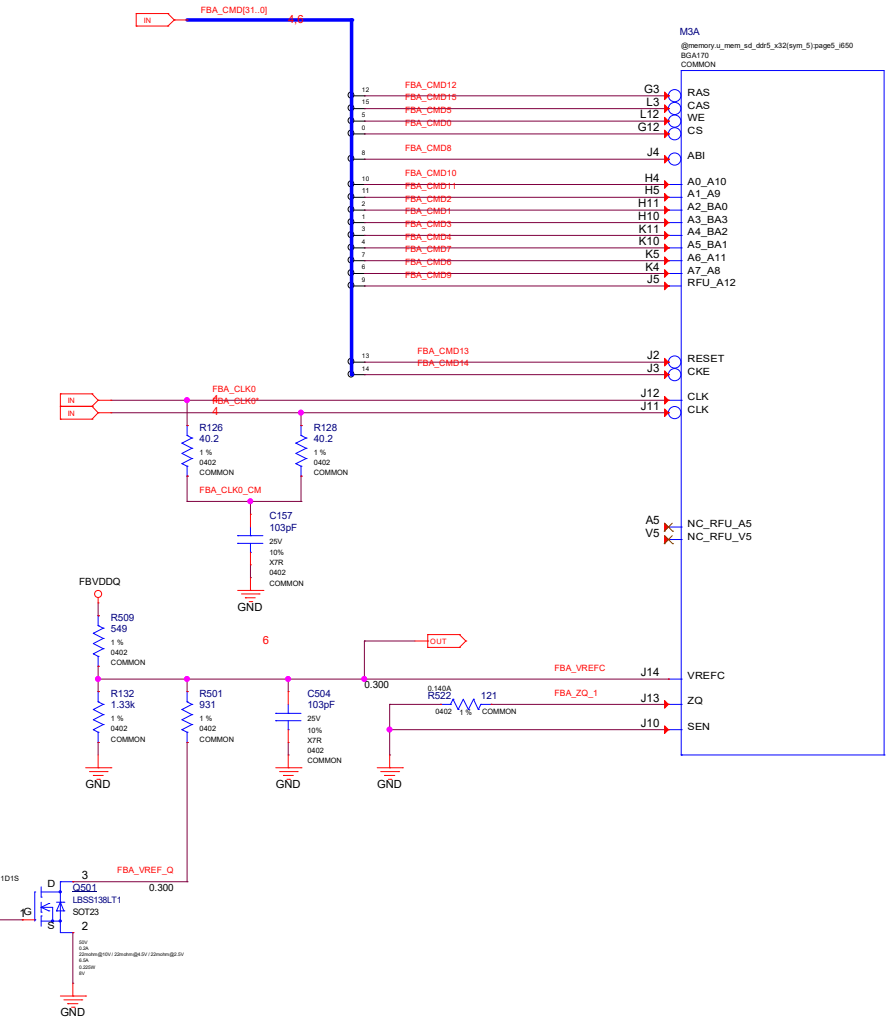
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MEMORY: GPU Partition A/B



MEMORY: FBA Partition 31..0

CMD	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	AB1*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		AB1*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*



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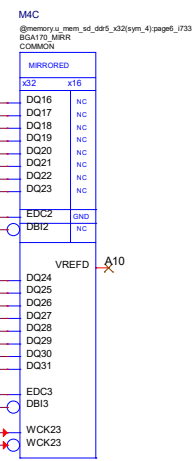
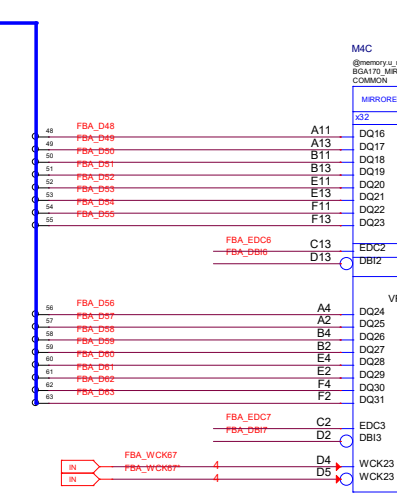
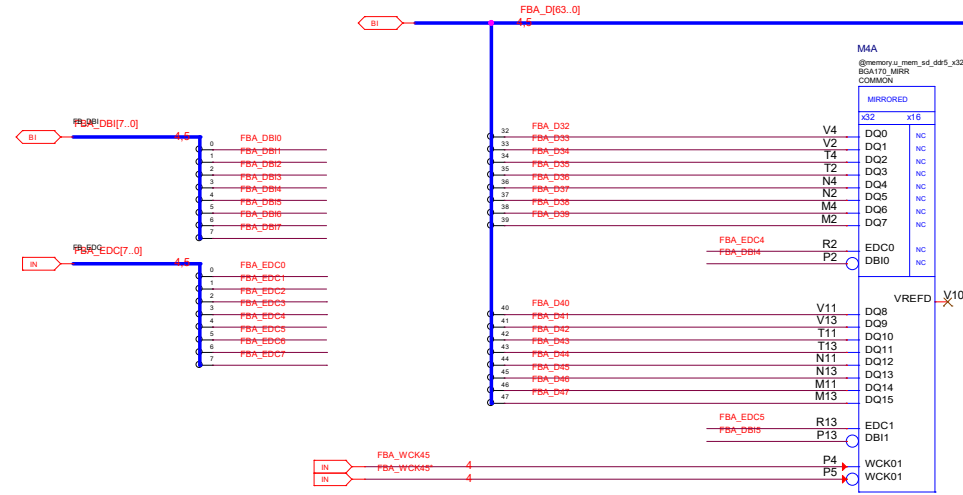
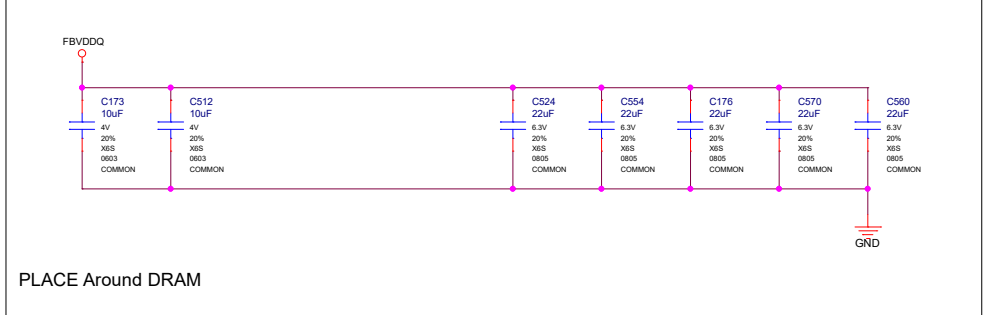
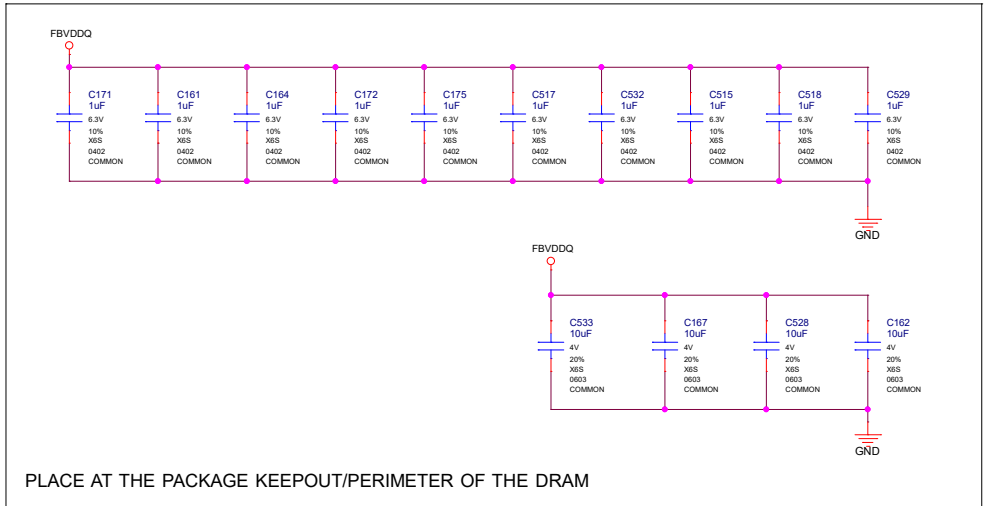
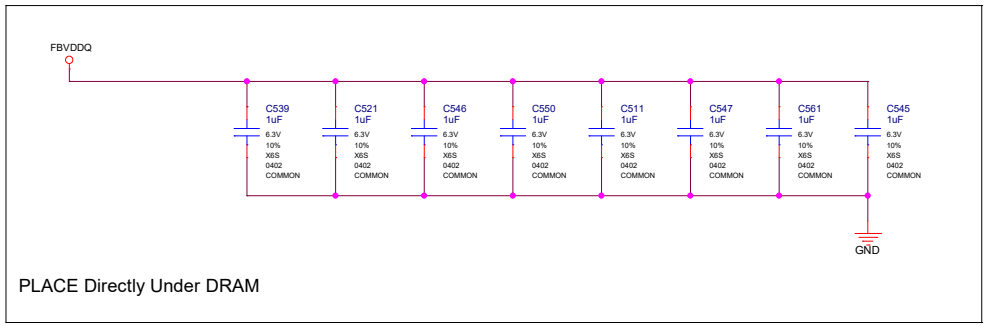
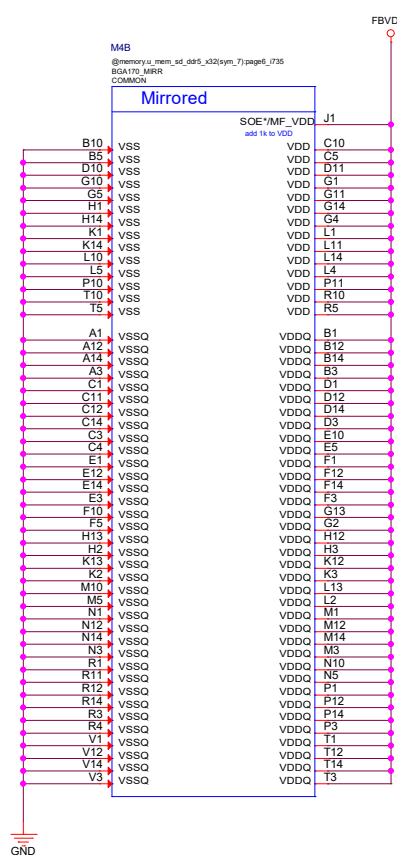
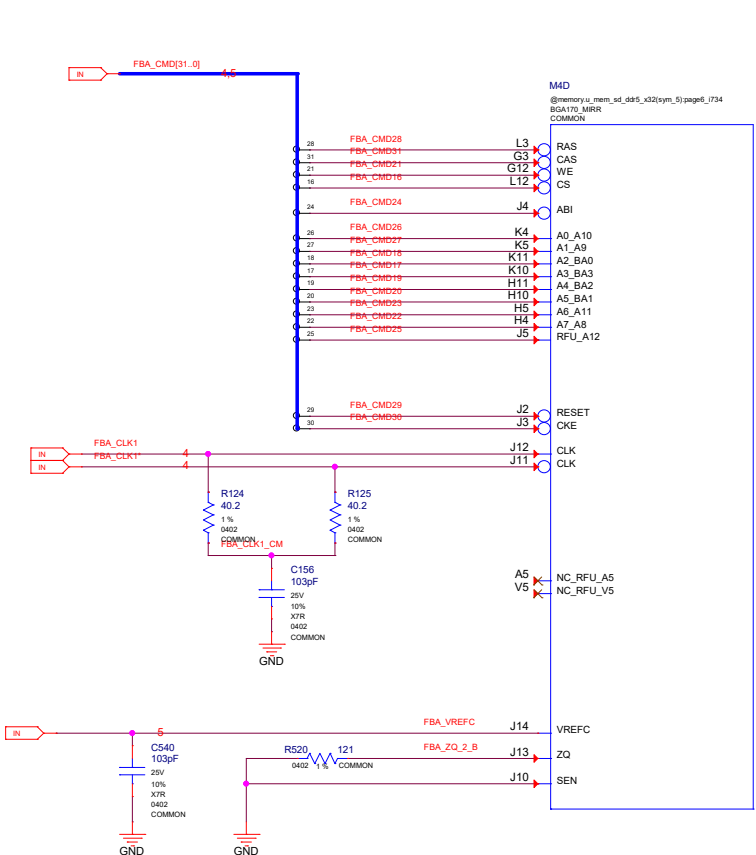
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MEMORY: FBA Partition 63..32

CMD	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	AB*	
CMD8	A12_RFU	
CMD9	A0_A10	
CMD10	A1_A9	
CMD11	RAS*	
CMD12	RST*	
CMD13	CKE*	
CMD14	CAS*	
CMD15		
CMD16		
CMD17		
CMD18		
CMD19		
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CMD31		



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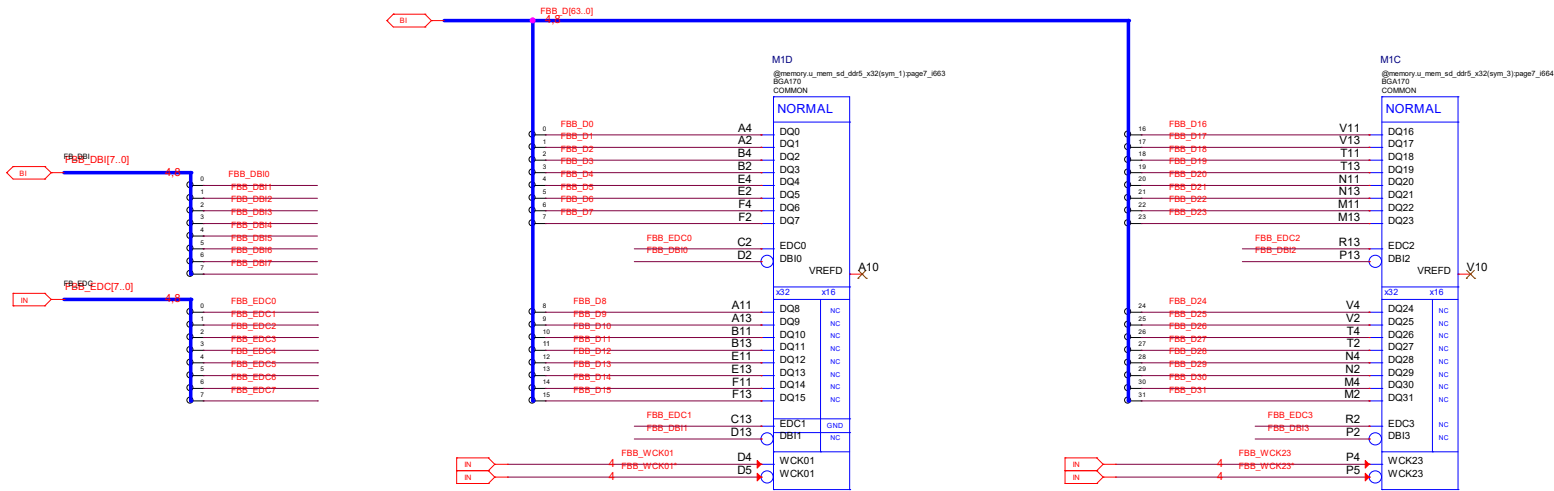
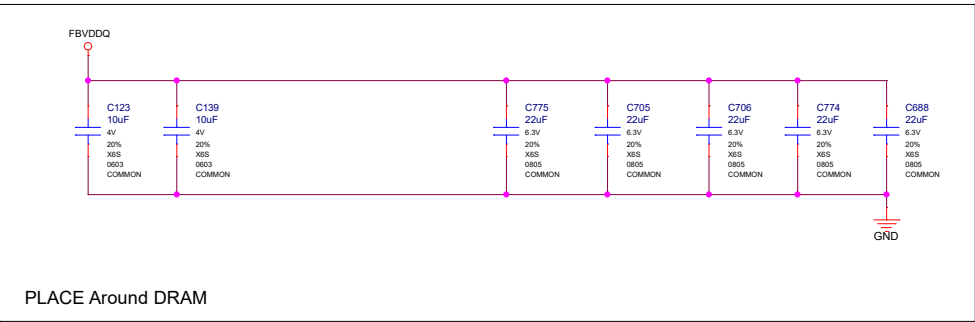
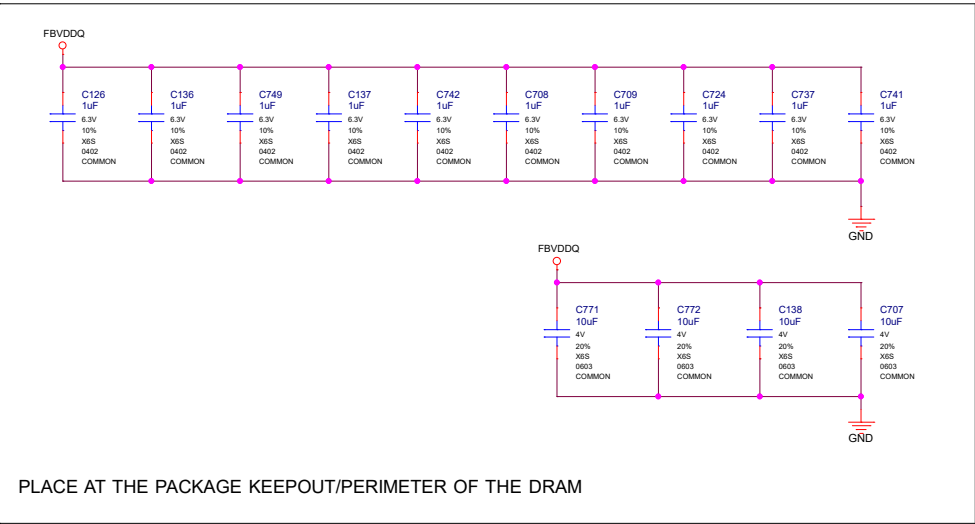
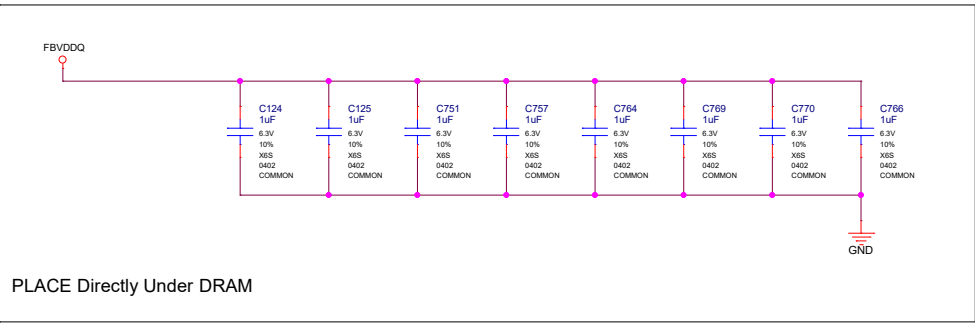
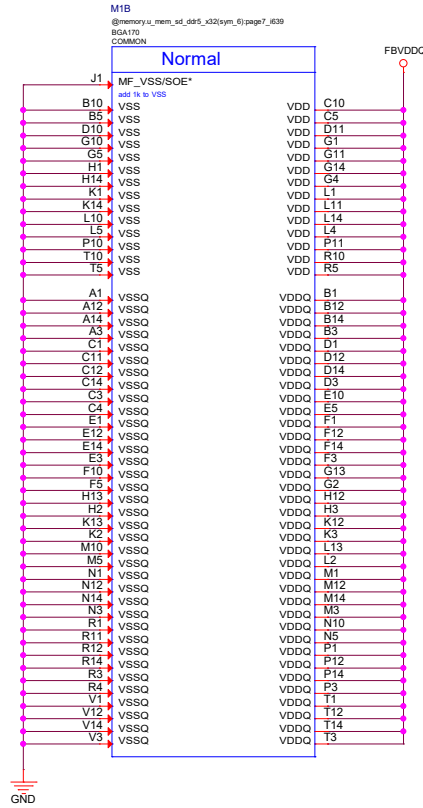
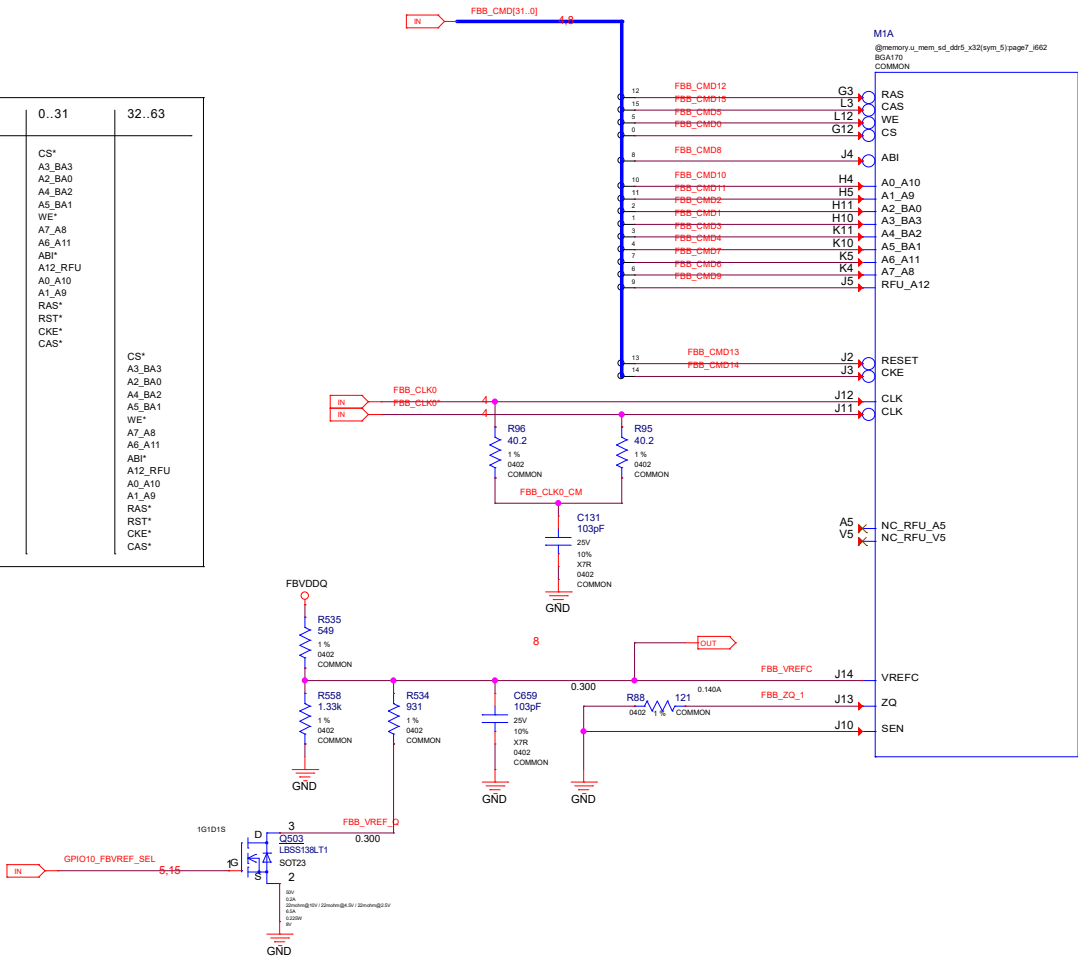
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MEMORY: FBB Partition 31..0

CMD	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	AB1*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		AB1*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*



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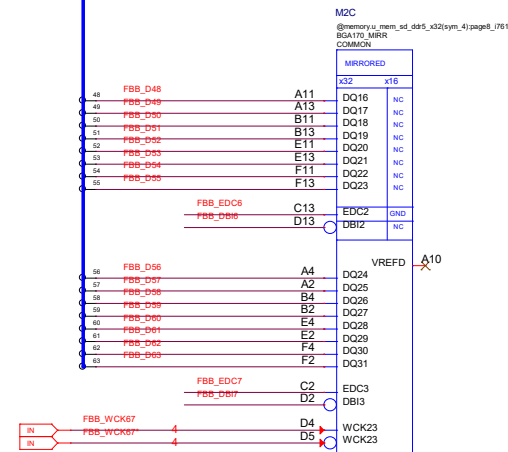
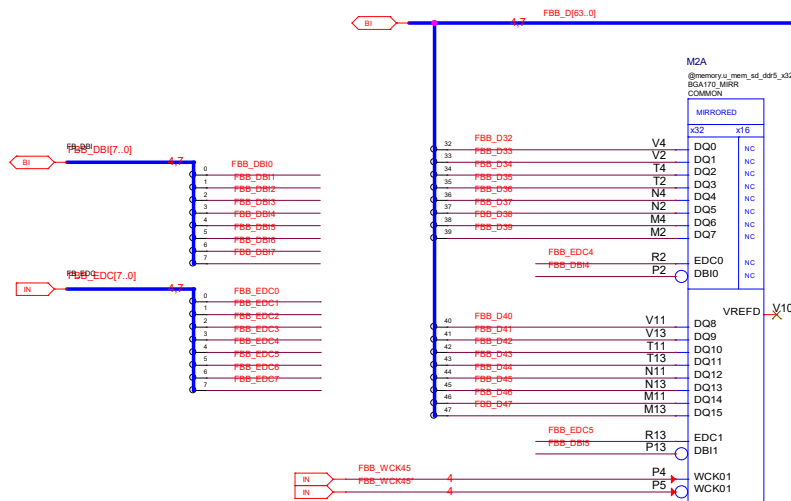
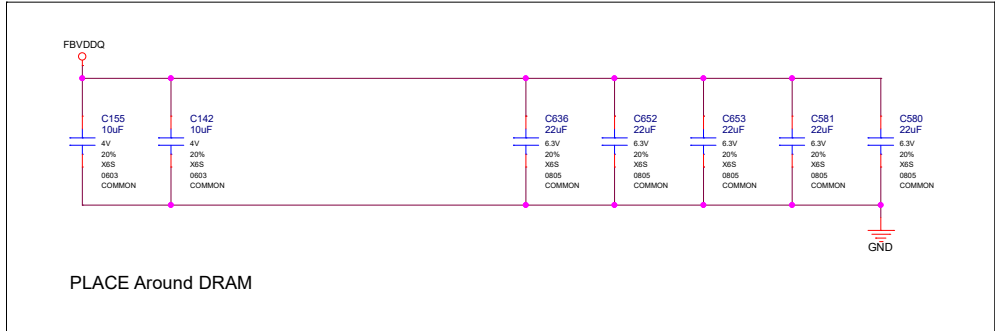
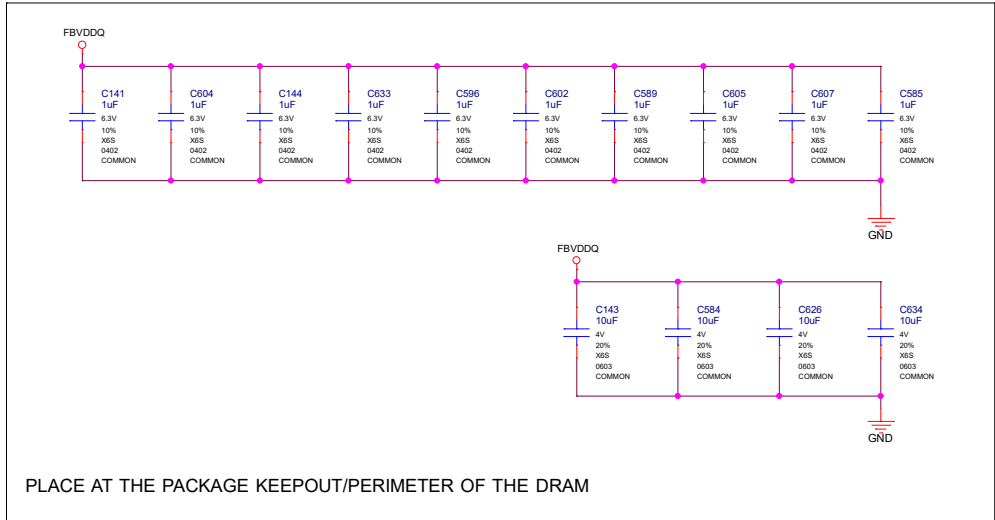
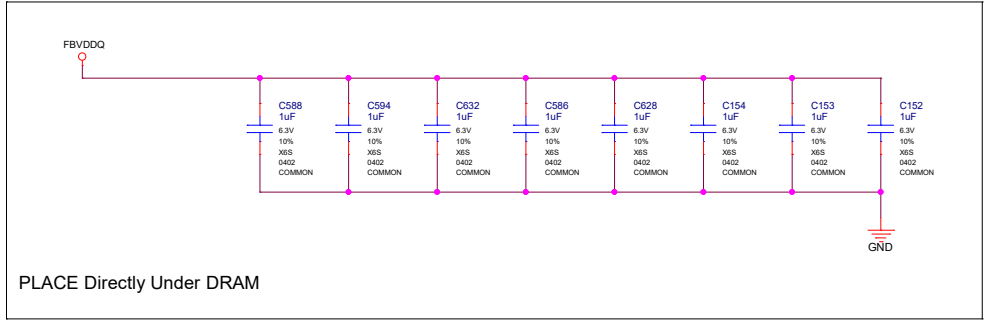
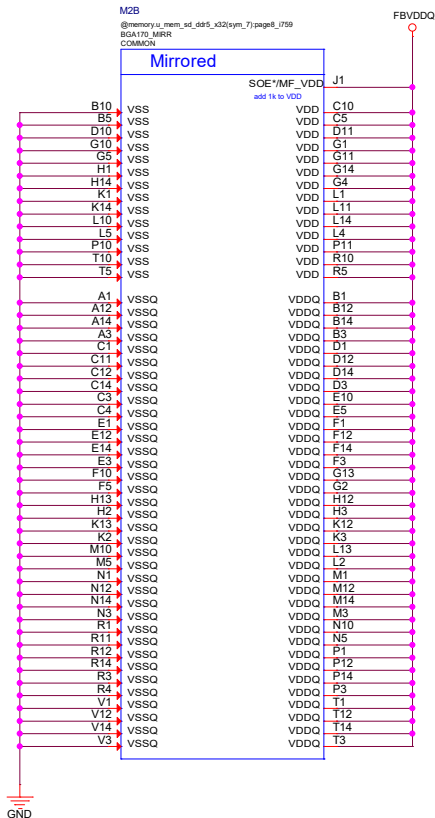
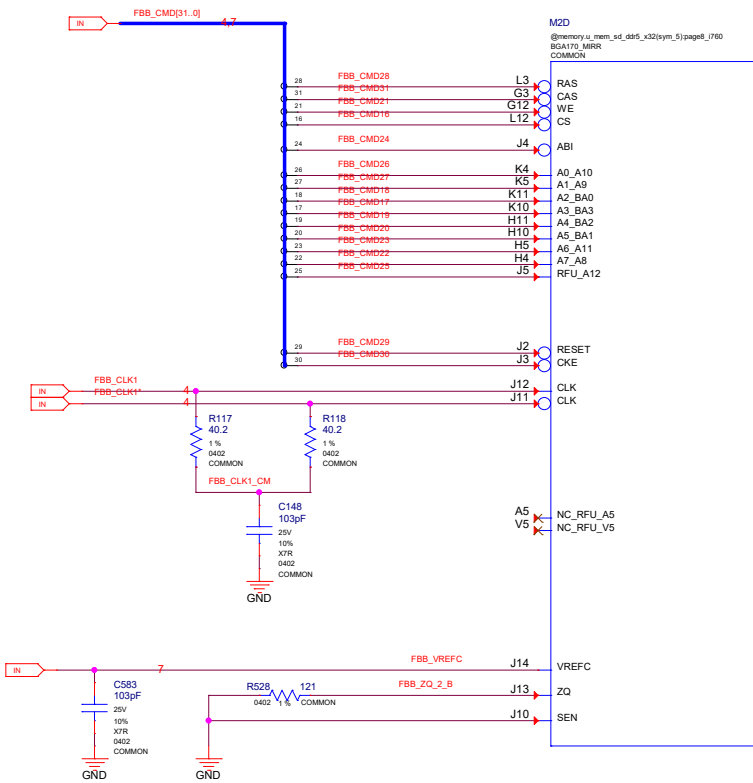
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CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	AB*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		AB*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*



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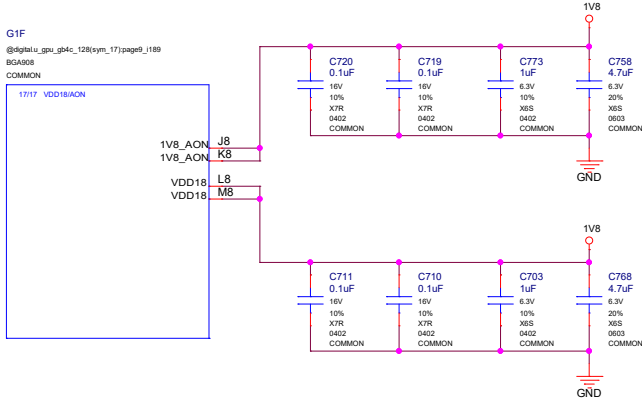
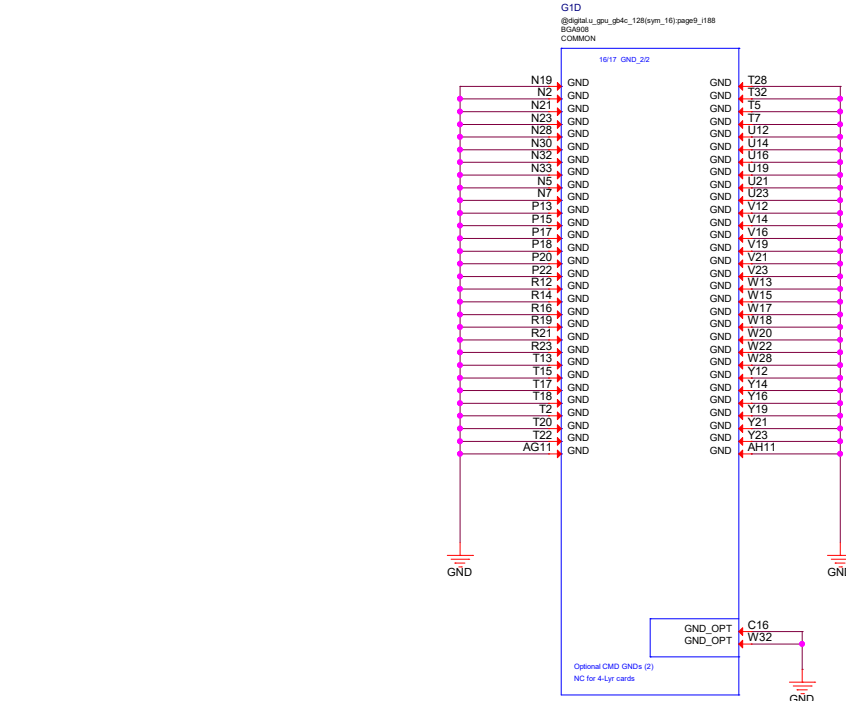
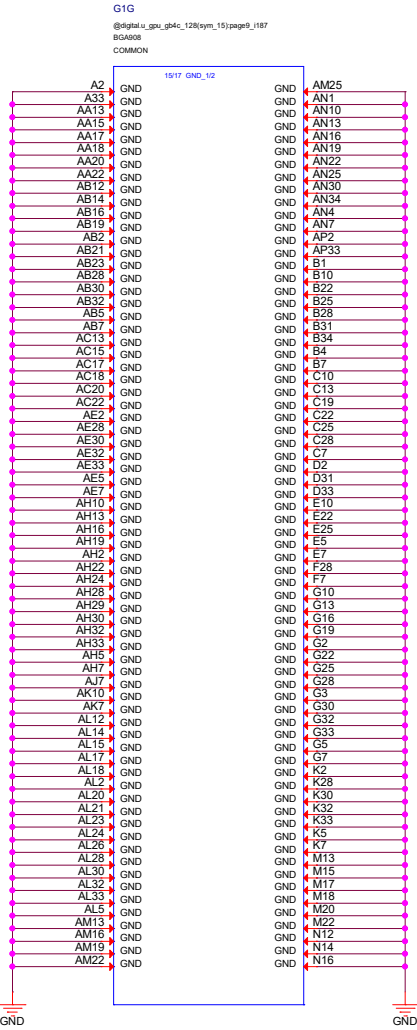
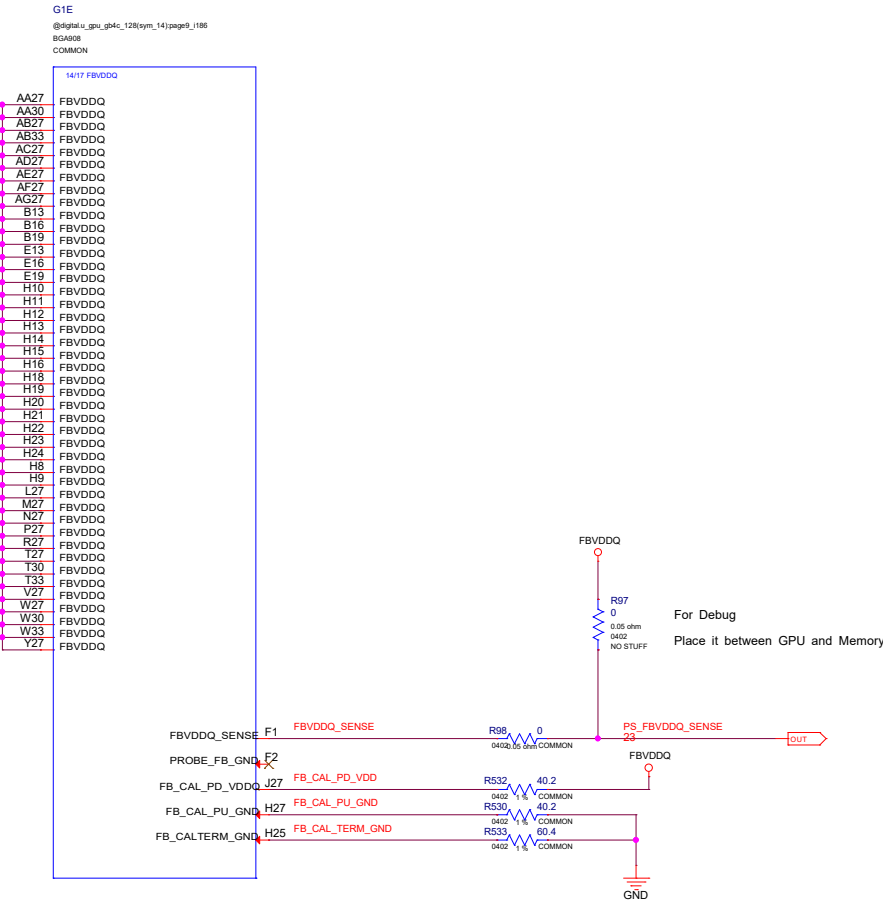
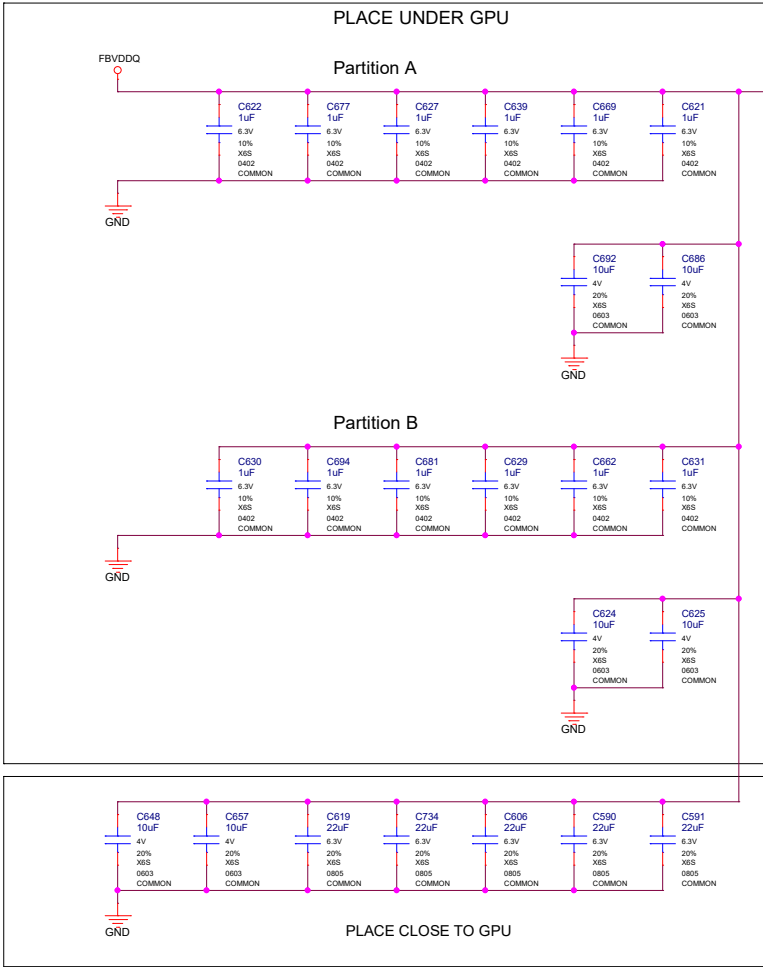
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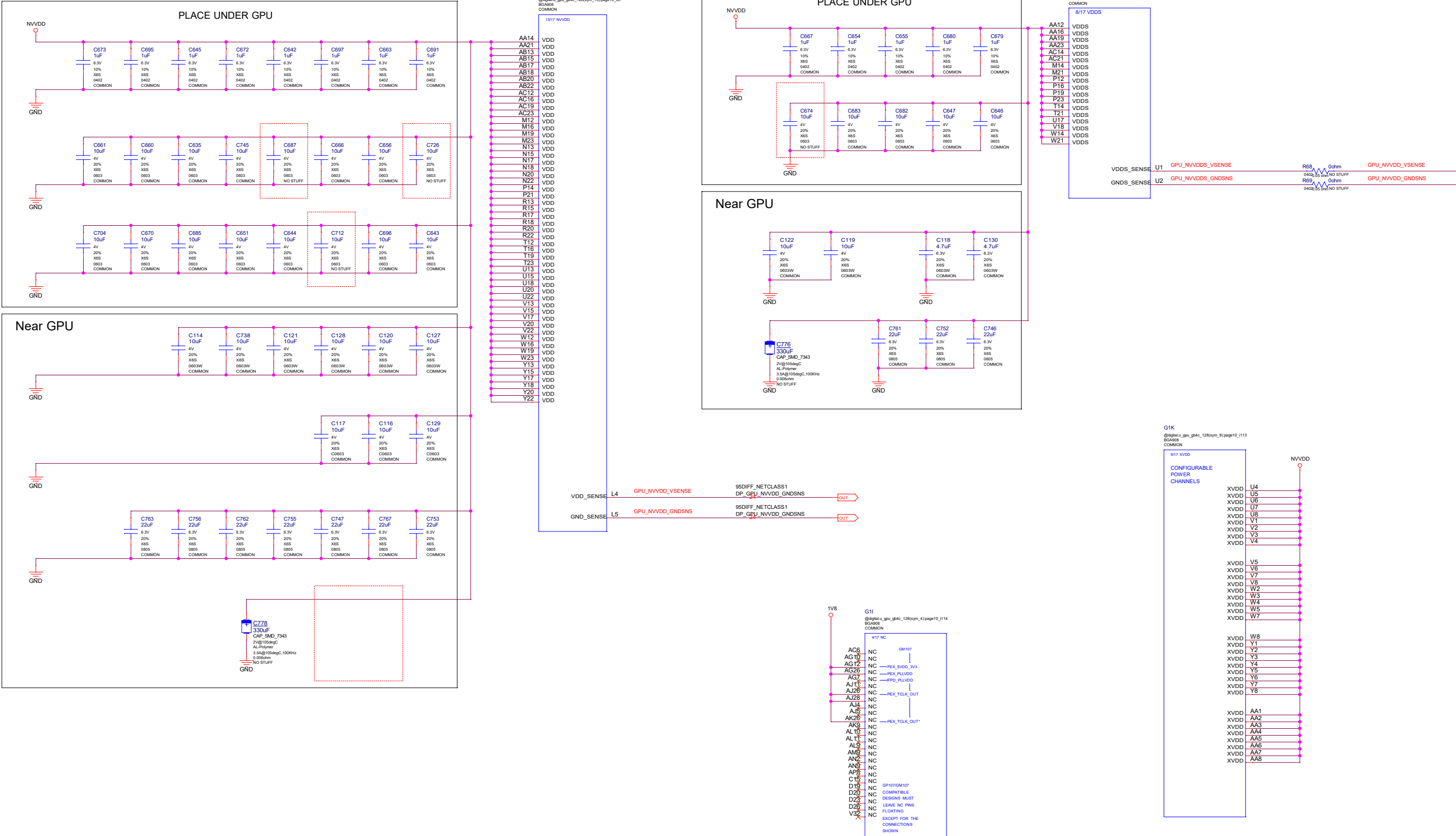
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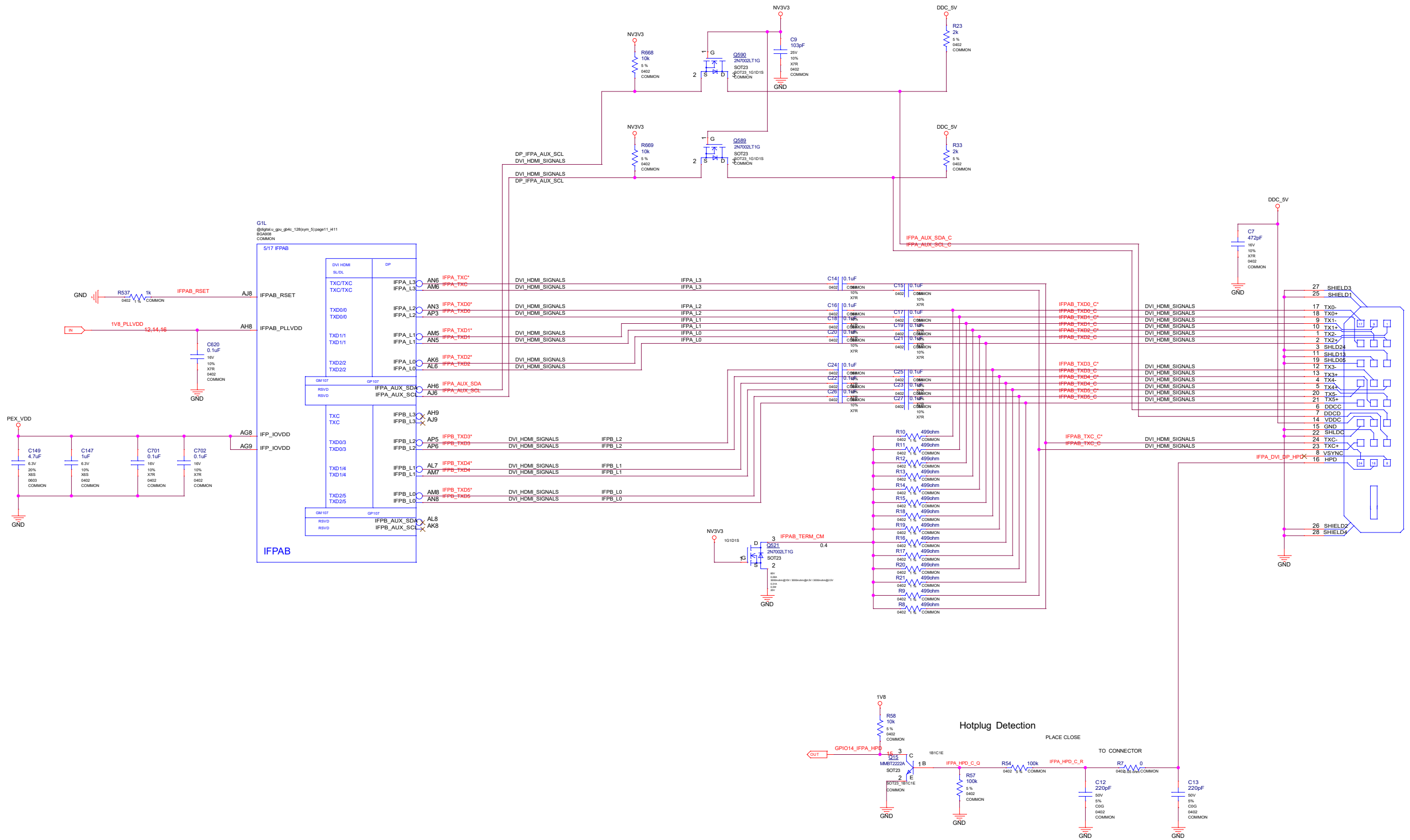
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ASSEMBLY PAGE DETAIL <ASSEMBLY_DESCRIPTION> GPU FBVDDQ & 1V8 Decoupling

GPU NVVDD & NVVDDS Decoupling

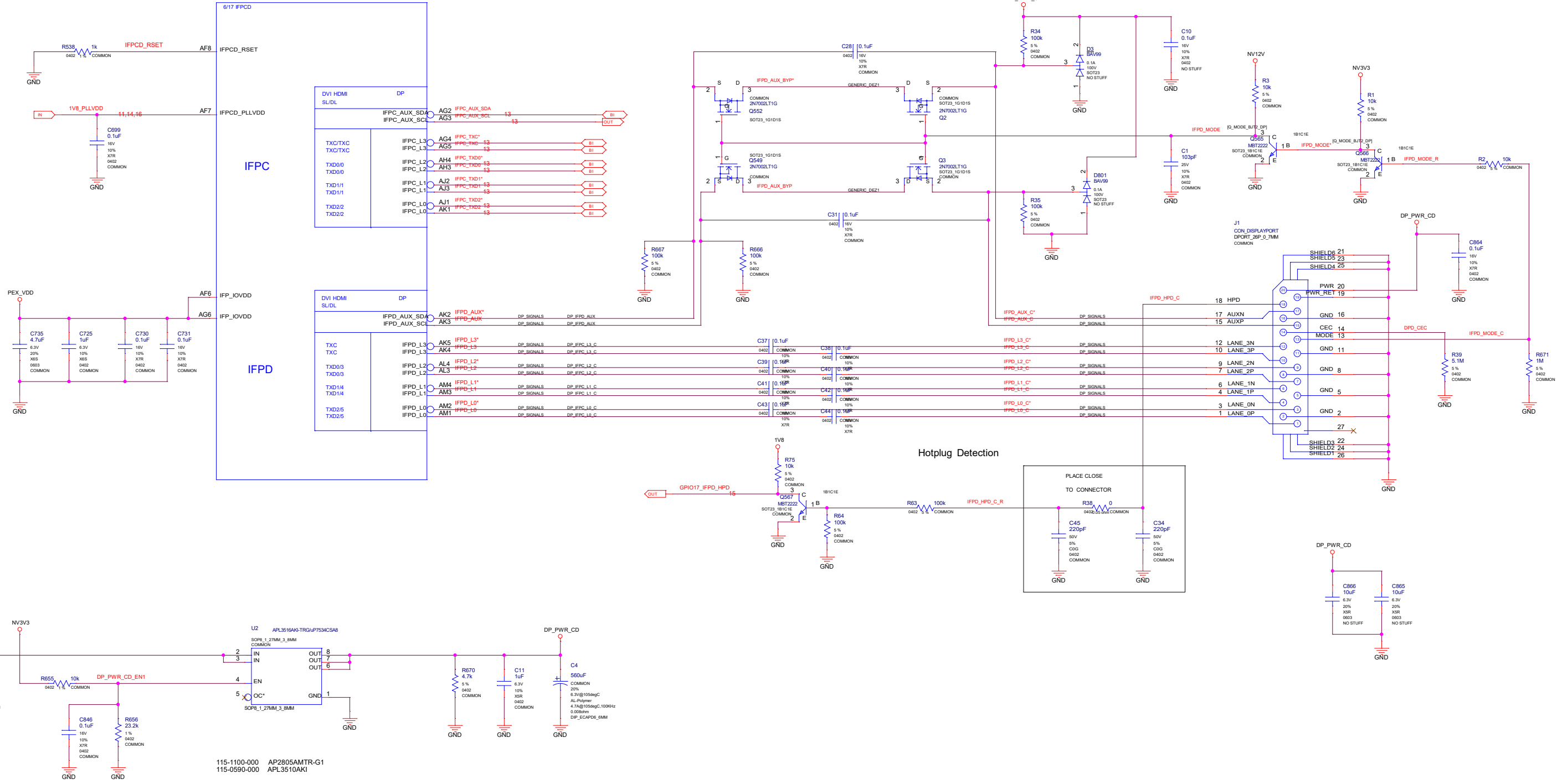


IFPAB DVI-DL



IFPD DP

G1M
(@digital_u_gnu_gnu4c_128vpm_8) page12_613
BGA008
COMMON



115-1100-000 AP2805AMTR-G1
115-0590-000 APL3510AK1

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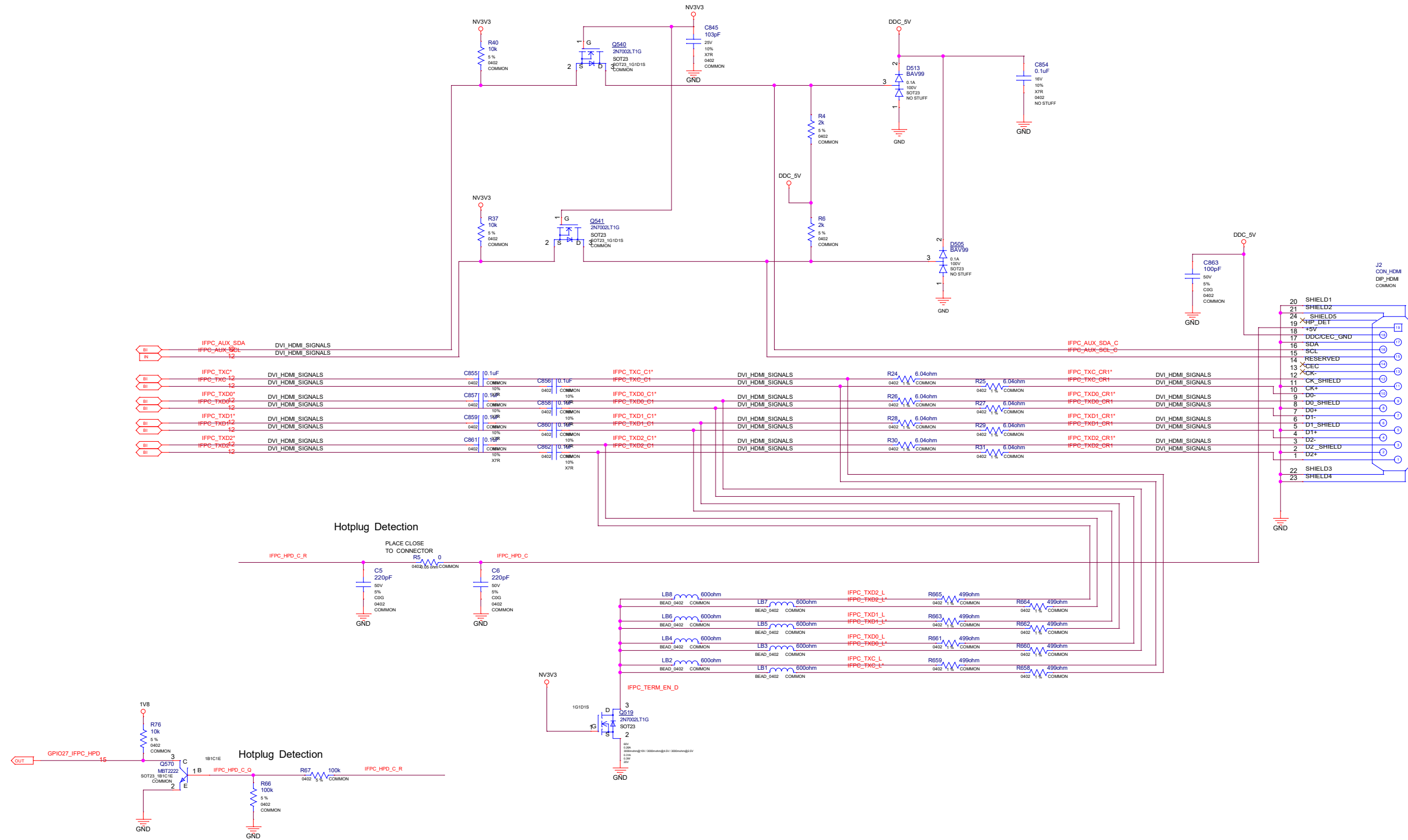
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IFPD DP

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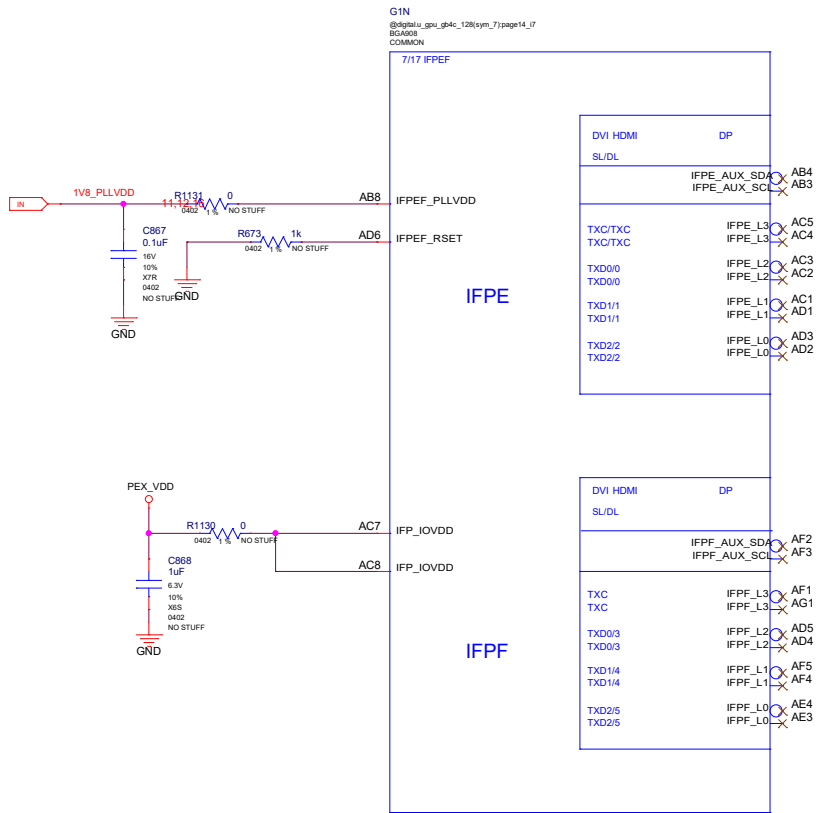
IFPC HDMI



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Page Name: IFPC HDMI			
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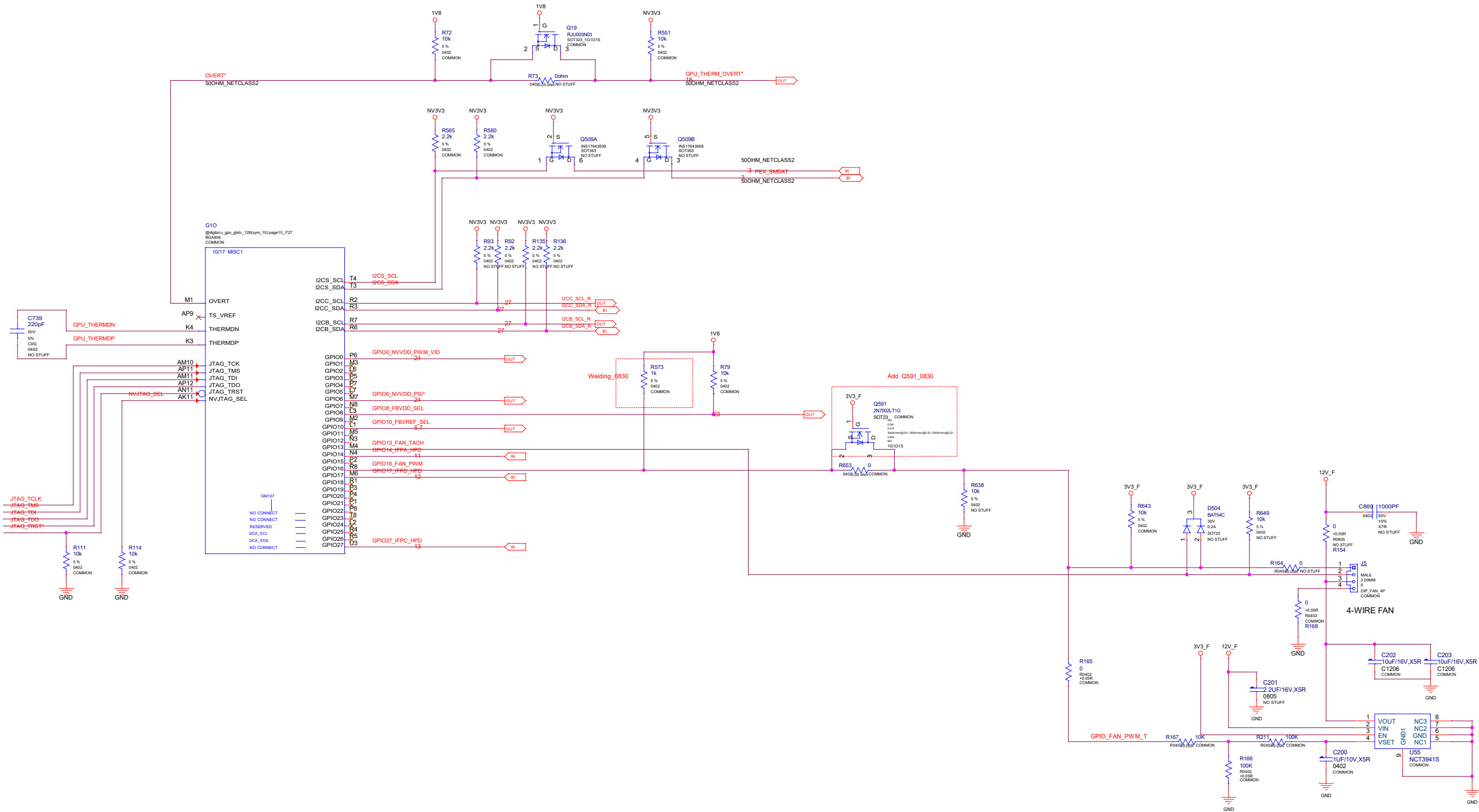


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Page Name: IFPD DP			
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MISC1: GPIO, Fan, Thermal, JTAG

PADS FOR DEBUGGING



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MISC1: Fan, Thermal, JTAG, GPIO

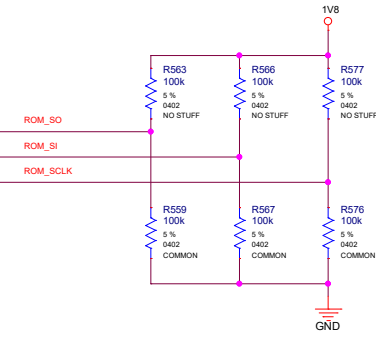
 GALAXY		<i>Galaxy Microsystems (HK) Ltd.</i>	
Page Name: MISC1: GPIO, Fan, Thermal, JTAG			
Size Custom	Project Name: P75L	Design By: James	Re: V10
Date: Wednesday, December 21, 2016		Sheet 15 of	
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MISC2: ROM, XTAL, Straps

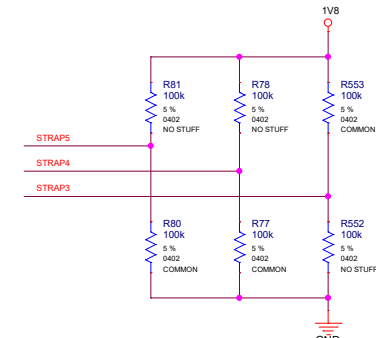
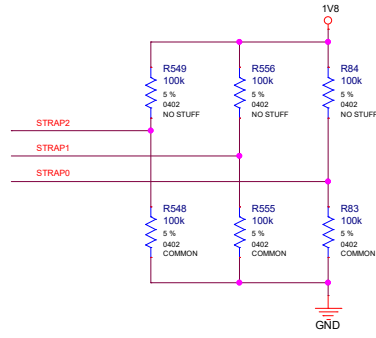
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	Default
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung B-Die 8Gb 256Mx32
L	L	H	0001	Micron F-Die 8Gb 256Mx32
L	H	L	0010	Hynix M-Die 8Gb 256Mx32
L	H	H	0011	
H	H	L	0110	Hynix A-Die 4Gb 128Mx32
H	H	H	0111	Samsung E-Die 4Gb 128Mx32
L	L	M	1000	Micron B-Die 4Gb 128Mx32
L	M	L	1001	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0



H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

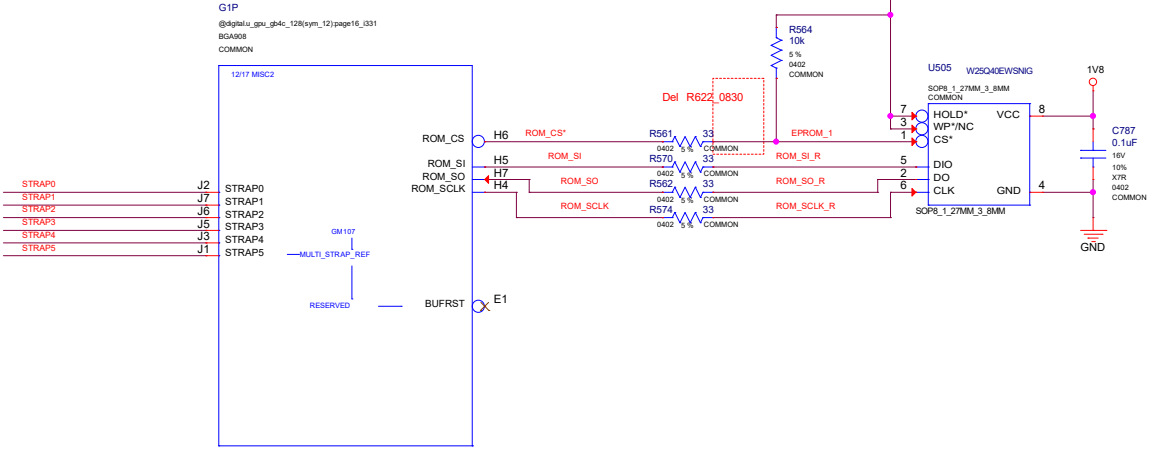


1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

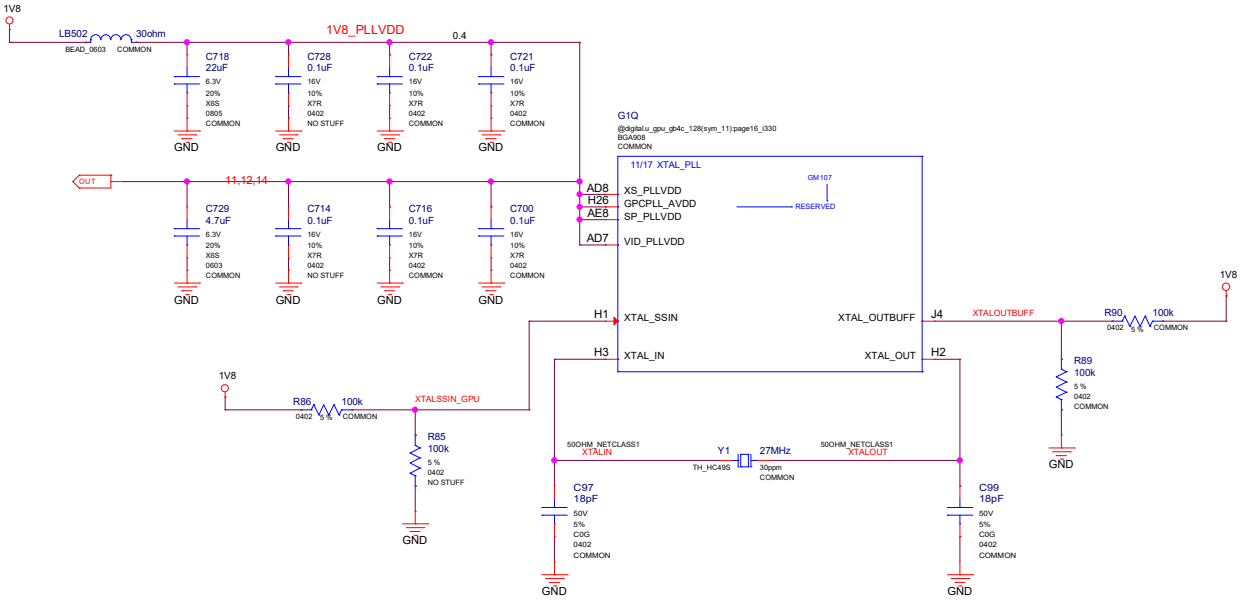
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



Smart Fan

XTALOUTBUFF	Volatge	SmartFan PWM	GPIO/PWM at the FAN
Low	0V	GPIO Disabled	100%
Middle	0.9V	66% PWM	33% PWM (Typical)
High	1.8V	33% PWM	66% PWM



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MISC2: ROM, XTAL, Straps

Size Custom

Project Name: P75L

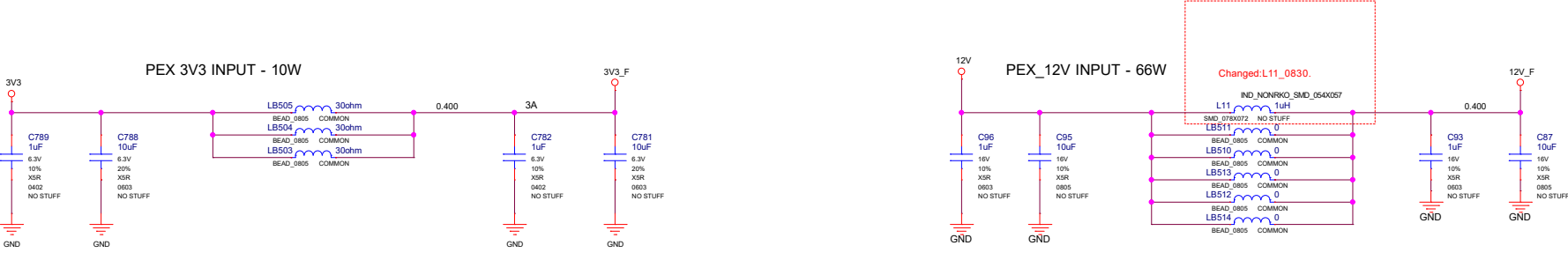
Design By: James

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Power Inputs and Filtering



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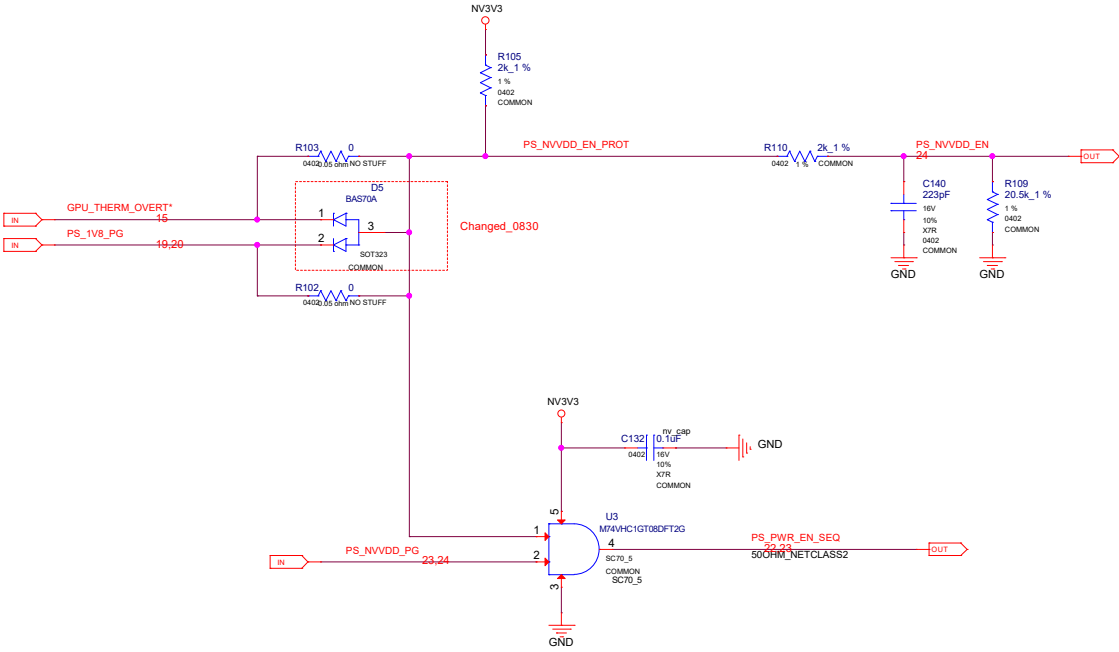
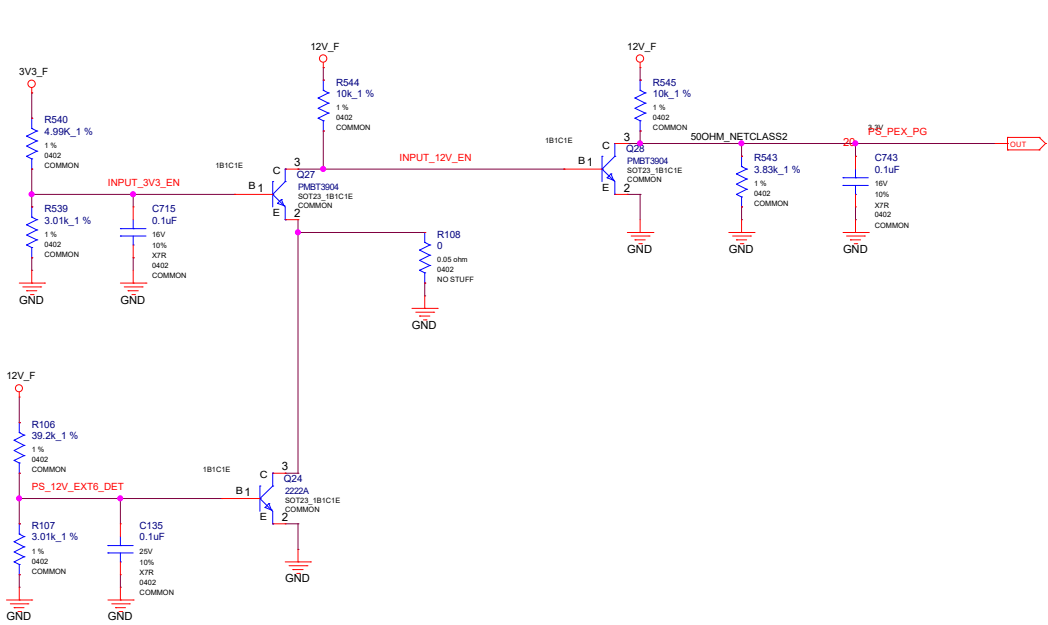
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Page Name:
Power Inputs and Filtering

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Power sequence



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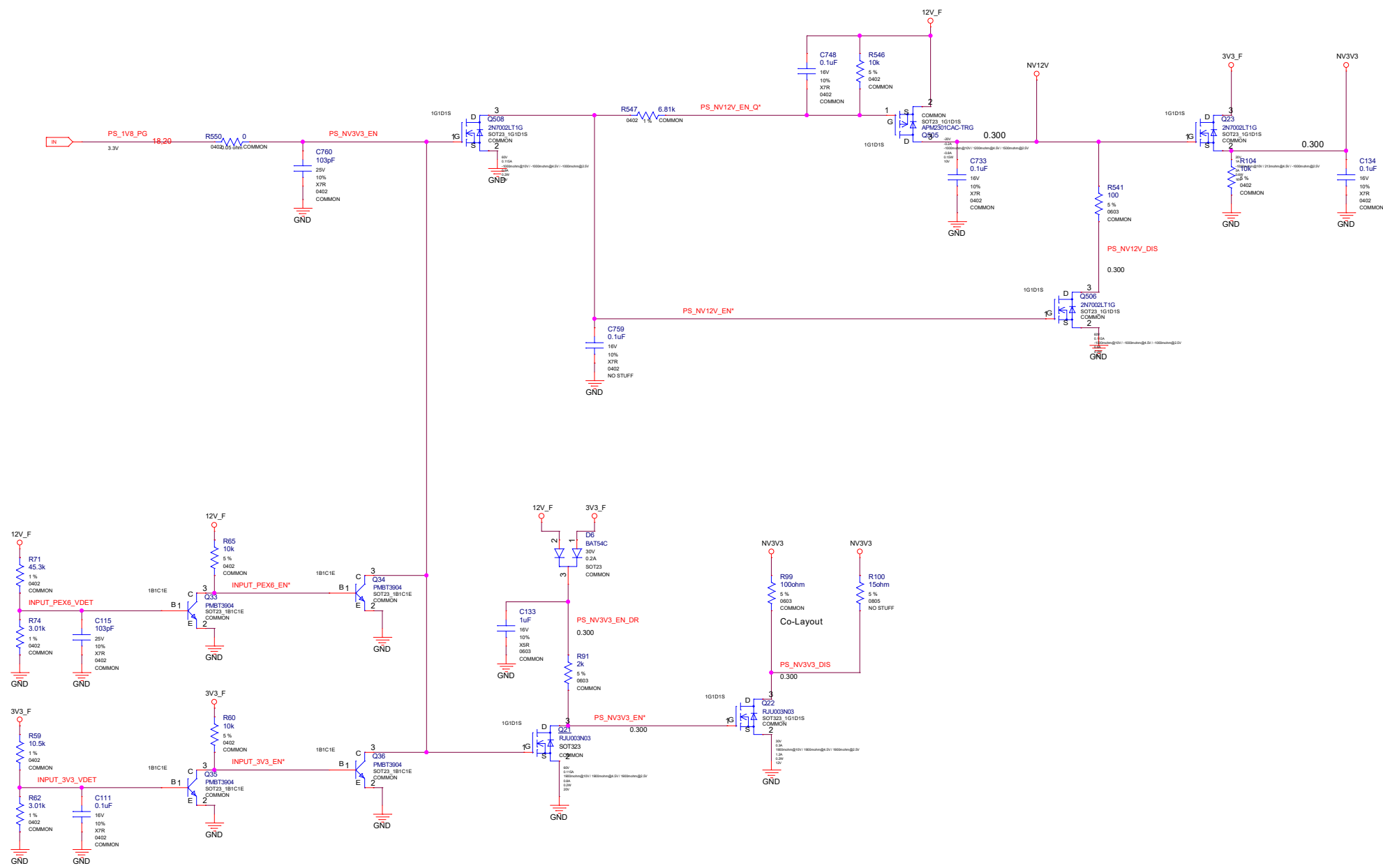
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Power Sequence



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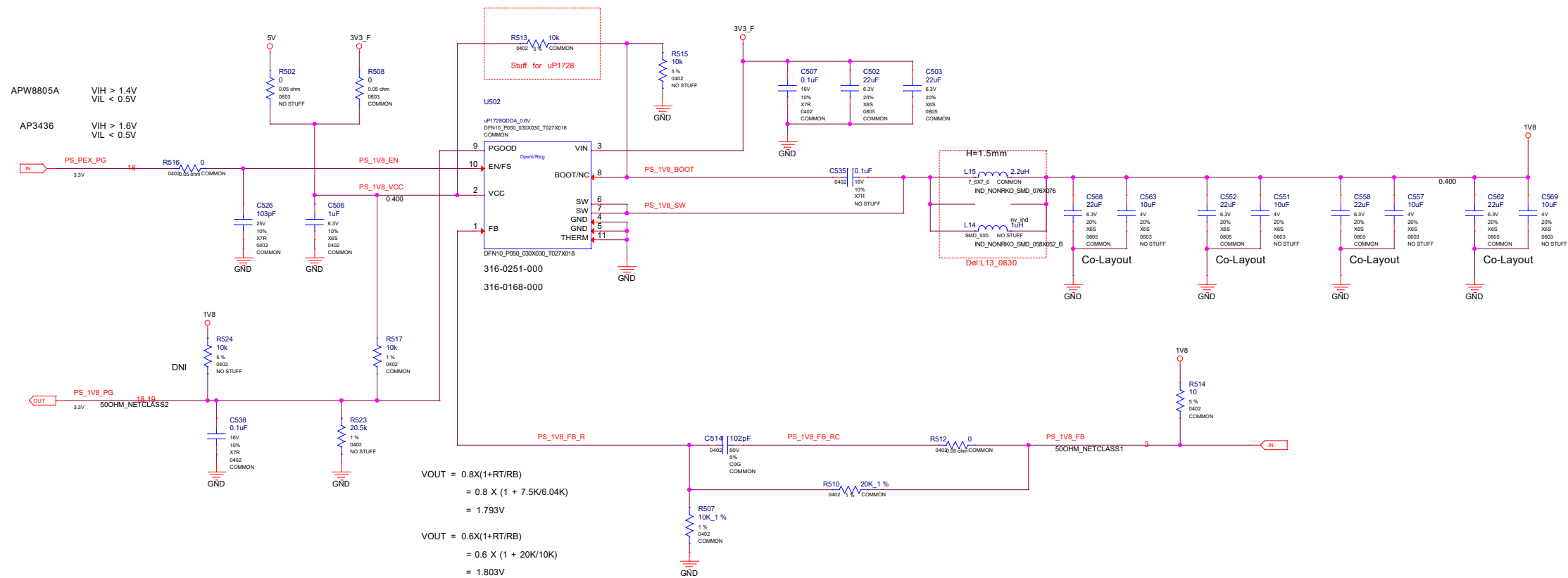
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Size: Custom	Project Name: P75L	Design By: James	Rev: V10
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PS: NV3V3 & NV12V



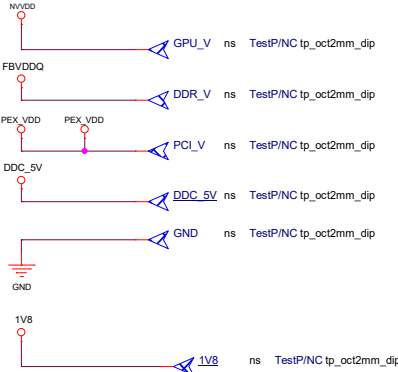
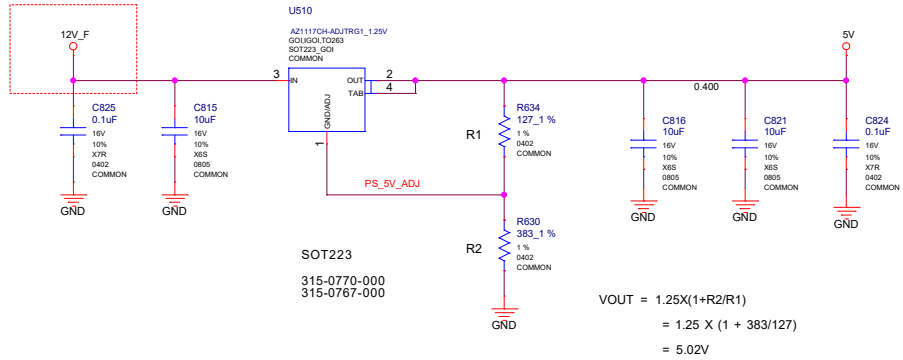
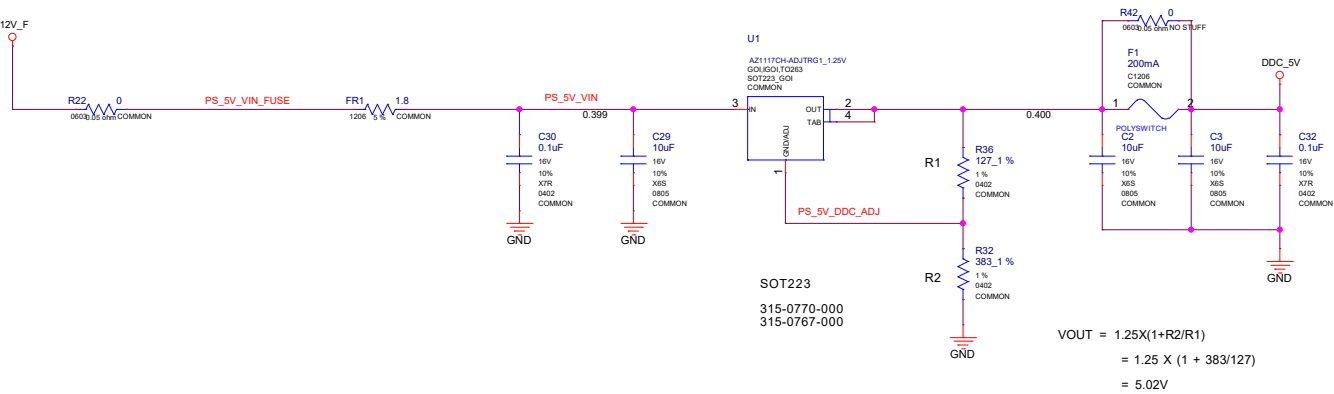
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NV3V3 & NV12V



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PSII:5V



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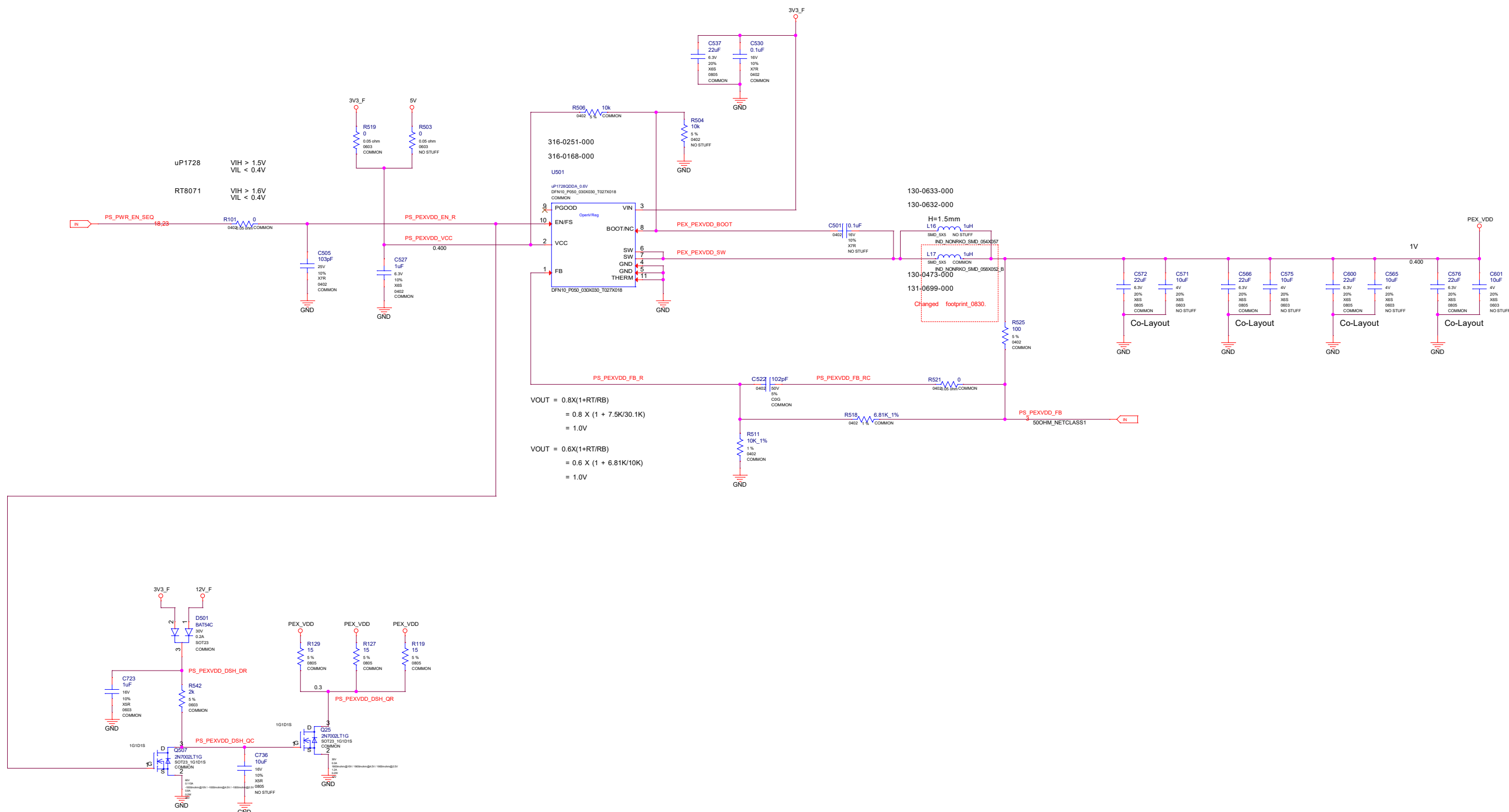
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PSII: 5V & 12V_FAN



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Page Name: PSII:5V & 12V_FAN			
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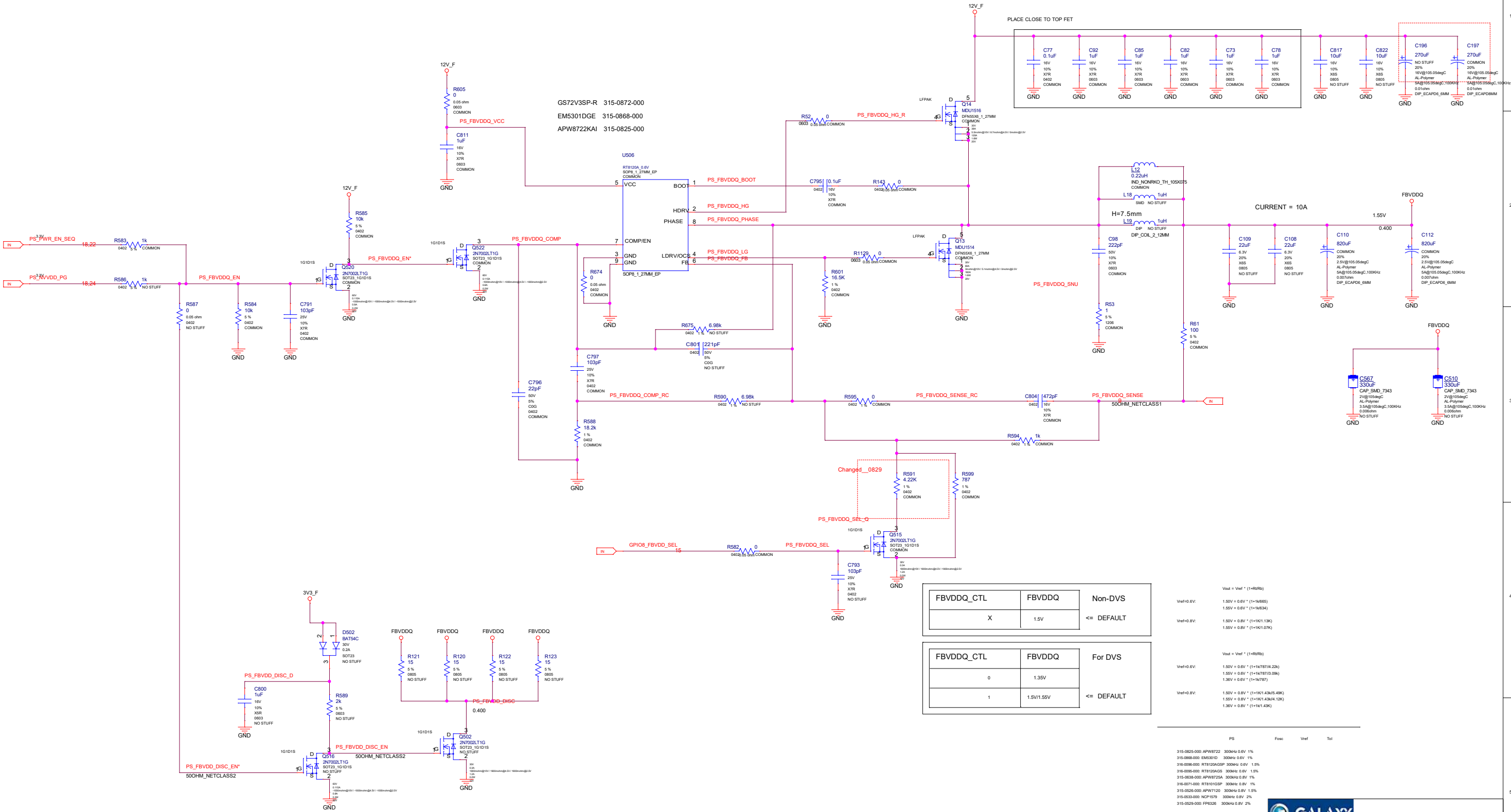
PS III: PEXVDD



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PAGE DETAIL	PS III: PEXVDD

PS IV: FBVDDQ



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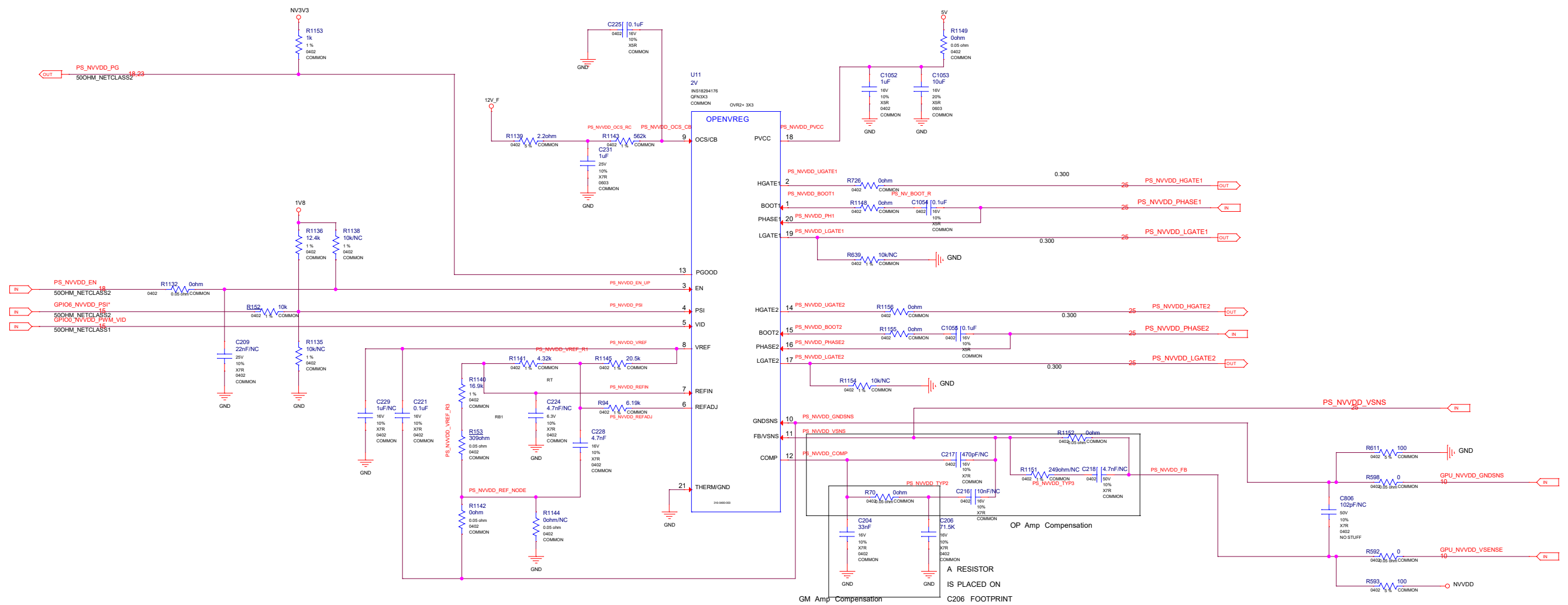
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PS V: NVVDD OVR2+1

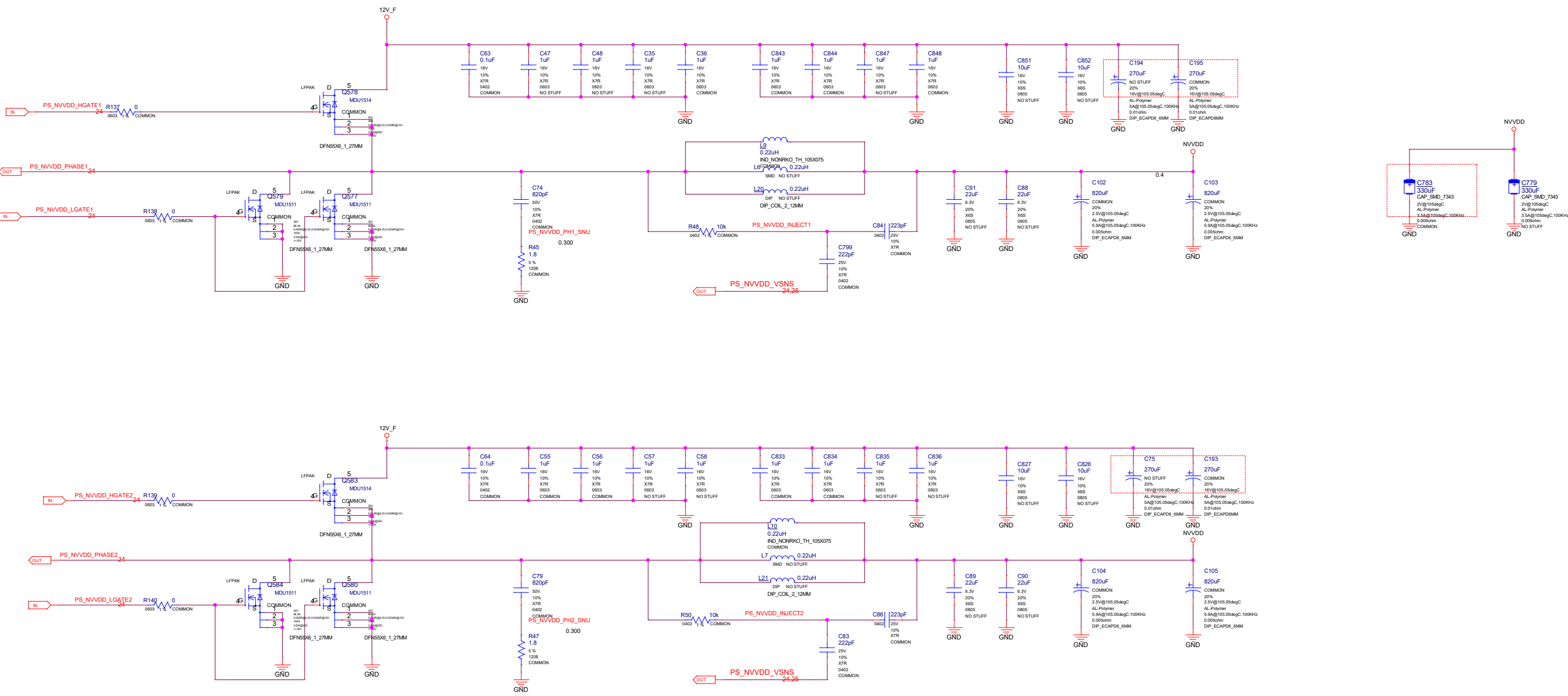


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PS V: NVVDD Phase 1,2



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Page Name:

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Size

Project Name:

Design By:

Rev

Custom

P75L

James

V10

Date:

Wednesday, December 21, 2016

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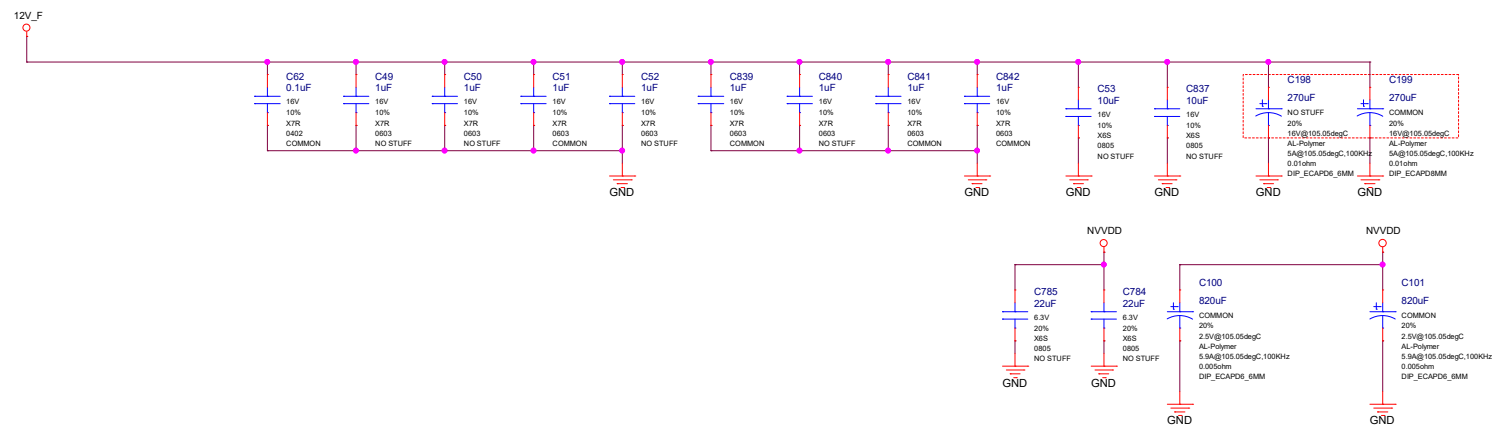
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PS V: NVVDD Phase 3



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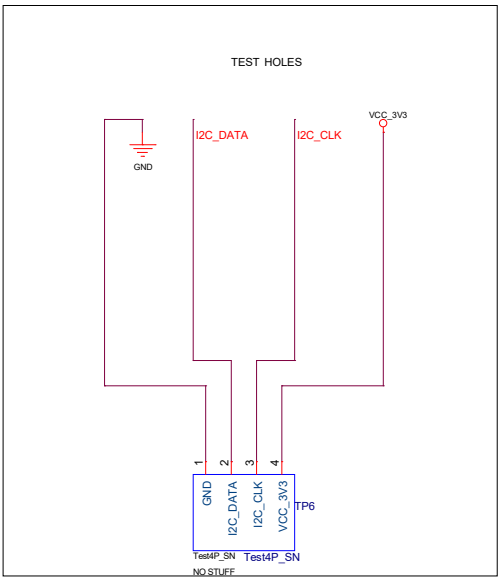
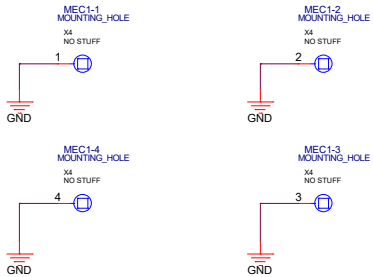
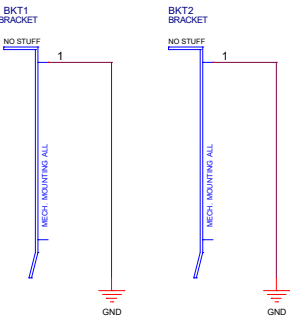


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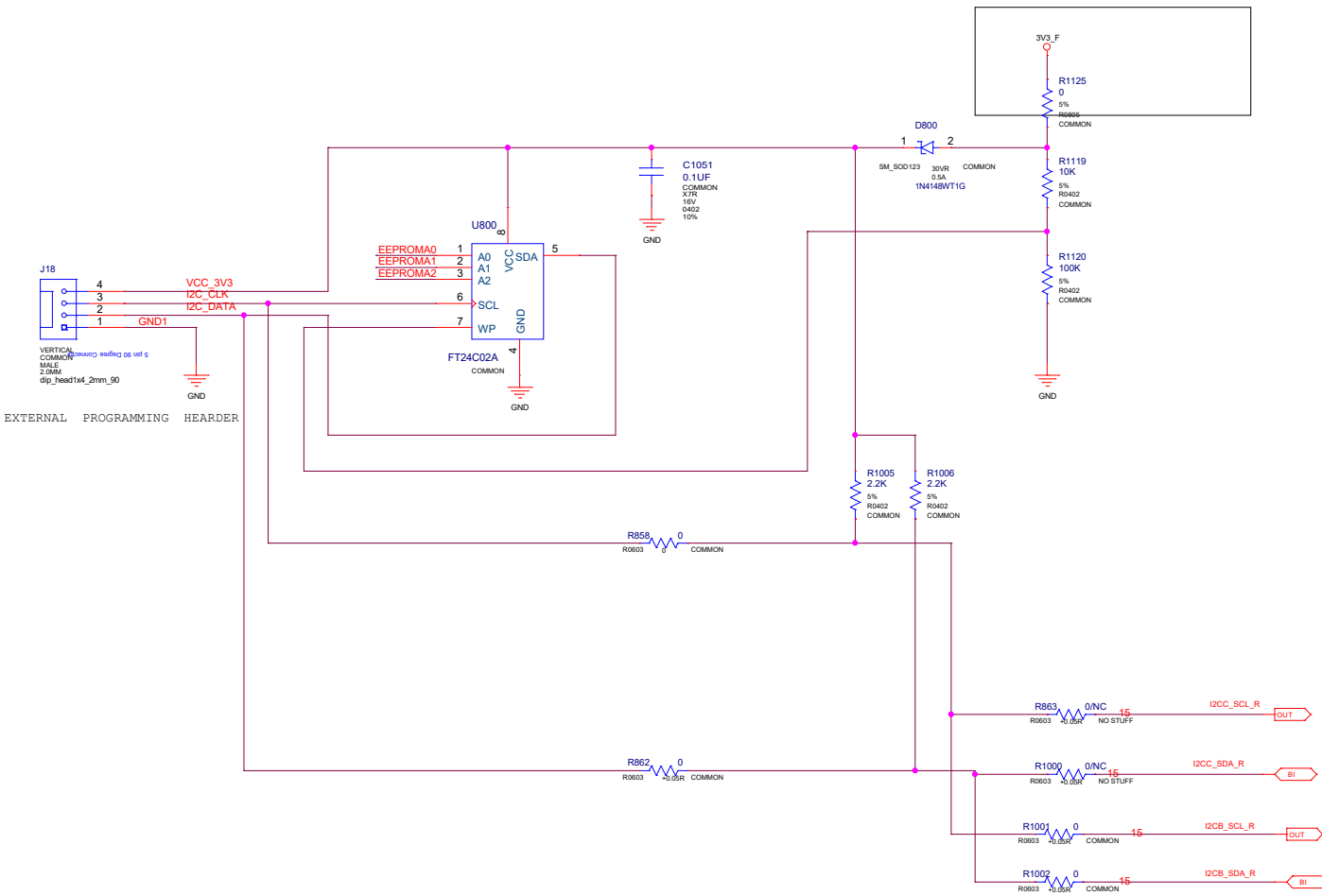
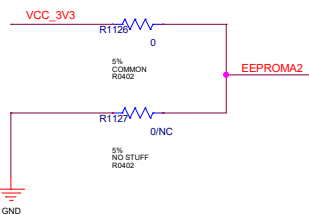
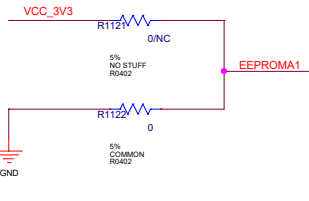
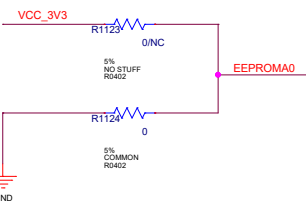
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SN EPROM

Brackets:



PLACEMENT IN PCB : (TOP VIEW)
FROM LEFT TO RIGHT : GND,I2C_DATA,I2C_CLK,VCC_3V3



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ASSEMBLY PAGE DETAIL
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MECH: Bracket/Thermal

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