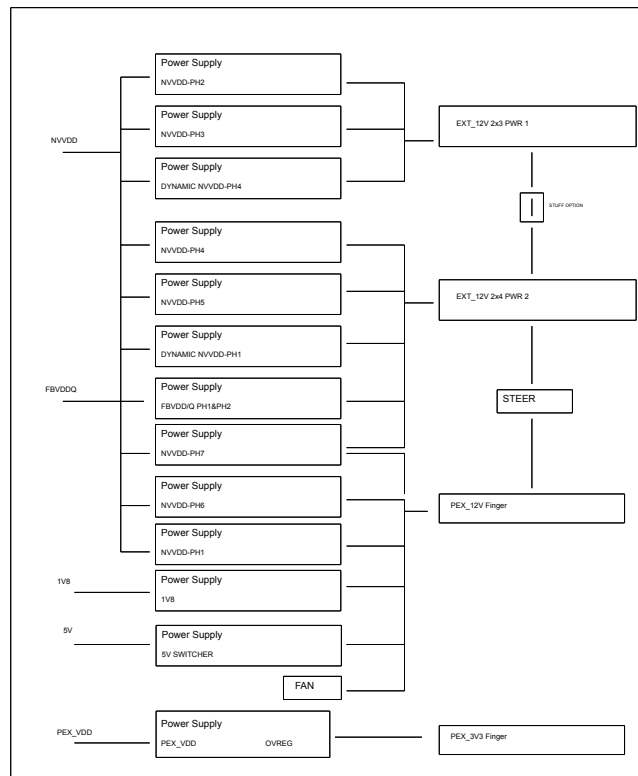
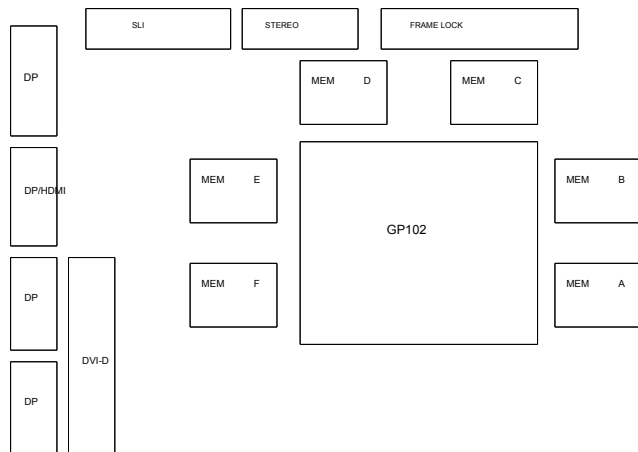


12GB GDDR5X, 384b, 256Mx32
TALL DVI-D + DP + DP + HDMI/DP + DP

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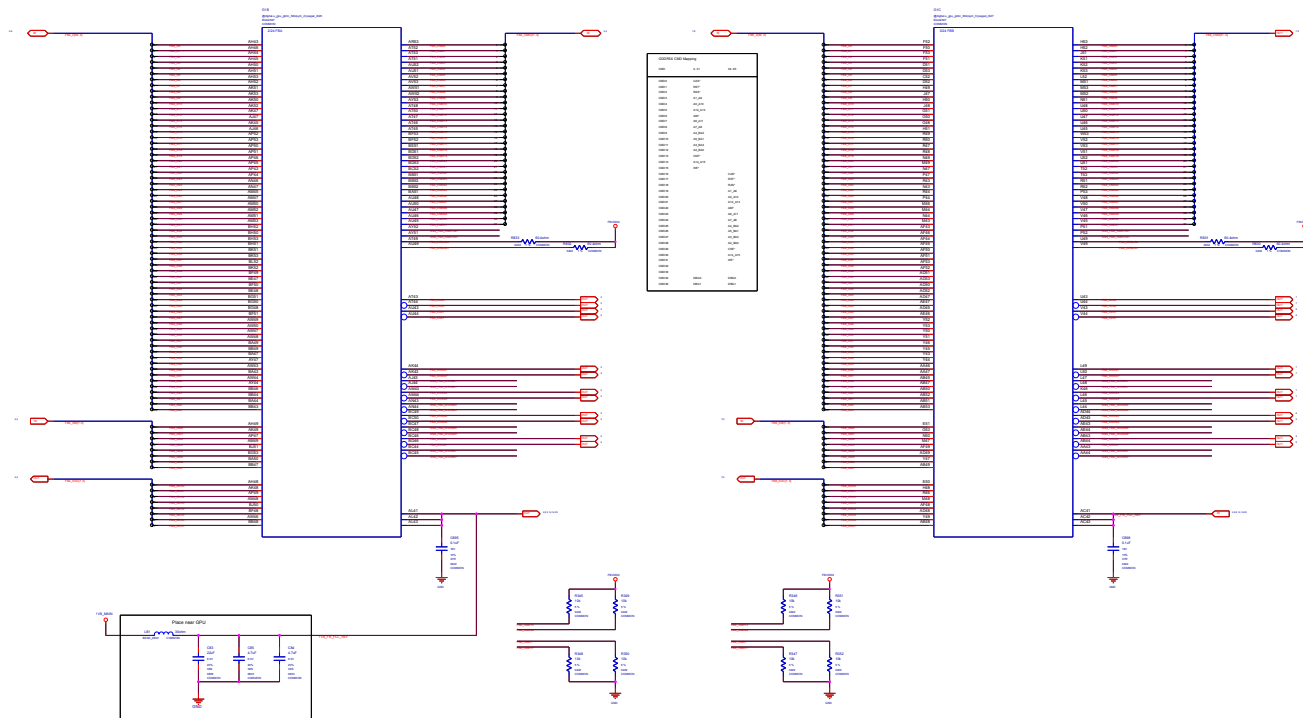


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 3840 LINDEN BLVD
 SANTA CLARA, CA 95051, USA

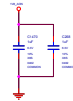
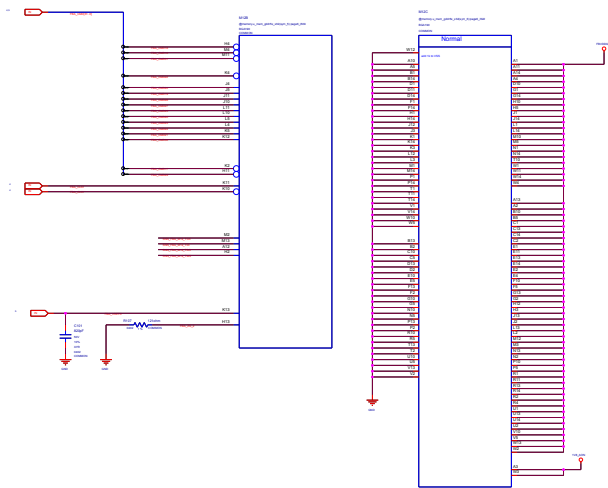


SKU: 10611-BASE-300

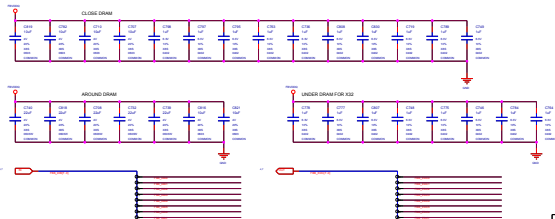
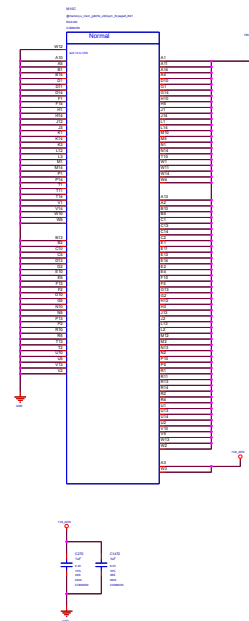
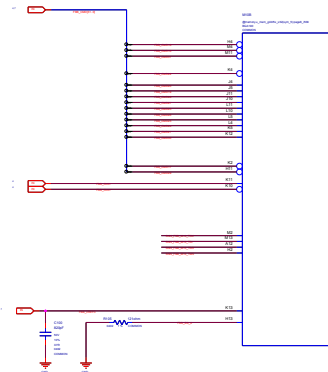
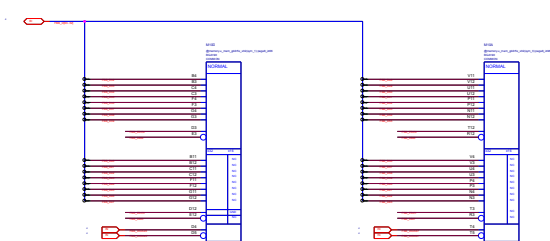
DATE	REV	DESCRIPTION
2018-01-10	1.0	Initial Release











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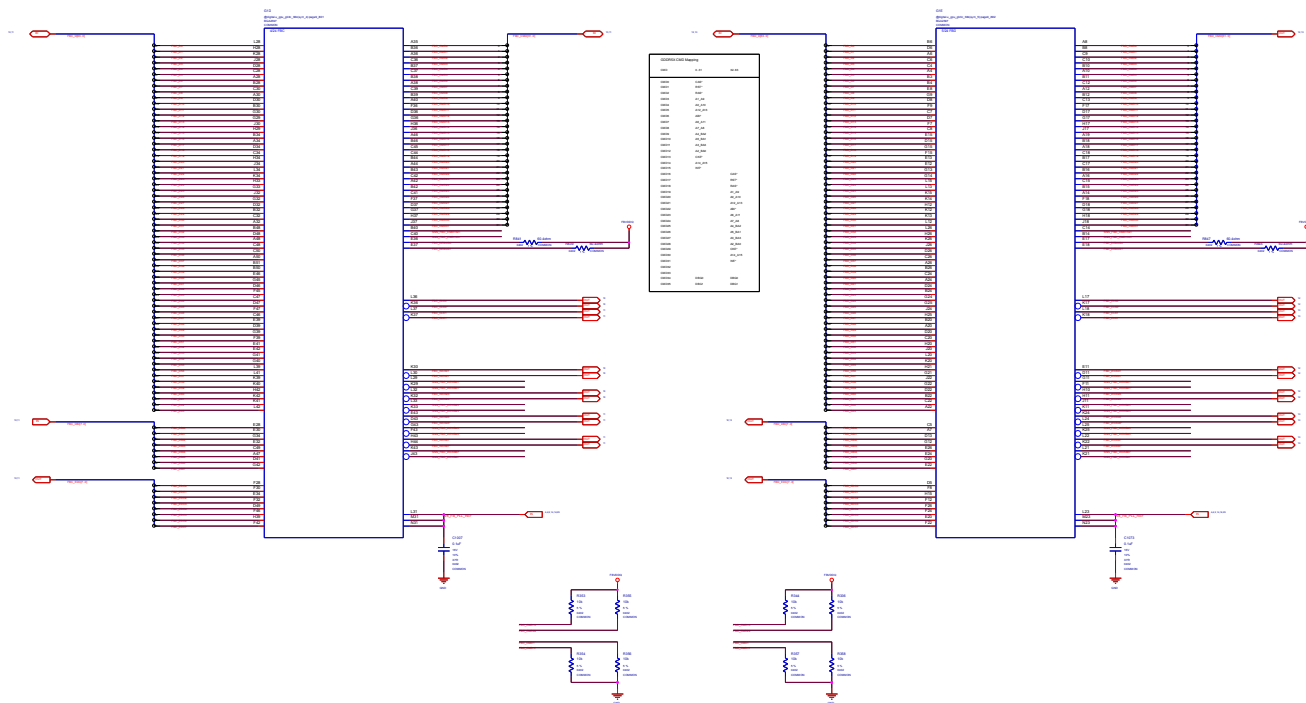
REVISION: 1.0
DATE: 01/11/2007

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100-10811-BASE-300

REV	DATE	BY	CHKD	APPD
1.0	01/11/2007	100-10811-BASE-300		

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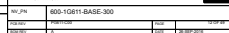


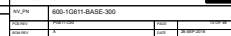
SKU: 800-10811-BASE-300

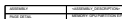
Part No.	Rev.	QTY.	UNIT
800-10811-BASE-300	1.0	1	UNIT

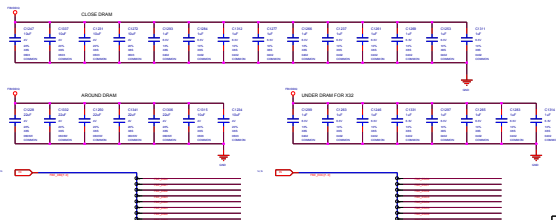
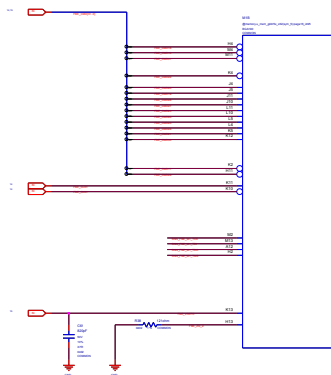








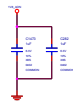


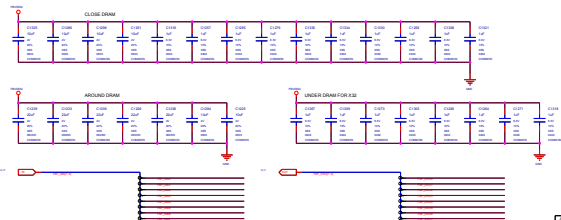
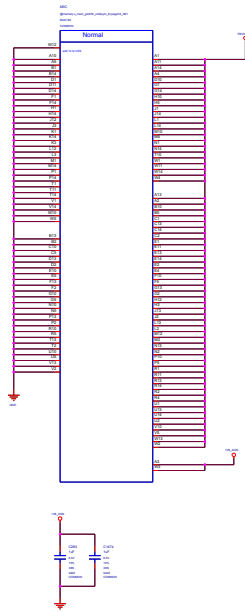


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NV_FN	600-10611-BASE-300		
PLN_REV	PLN11-000	PLN0	16-SEP-20
SCM_REV	A	SCM0	20-SEP-2018



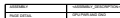


assembly	assembly description
page 1 of 10	assembly for page 1 of 10

2006 SANTOMAS EXPRESS
SANTA CLARA, CA 95050 USA



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BOBREV	A	DATE	26-SEP-2016





2004 SANITARIUM EXPERIMENT

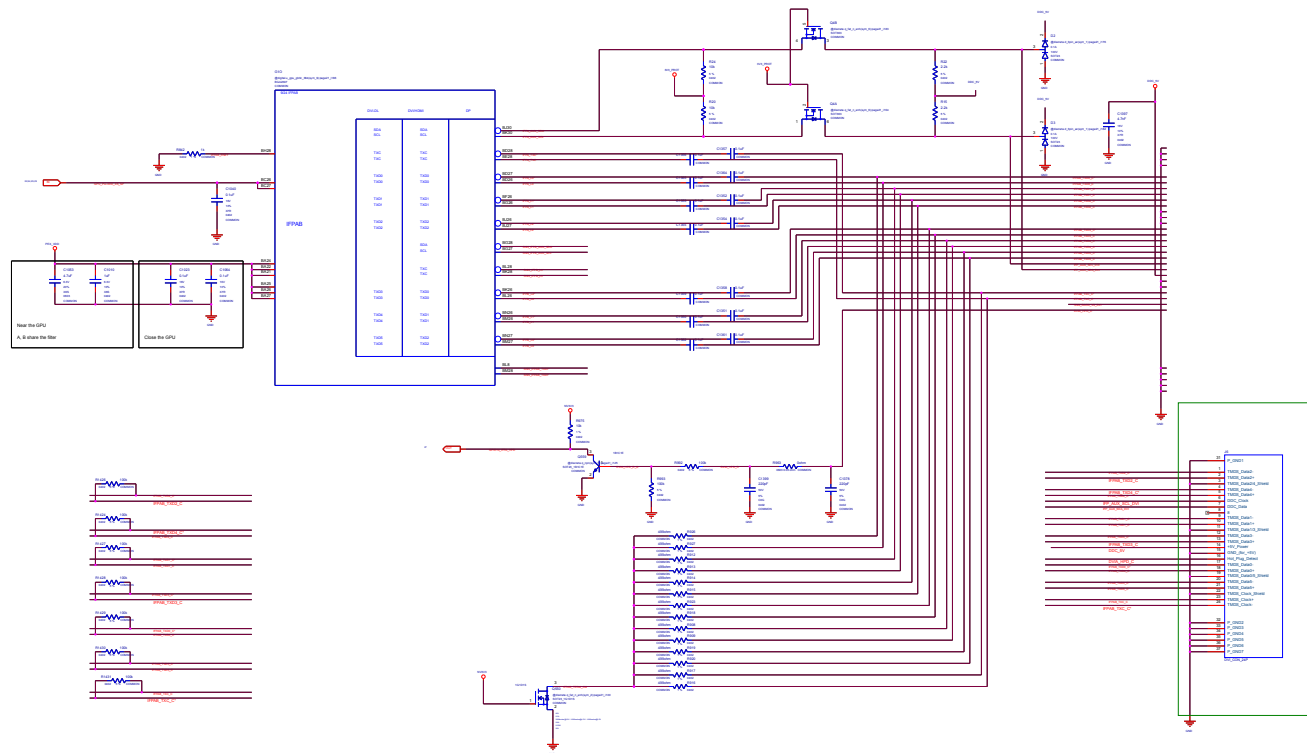
NV_FW	600-10611-BASE-30V
-------	--------------------

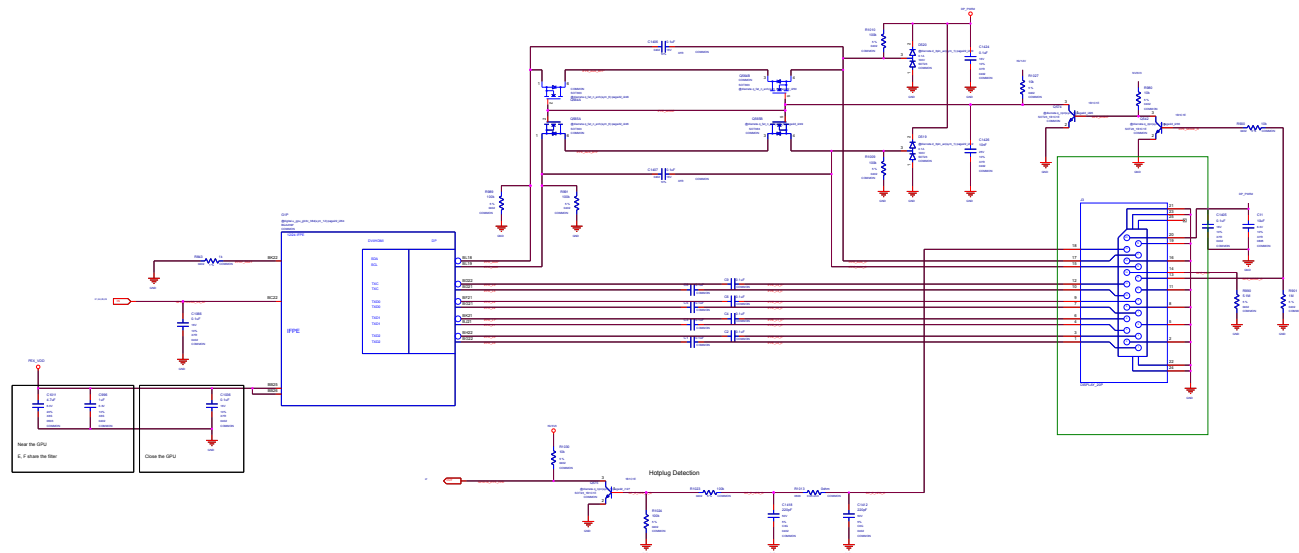
POSSIBLE	PARTICLES
----------	-----------

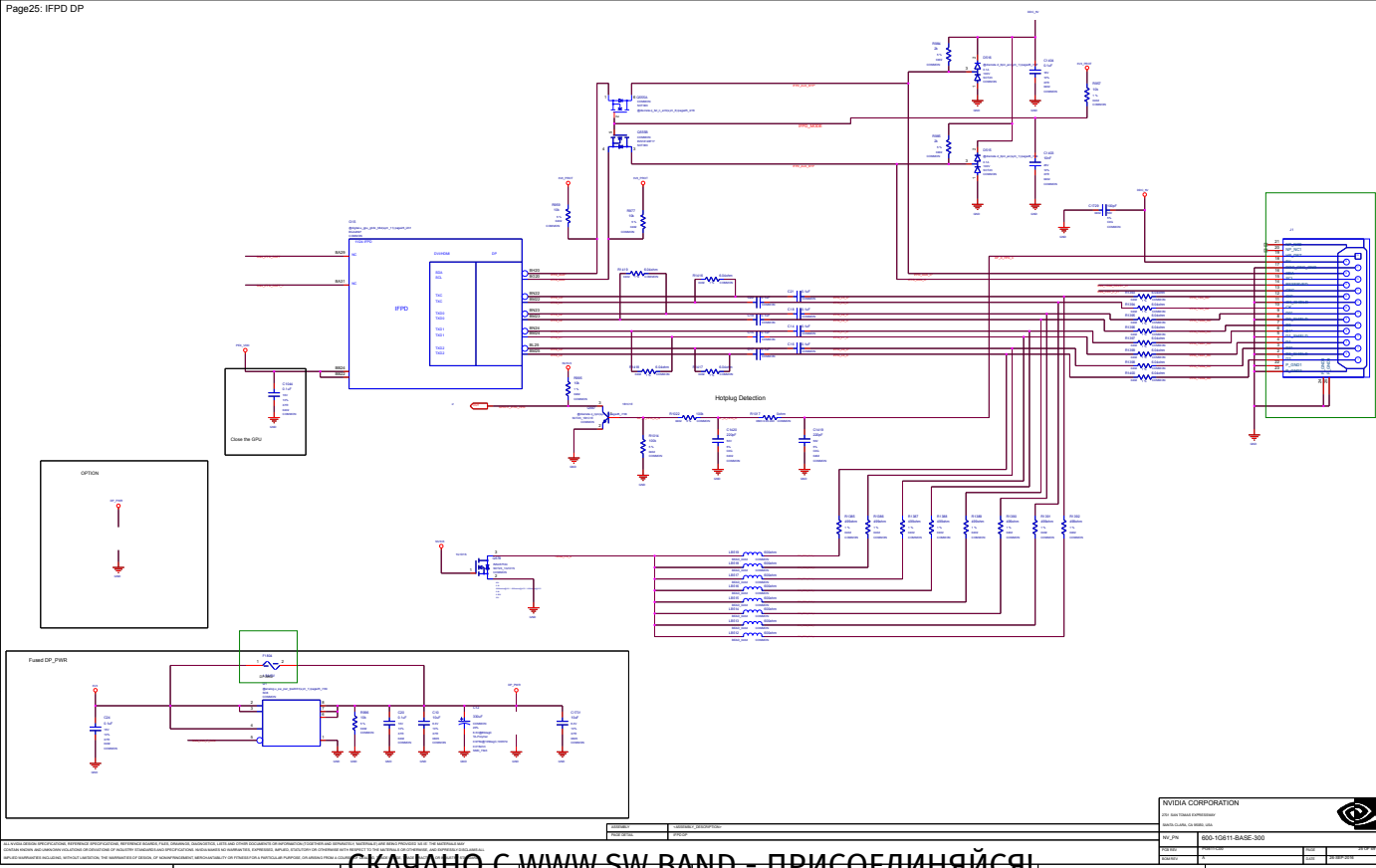
Score	A
-------	---

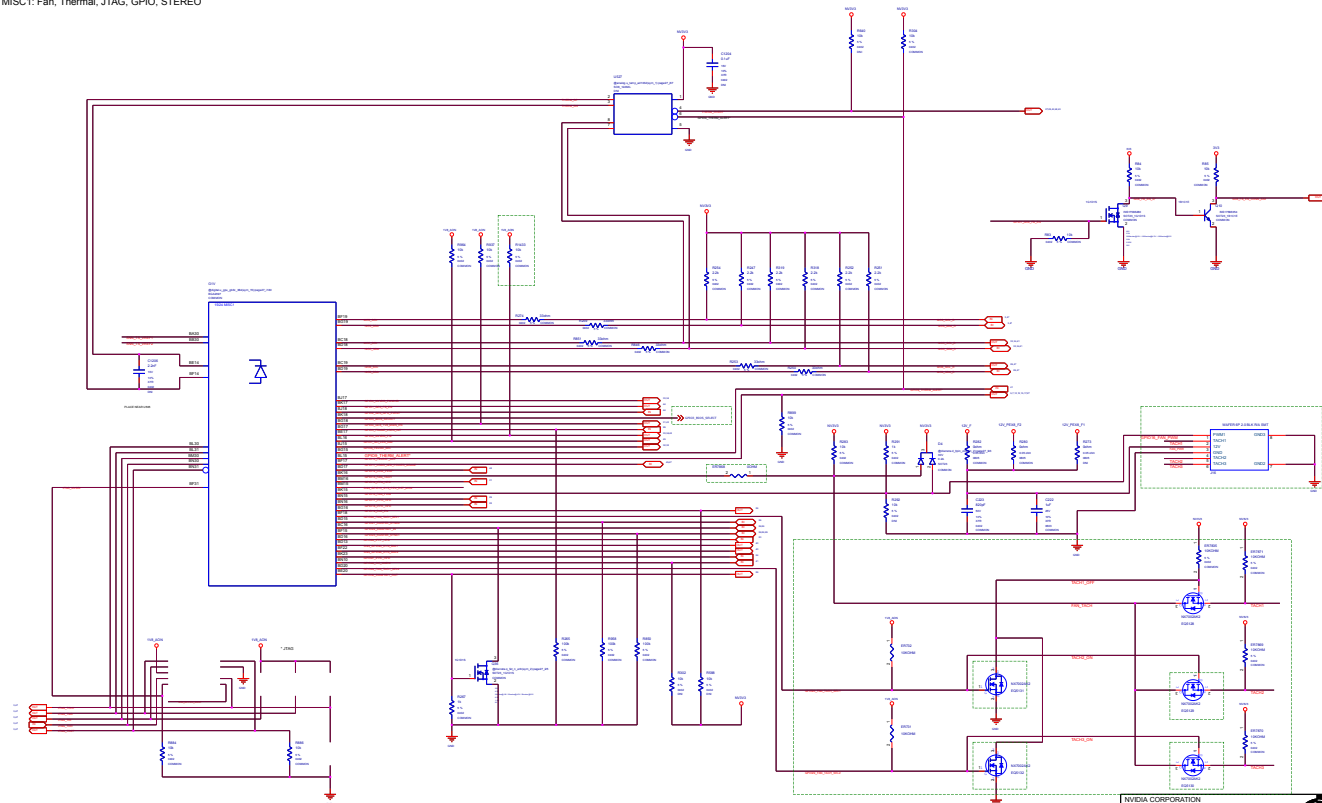
--	--

--	--









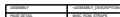
H=High :Tied to 1.5V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVIO_SEL REBRAND
0: DEVIO_SEL ORIGINAL

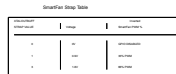
1:PCIE_CFG_LOW_POWER
0:PCIE_CFG_HIGH_POWER

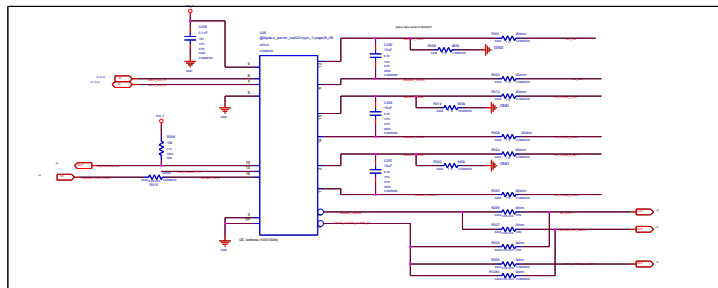
1:VGA_DEVICE_ENABLE
0:VGA_DEVICE_DISABLE



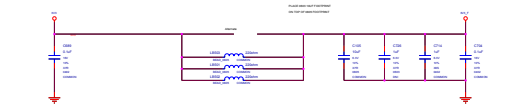
NY PN	600-10611-BASE-30
-------	-------------------

FOR REV	FOR INFO	DATE	28 OF 28
ADDRESS	A	DATE	28 SEP 2015

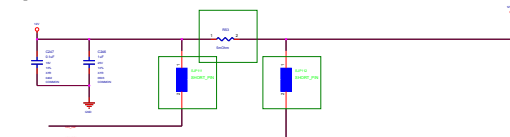




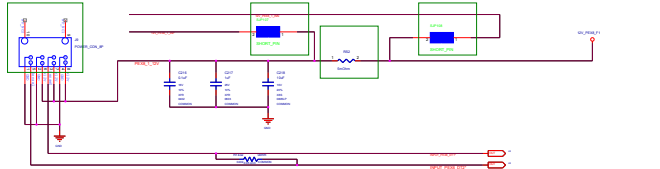
PEX3_V3 INPUT - 10W



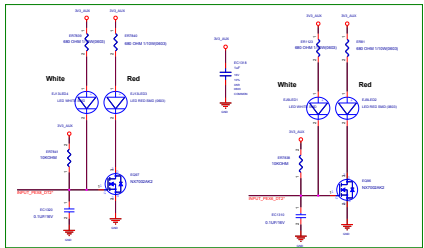
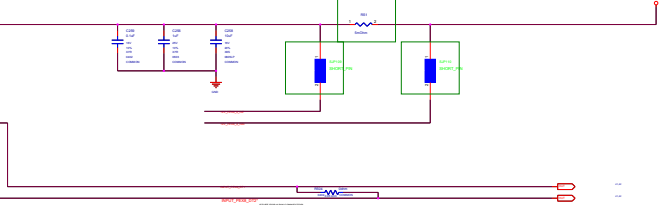
PEX3_V2 INPUT - 60W



PEX3 INPUT 1 - 2x4 POE CON 150W



PEX3 INPUT 2 - 2x4 POE CON 150W



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1000-10811-BASE 300

1000-10811-BASE 300

1000-10811-BASE 300

1000-10811-BASE 300

1000-10811-BASE 300

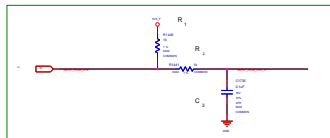
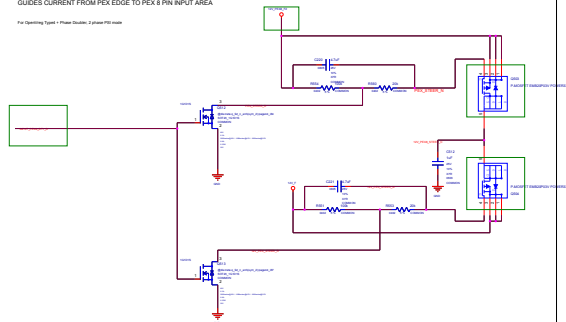
1000-10811-BASE 300

QUADRO TESLA

12V CURRENT STEERING (UNDER POWER BOOT)

GUIDES CURRENT FROM PEX EDGE TO PEX & PIN INPUT AREA

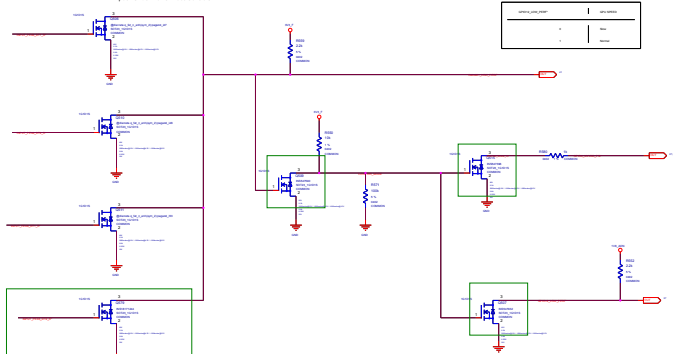
For Operating Type 1 Phase Stealer, 2 phase PEX mode



PCIE IN PCIE CONNECTOR Present

PEX & Input Present

PEX Input - Under Power Boot Controls



A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W series (Quadro Connect) and Quadro Connect to avoid end user confusion.

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QUADRO TESLA
NVIDIA CORPORATION
NVIDIA CORPORATION

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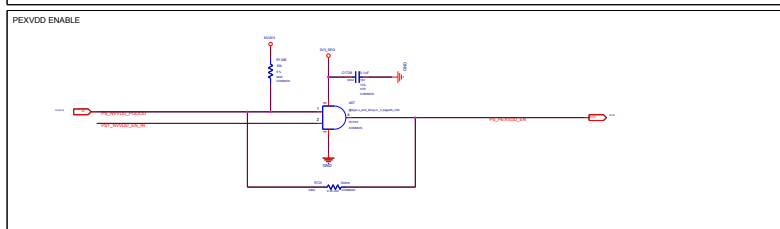
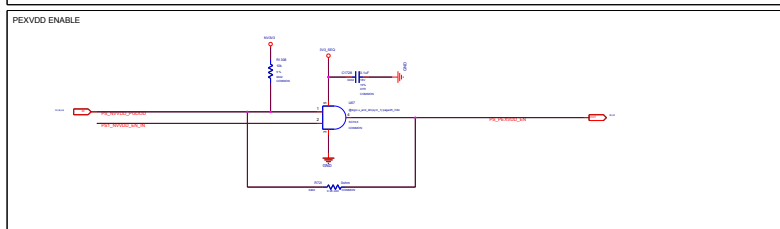
NVIDIA CORPORATION

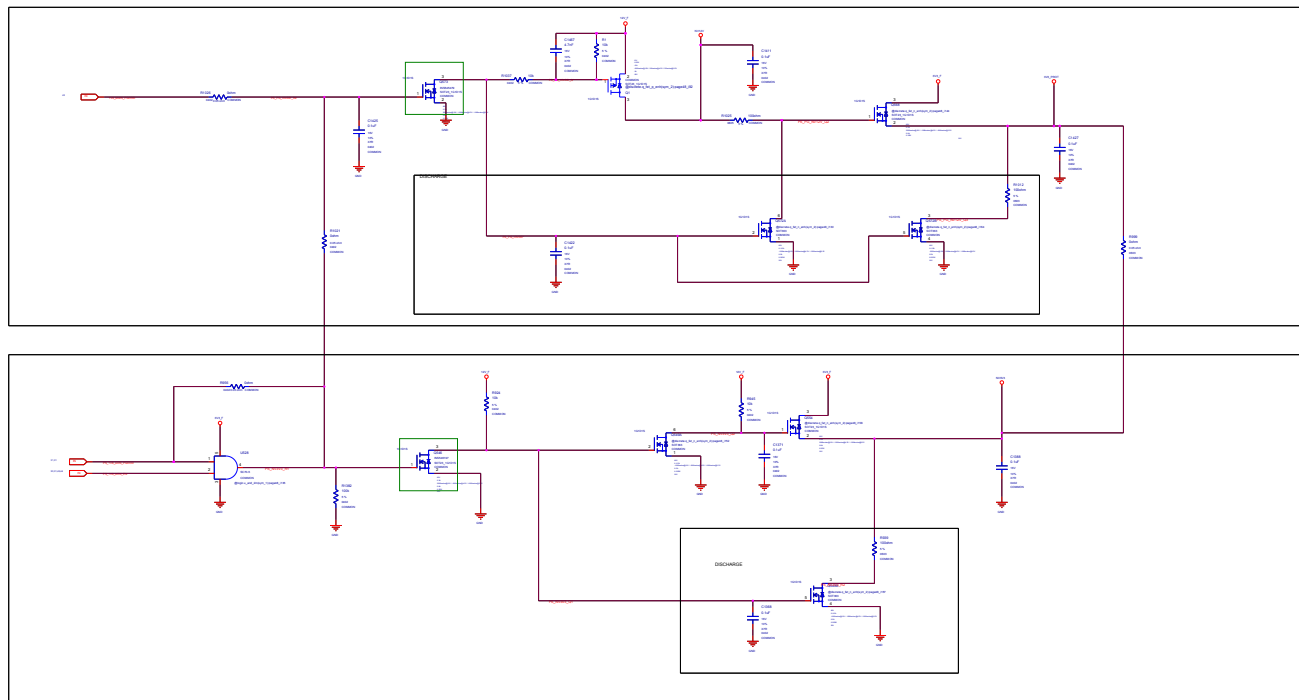
NVIDIA CORPORATION

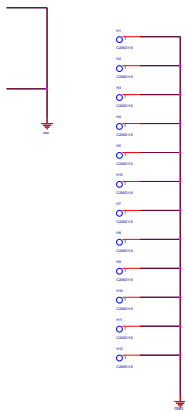
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[contacts](#)

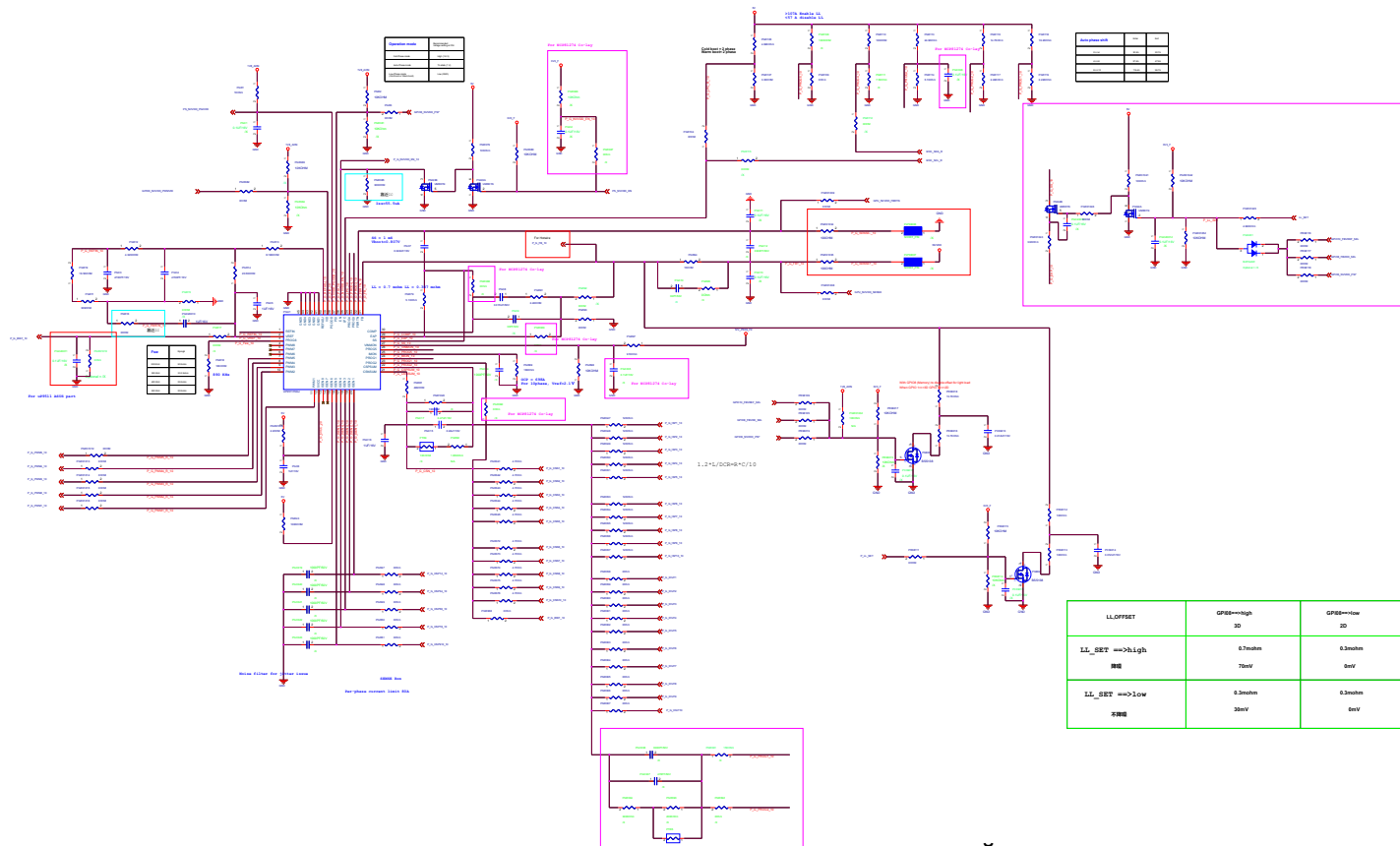
[new to midi - 1000000000](#)
[midi - 1000000000](#)

[illegible]

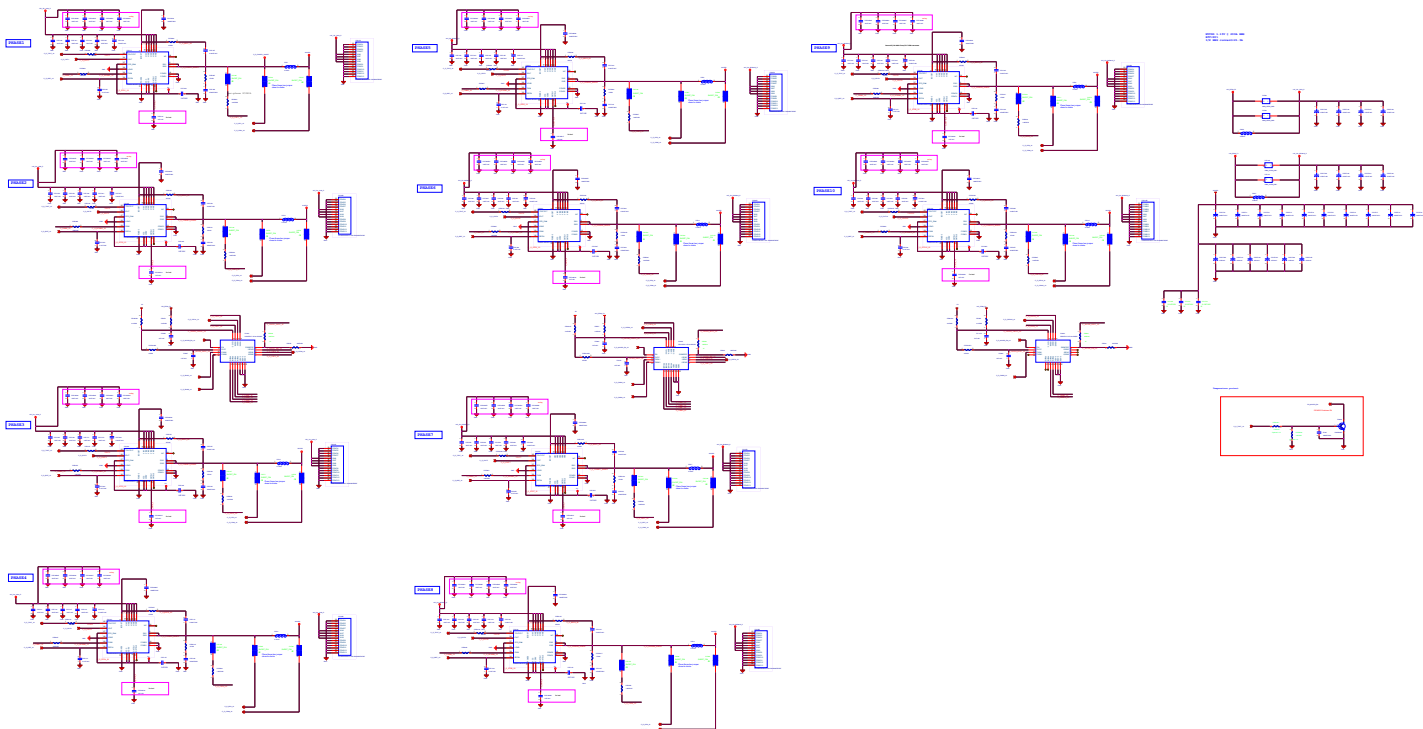
The screenshot shows a PCB layout. A blue rectangular area is labeled "BOARD STIFFENER" with the note "An overmolded mounting plate". To the right, a component labeled "uPIC18" is shown with its pins connected to a common ground symbol. The pins are labeled with their functions: `uPIC18_P1_0`, `uPIC18_P1_1`, `uPIC18_P1_2`, `uPIC18_P1_3`, `uPIC18_P1_4`, `uPIC18_P1_5`, `uPIC18_P1_6`, `uPIC18_P1_7`, `uPIC18_P1_8`, `uPIC18_P1_9`, `uPIC18_P1_10`, `uPIC18_P1_11`, `uPIC18_P1_12`, `uPIC18_P1_13`, `uPIC18_P1_14`, `uPIC18_P1_15`, `uPIC18_P1_16`, `uPIC18_P1_17`, `uPIC18_P1_18`, `uPIC18_P1_19`, `uPIC18_P1_20`, `uPIC18_P1_21`, `uPIC18_P1_22`, `uPIC18_P1_23`, `uPIC18_P1_24`, `uPIC18_P1_25`, `uPIC18_P1_26`, `uPIC18_P1_27`, `uPIC18_P1_28`, `uPIC18_P1_29`, `uPIC18_P1_30`, `uPIC18_P1_31`, `uPIC18_P1_32`, `uPIC18_P1_33`, `uPIC18_P1_34`, `uPIC18_P1_35`, `uPIC18_P1_36`, `uPIC18_P1_37`, `uPIC18_P1_38`, `uPIC18_P1_39`, `uPIC18_P1_40`, `uPIC18_P1_41`, `uPIC18_P1_42`, `uPIC18_P1_43`, `uPIC18_P1_44`, `uPIC18_P1_45`, `uPIC18_P1_46`, `uPIC18_P1_47`, `uPIC18_P1_48`, `uPIC18_P1_49`, `uPIC18_P1_50`, `uPIC18_P1_51`, `uPIC18_P1_52`, `uPIC18_P1_53`, `uPIC18_P1_54`, `uPIC18_P1_55`, `uPIC18_P1_56`, `uPIC18_P1_57`, `uPIC18_P1_58`, `uPIC18_P1_59`, `uPIC18_P1_60`, `uPIC18_P1_61`, `uPIC18_P1_62`, `uPIC18_P1_63`, `uPIC18_P1_64`, `uPIC18_P1_65`, `uPIC18_P1_66`, `uPIC18_P1_67`, `uPIC18_P1_68`, `uPIC18_P1_69`, `uPIC18_P1_70`, `uPIC18_P1_71`, `uPIC18_P1_72`, `uPIC18_P1_73`, `uPIC18_P1_74`, `uPIC18_P1_75`, `uPIC18_P1_76`, `uPIC18_P1_77`, `uPIC18_P1_78`, `uPIC18_P1_79`, `uPIC18_P1_80`, `uPIC18_P1_81`, `uPIC18_P1_82`, `uPIC18_P1_83`, `uPIC18_P1_84`, `uPIC18_P1_85`, `uPIC18_P1_86`, `uPIC18_P1_87`, `uPIC18_P1_88`, `uPIC18_P1_89`, `uPIC18_P1_90`, `uPIC18_P1_91`, `uPIC18_P1_92`, `uPIC18_P1_93`, `uPIC18_P1_94`, `uPIC18_P1_95`, `uPIC18_P1_96`, `uPIC18_P1_97`, `uPIC18_P1_98`, `uPIC18_P1_99`, `uPIC18_P1_100`, `uPIC18_P1_101`, `uPIC18_P1_102`, `uPIC18_P1_103`, `uPIC18_P1_104`, `uPIC18_P1_105`, `uPIC18_P1_106`, `uPIC18_P1_107`, `uPIC18_P1_108`, `uPIC18_P1_109`, `uPIC18_P1_110`, `uPIC18_P1_111`, `uPIC18_P1_112`, `uPIC18_P1_113`, `uPIC18_P1_114`, `uPIC18_P1_115`, `uPIC18_P1_116`, `uPIC18_P1_117`, `uPIC18_P1_118`, `uPIC18_P1_119`, `uPIC18_P1_120`, `uPIC18_P1_121`, `uPIC18_P1_122`, `uPIC18_P1_123`, `uPIC18_P1_124`, `uPIC18_P1_125`, `uPIC18_P1_126`, `uPIC18_P1_127`, `uPIC18_P1_128`, `uPIC18_P1_129`, `uPIC18_P1_130`, `uPIC18_P1_131`, `uPIC18_P1_132`, `uPIC18_P1_133`, `uPIC18_P1_134`, `uPIC18_P1_135`, `uPIC18_P1_136`, `uPIC18_P1_137`, `uPIC18_P1_138`, `uPIC18_P1_139`, `uPIC18_P1_140`, `uPIC18_P1_141`, `uPIC18_P1_142`, `uPIC18_P1_143`, `uPIC18_P1_144`, `uPIC18_P1_145`, `uPIC18_P1_146`, `uPIC18_P1_147`, `uPIC18_P1_148`, `uPIC18_P1_149`, `uPIC18_P1_150`, `uPIC18_P1_151`, `uPIC18_P1_152`, `uPIC18_P1_153`, `uPIC18_P1_154`, `uPIC18_P1_155`, `uPIC18_P1_156`, `uPIC18_P1_157`, `uPIC18_P1_158`, `uPIC18_P1_159`, `uPIC18_P1_160`, `uPIC18_P1_161`, `uPIC18_P1_162`, `uPIC18_P1_163`, `uPIC18_P1_164`, `uPIC18_P1_165`, `uPIC18_P1_166`, `uPIC18_P1_167`, `uPIC18_P1_168`, `uPIC18_P1_169`, `uPIC18_P1_170`, `uPIC18_P1_171`, `uPIC18_P1_172`, `uPIC18_P1_173`, `uPIC18_P1_174`, `uPIC18_P1_175`, `uPIC18_P1_176`, `uPIC18_P1_177`, `uPIC18_P1_178`, `uPIC18_P1_179`, `uPIC18_P1_180`, `uPIC18_P1_181`, `uPIC18_P1_182`, `uPIC18_P1_183`, `uPIC18_P1_184`, `uPIC18_P1_185`, `uPIC18_P1_186`, `uPIC18_P1_187`, `uPIC18_P1_188`, `uPIC18_P1_189`, `uPIC18_P1_190`, `uPIC18_P1_191`, `uPIC18_P1_192`, `uPIC18_P1_193`, `uPIC18_P1_194`, `uPIC18_P1_195`, `uPIC18_P1_196`, `uPIC18_P1_197`, `uPIC18_P1_198`, `uPIC18_P1_199`, `uPIC18_P1_200`, `uPIC18_P1_201`, `uPIC18_P1_202`, `uPIC18_P1_203`, `uPIC18_P1_204`, `uPIC18_P1_205`, `uPIC18_P1_206`, `uPIC18_P1_207`, `uPIC18_P1_208`, `uPIC18_P1_209`, `uPIC18_P1_210`, `uPIC18_P1_211`, `uPIC18_P1_212`, `uPIC18_P1_213`, `uPIC18_P1_214`, `uPIC18_P1_215`, `uPIC18_P1_216`, `uPIC18_P1_217`, `uPIC18_P1_218`, `uPIC18_P1_219`, `uPIC18_P1_220`, `uPIC18_P1_221`, `uPIC18_P1_222`, `uPIC18_P1_223`, `uPIC18_P1_224`, `uPIC18_P1_225`, `uPIC18_P1_226`, `uPIC18_P1_227`, `uPIC18_P1_228`, `uPIC18_P1_229`, `uPIC18_P1_230`, `uPIC18_P1_231`, `uPIC18_P1_232`, `uPIC18_P1_233`, `uPIC18_P1_234`, `uPIC18_P1_235`, `uPIC18_P1_236`, `uPIC18_P1_237`, `uPIC18_P1_238`, `uPIC18_P1_239`, `uPIC18_P1_240`, `uPIC18_P1_241`, `uPIC18_P1_242`, `uPIC18_P1_243`, `uPIC18_P1_244`, `uPIC18_P1_245`, `uPIC18_P1_246`, `uPIC18_P1_247`, `uPIC18_P1_248`, `uPIC18_P1_249`, `uPIC18_P1_250`, `uPIC18_P1_251`, `uPIC18_P1_252`, `uPIC18_P1_253`, `uPIC18_P1_254`, `uPIC18_P1_255`, `uPIC18_P1_2`

STIFFENER

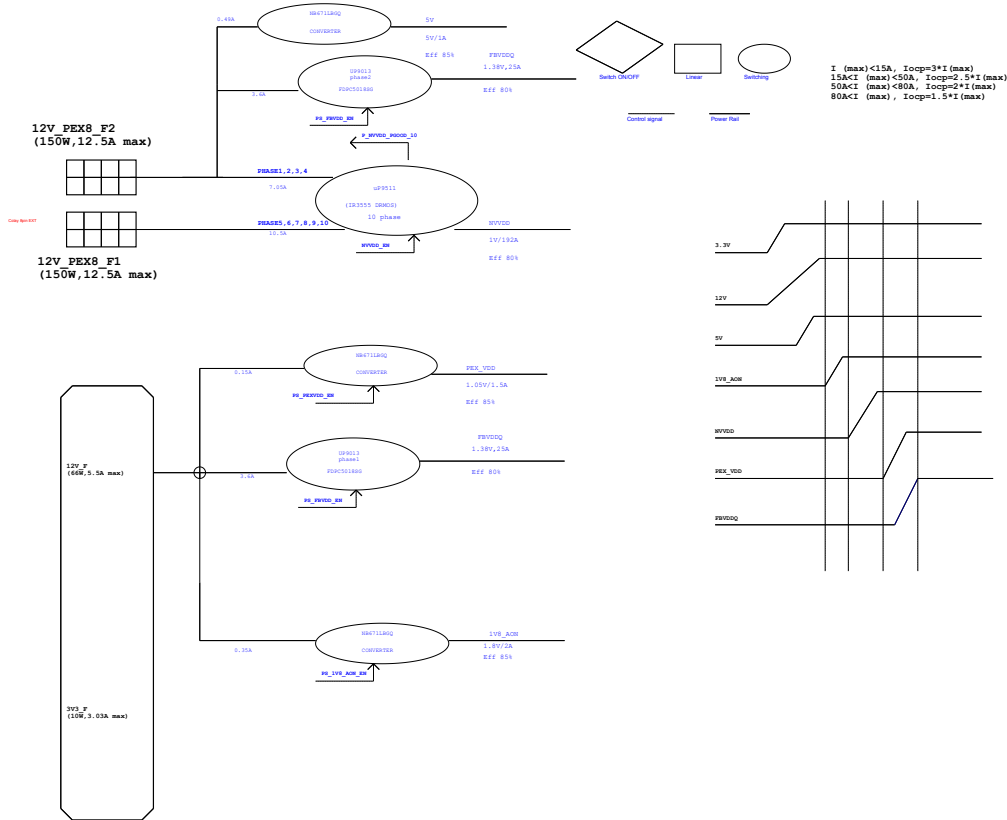


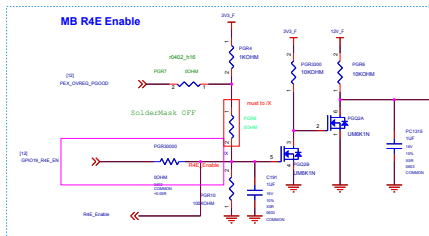
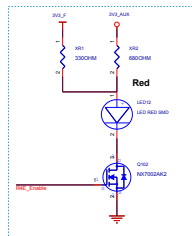


СКАЧАНО С WWW.SW.BAND - ПРИСОЕДИНЯЙСЯ!

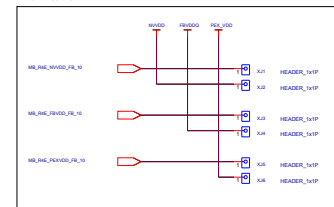


СКАЧАНО С WWW.SW.BAND - ПРИСОЕДИНЯЙСЯ!





MB VGA HotWire



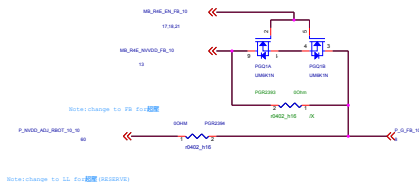
P-STATE VOLTAGES

1. P0 at 1.05V to 1.15V (depending on VB)
2. P0P12 at 0.80V

SOFT START (VR11)

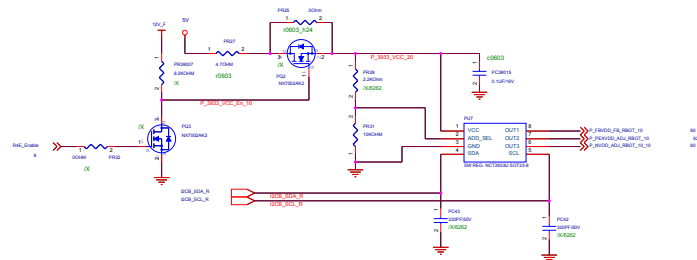
1. Ramp 0V to 1.15V in ~5ms
2. Hold at 1.15V for 100ms
3. Read VID
4. VID set to 0.8V during GPO to stable VID@ 10-1000 to set 0.9125V

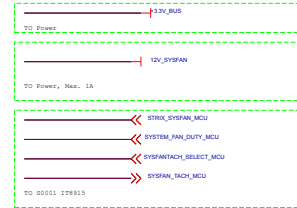
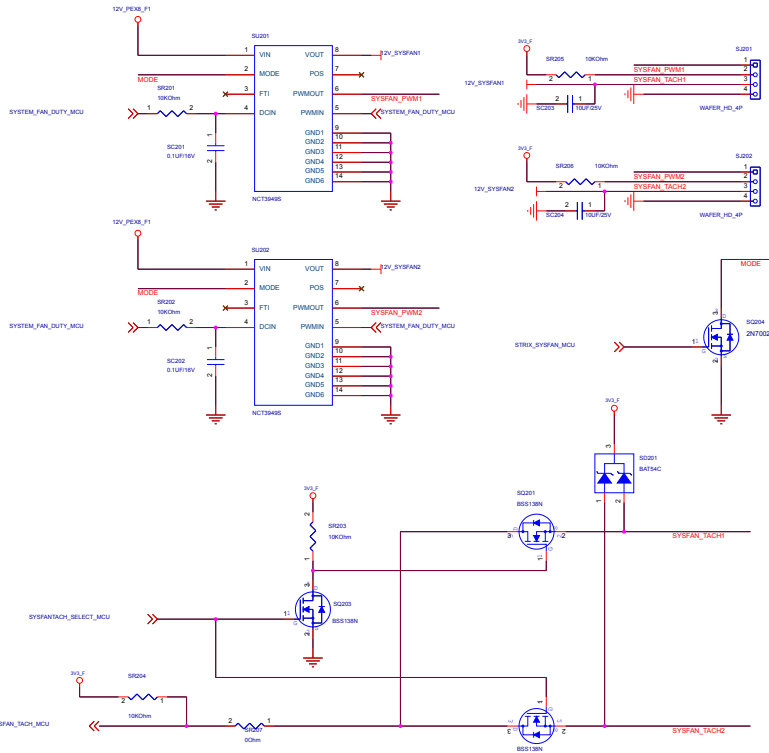
For MB R4E的预留超压电路



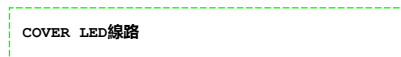
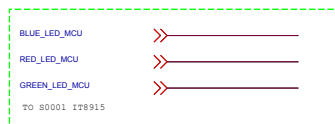
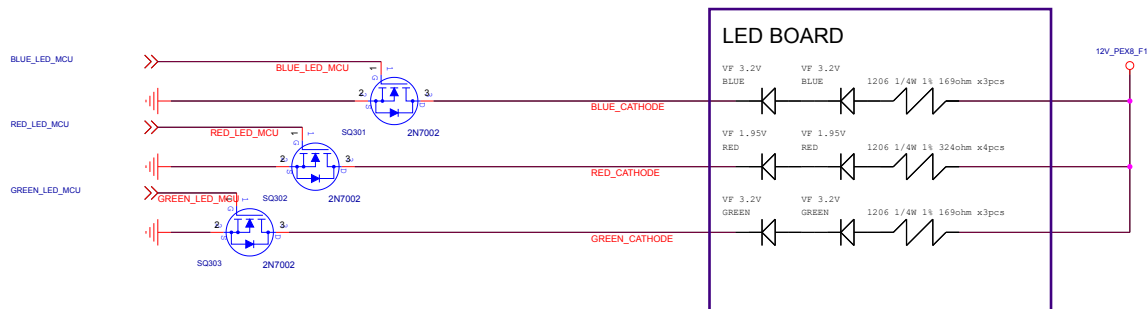
NCT3933U Over Voltage

Address : 0x2A





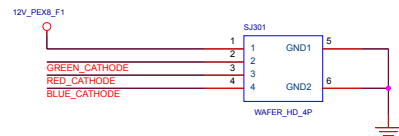
STRIX_SYSFAN_MCU	Mode
L	NORMAL
H(Default)	STRIX
SYSFANTACH_SELECT_MCU	Mode
L	SYSFAN_TACH1
H(Default)	SYSFAN_TACH2

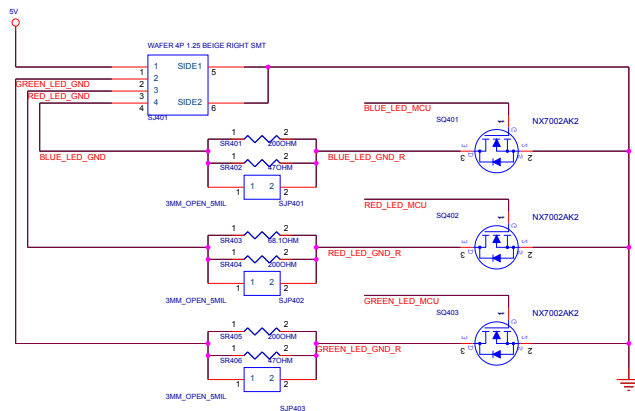


示意圖



連接座旁請註明 12V G R B

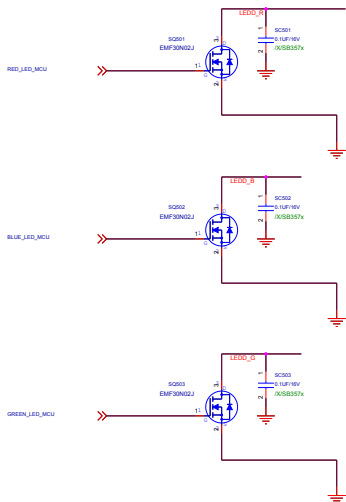
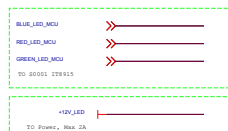




背板ROG LED線路

TO Power

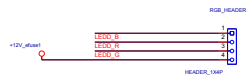
BLUE_LED_MCU
RED_LED_MCU
GREEN_LED_MCU
TO S0001 IT8915



示意图



連接座旁請註明 12V G R B
 RGB Header



eFuse

